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Sorting of STS-XYTER2 data for microslice building for CBM experiment

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The readout system for triggerless High Energy Physics experiments, recently under intense development, contain an aggregation and data processing modules. They are responsible for collecting data from multiple input links, pre-processing and packaging them into containers for the event selection module located next in the readout chain.
The presented article discusses design considerations for such module, inspired by requirements of the readout in the CBM experiment and prepared for the DPB/CRI aggregation module.

Summary

The presented article discusses a sorting solution designed for the FPGA firmware to be used in data aggregation and sorting module, prepared for CBM - a High Energy Physics (HEP) experiment, designed to investigate matter properties under extremely high densities.
In order to minimize a possibility of discarding any valuable data, CBM will have a triggerless readout chain. Data captured by FEE will be streamed down the readout chain all the way to the software event selector. It will reconstruct collisions based on whole data registered in a certain time interval.
The Data Processing Board (DPB) and the Common Readout Interface (CRI) are the following generations of data aggregation elements of CBM readout chain. Both elements contain FPGA chips that share similar aggregation and sorting module. CRI provide more logical resources, enabling instantiation of more aggregation modules working in parallel, and aggregation of a higher number of input streams.
The Front End Electronics (FEE) ASIC for many detectors in the CBM experiment, is STS-XYTER2. It generates a stream of data with throughput up to 10 millions samples per second. Each sample is marked with a timestamp. The samples are generally ordered according to their timestamps, but in certain heavy load conditions the strict sorting is not possible and certain disorder is introduced into the data stream. The data streams from multiple FEE ASICs are aggregated in the DPB/CRI into a high bandwidth stream. The aggregated data are split into so-called Microslices (MCSs), containing hits recorded in a certain period of time.
In order to create valid MCSs the DPB/CRI buffers all the data, for long enough to account for the delay, before the MCS is sent to the FLES. The data may be strictly sorted inside DPB/CRI, depending on available logical resources.
The article starts with an introduction to data acquisition requirements for triggerless High Energy Physics experiments. We discuss general considerations in designing an aggregation and sorting module for such experiment.
The second section starts with a selection of optimal aggregation throughput, based on experiment requirements, hardware utilization, performance, and reliability.
Next, we describe a few data sorting algorithms, possible to implement on FPGA device, and discuss which one is the best suited for triggerless HEP data concentrator. Firmware architectures containing sorting and aggregation elements are discussed at the end of the section.
The last section of the presented paper starts with a summary of previous development. Next, we give a detailed analysis of final aggregation and sorting firmware of DPB/CRI module. We describe our design choices

and justify them in CBM environment. The section is ended with a listing of achieved performance and resource utilization.

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