The VMM front-end integration in the Scalable Readout System: On the way to a next generation readout system for generic detector R&D and experiment instrumentation

Michael Lupberger (CERN)

TWEPP, Antwerp, 18.09.2018
Outline

Introduction: What is SRS?

SRS and front-end ASICs

VMM integration in SRS

Status and applications

Conclusion

(Personal) ideas for the future
What is SRS?

Scalable Readout System:
A generic readout system for laboratory and detector instrumentation developed and supported by the RD51 Collaboration since 2009
(Inventor: H. Müller)

RD51: CERN project and collaboration with more than 500 members from about 90 institutes, recently approved by LHCC for a continuation until 2024
What is SRS?

Front-end ASIC(s) → Hybrid → Detector

HDMI/optical links specific protocol
What is SRS?

- Adapter card
- Detector
- Front-end ASIC(s)
- Master only
- Detector
- Front-end ASIC(s)
- Master/Slave
- Detector
- HDMI/optical links
  specific protocol
- 8x1
- 4x2
- 8x1
What is SRS?

- Front-end ASIC(s)
  - Hybrid
  - 8x1
  - 8x1
  - 4x2

- Detector
  - Master only
  - Master/Slave

- HDMI/optical links
  - specific protocol
What is SRS?

- **Trigger** from PC
- **SRU**
  - 10 GbE data
  - 40x 1 GbE data, trigger, clock, control links (CAT5)
  - 4x2 HDMI/optical links specific protocol

- **FEC Adapter card**
  - 8x1

- **Front-end ASIC(s)**
  - Hybrid
  - Hybrid
  - Hybrid
  - Hybrid

- **Detector**
  - Master only
  - Master/Slave
What is SRS?

10 GbE data

PC

SRU

1 GbE data, trigger, clock, control links (CAT5)

40x

1 GbE CAT5

or

Ethernet switch

+ 

Trigger

Clock & trigger generator fan-out (CAT5)

1 GbE data, control (CAT5)

Front-end ASIC(s)

Master only

Detector

Master/Slave

Hybrid

1 GbE data, trigger, clock, control links (CAT5)

8x1

FEC Adapter card

Hybrid

Hybrid

Hybrid

Hybrid

Hybrid

4x2

HDMI/optical links specific protocol

1 GbE

CAT5

10 GbE

data

Trigger
What is SRS?

Example AVP25 (strip readout) up to:
- 82k ch/SRU
- 2048 ch/FEC
- 128 ch/hybrid + (master/slave)

Front-end ASIC(s)
- Hybrid
- Master only
- Detector
- Master/Slave
- Detector

Ethernet switch or +
- 1 GbE data, control (CAT5)
- 40x

1 GbE data, trigger, clock, control links (CAT5)
- 8x1

Clock & trigger generator fan-out (CAT5)

10 GbE data

PC

SRU

FEC Adapter card

FEC Adapter card

FEC Adapter card

HDMI/optical links specific protocol

1 GbE data, trigger, clock, control links (CAT5)
- 4x2

Fan-out (CAT5)
What is SRS?

1 GbE or DDTC to SRU

FECv6 (2013)

Virtex-6

CTGF v3

FECv3 (2010)

Virtex-5

SRU

10 GbE SFP+

40x DDTC from FECs
SRS and front-end ASICs

Different ASICs are implemented in SRS:
- APV25 (backbone of MPGD R&D)
- Beetle
- VFAT
- Timepix
- SiPMs

Ongoing:
- Timepix3
- VMM (future backbone, as APV25 is discontinued)

Future:
SAMPA?
APV25 ASIC: Readout chip for CMS tracker
- 250 nm CMOS technology
- Delivered: 2001
- Configuration via I2C
- 128 channels with preamp and shaper
- Output: multiplexed analogue levels
- 40MHz clock

APV25 hybrid:
- One APV25 ASIC
- PLL
- LDO for power
- Master/Slave
- Protection circuit

Adapter card:
- Mainly ADCs
- Can read up to 16 APV25 hybrids

S. Martoiu et al., Development of the scalable readout system for micro-pattern gas detectors and other applications, JINST 8.03 (2013), C03015
SRS APV

1) Detection and imaging of high-Z materials with a muon tomography station using GEM detectors

2) Performance in Test Beam of a Large-area and Light-weight GEM detector with 2D Stereo-Angle (U-V) Strip Readout

3) GEM-based polarimeter detector development for storage ring EDM experiment
S. Park, Presentation given at the AFAD2018, Jan 2018.

4) Development and test of the DAQ system for a Micromegas prototype installed in the ATLAS experiment

5) Performance studies under high irradiation of resistive bulk Micromegas chambers at the CERN Gamma Irradiation Facility

6) Characterization of triple-GEM detectors for the Phase I Muon System Upgrade of the CMS Experiment at LHC

7) More than 100 systems sold via CERN store
SRS APV - Drawbacks

- ASIC is more than 15 years old
- Low trigger rate $O(10 \text{ kHz})$
- Low data rate due to multiplexed analog output of ASIC
- Limited input capacitance range $< 50 \text{ pF}$
- Limited gain range
- No zero suppression in ASIC (only on FEC)
- Export restrictions
- No new production of the ASCI CERN store stock $< 600$ hybrids

$\Rightarrow$ New ASIC implementation required
VMM front-end ASIC

- 130 nm CMOS technology
- 64 input channels, each w/ preamplifier, shaper, peak detector, several ADCs
- Pos. & neg. polarity sensitive
- Digital block w/ neighbouring logic, FIFO, multiplexer
- Adjustable gain 0.5-16 mV/fC
- Adjustable shaping time from 25 ns – 200 ns
- Input capacitance from few pF – 1 nF
VMM front-end ASIC

- Internal test pulser with adjustable amplitude
- Global threshold & adjustment per channel
- Self-triggered, zero suppressed
- 38 bit per hit

(if input charge goes over threshold)

1. Event flag (1 bit)
2. Over threshold flag (1 bit)
3. Channel number (6 bit)
4. Signal amplitude (10 bit)
5. Arrival time (20 bit)
Implementation of the VMM ASIC in SRS

Project in Gaseous Detector Development group at CERN

- funded by EU BrightnESS and AIDA2020 project and the detector group of the European Spallation Source ESS
- Project driver: NMX instrument at ESS
- Benefit for whole RD51 community and beyond
- Goal: replace SRS APV as backbone for MPGD R&D
  - THE readout for the next decade within the community
  - Application beyond the community
  - Application beyond R&D → experiments
Implementation of the VMM ASIC in SRS

Status

Hardware components:

- SRS FEC: general SRS component → ✔
- Hybrid: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), industrial test production started with 20 v4 (VMM3a) → ✔
- Adapter Card: 3 prototypes, final version design →
Implementation of the VMM ASIC in SRS

Status

Hardware components:
- SRS FEC: general SRS component → ✔
- Hybrid: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), industrial test production started with 20 v4 (VMM3a) → ✔
- Adapter Card: 3 prototypes, final version design → 

Firmware:
- SRS FEC: basics working, improvements → ✔
- Hybrid: basics working, improvements → ✔
Implementation of the VMM ASIC in SRS

Status

Hardware components:
- SRS FEC: general SRS component → ✔
- Hybrid: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), industrial test production started with 20 v4 (VMM3a) → ✔
- Adapter Card: 3 prototypes, final version design → 

Firmware:
- SRS FEC: basics working, improvements → ✔
- Hybrid: basics working, improvements → ✔

Software:
- Slow control, online monitoring, DAQ working → ✔
- Redesign into VMM DAQ ongoing with CERN EP-DT-DI →
Implementation of the VMM ASIC in SRS

Status

Hardware components:
- SRS FEC: general SRS component \(\rightarrow \checkmark\)
- Hybrid: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), industrial test production started with 20 v4 (VMM3a) \(\rightarrow \checkmark\)
- Adapter Card: 3 prototypes, final version design \(\rightarrow \)

Firmware:
- SRS FEC: basics working, improvements \(\rightarrow \checkmark\)
- Hybrid: basics working, improvements \(\rightarrow \checkmark\)

Software:
- Slow control, online monitoring, DAQ working \(\rightarrow \checkmark\)
- Redesign into VMM DAQ ongoing with CERN EP-DT-DI

Integration
- Single FEC (4 hybrids) used at many test beams \(\rightarrow \checkmark\)
- Multi-FEC systems not tested \(\rightarrow \)
Implementation of the VMM ASIC in SRS

Test beams

August 2017 (SPS): 3 VMM3 hybrids

October 2017 (SPS): 4 VMM3 hybrids

July 2018 (Neutrons@Wigner): 3 VMM3 + 1 VMM3a hybrids

August 2018 (SPS): 3 VMM3 + 1 VMM3a hybrids, GBAR proto
Implementation of the VMM ASIC in SRS

Test beams

August 2017 (SPS): 3 VMM3 hybrids

October 2017 (SPS): 4 VMM3 hybrids

August 2018 (SPS): 3 VMM3 + 1 VMM3a hybrids, GBAR proto

July 2018 (Neutrons@Wigner): 3 VMM3 + 1 VMM3a hybrids

Cadmium mask, 1 mm holes

Reconstructed neutron hits

Cadmium mask, 1 mm holes, normalized, time corrected

## Future SRS VMM users

<table>
<thead>
<tr>
<th>Group</th>
<th>Application</th>
<th>VMM hybrids</th>
<th>Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESS Lund / BrightnESS</td>
<td>NMX instrument @ ESS</td>
<td>164</td>
<td>Dorothea PFEIFFER</td>
</tr>
<tr>
<td>University of Science and Technology of China</td>
<td>RICH R&amp;D for future colliders in China (CEPC and STCF)</td>
<td>156</td>
<td>LUI Jianbei</td>
</tr>
<tr>
<td>Bonn University</td>
<td>BASTARD neutron detector</td>
<td>71</td>
<td>Jochen KAMINSKI Markus KÖHLI</td>
</tr>
<tr>
<td>Mainz University</td>
<td>MAGIX experiment @ MESA*</td>
<td>211</td>
<td>Stefano CAIAZZA</td>
</tr>
<tr>
<td>Budker Institute of Nuclear Physics, Novosibirsk</td>
<td>μWell MPGD R&amp;D</td>
<td>22</td>
<td>Lev I. SHEKHTMAN</td>
</tr>
<tr>
<td>INFN Tieste</td>
<td>Generic R&amp;D</td>
<td>10</td>
<td>Silvia DALLA TORRE</td>
</tr>
<tr>
<td>Tsukuba University</td>
<td>ALICE FoCal, Si Pads</td>
<td>50</td>
<td>CHUJO Tatsuya</td>
</tr>
<tr>
<td>GDD group CERN</td>
<td>Generic R&amp;D</td>
<td>16</td>
<td>Eraldo OLIVERI</td>
</tr>
<tr>
<td>Peking University</td>
<td>CMS GEM upgrade</td>
<td>52</td>
<td>Dayong WANG</td>
</tr>
<tr>
<td>LMU Munich</td>
<td>Ion Tomography with Micromegas</td>
<td>16</td>
<td>Felix KLITZNER</td>
</tr>
<tr>
<td>LMU Munich</td>
<td>Medical physics with MPGDs, Si</td>
<td>48</td>
<td>Jona BORTFELDT</td>
</tr>
<tr>
<td>ETH Zurich</td>
<td>GBAR experiment @ CERN</td>
<td>≈40</td>
<td>Gianluca JANKA</td>
</tr>
<tr>
<td>CERN</td>
<td>BGV(Beam Gas Vertex) beam monitor*</td>
<td>200</td>
<td>Robert KIEFFER</td>
</tr>
<tr>
<td>University of Virginia, Charlottesville</td>
<td>EIC tracker @ RHIC*</td>
<td>Not known yet</td>
<td>Kondo GNANVO</td>
</tr>
</tbody>
</table>

*: not yet approved
Conclusion

- VMM ASIC has been implemented in the Scalable Readout System within the BrightnESS project, outcome is a prototype
- VMM was correct choice due to flexible configuration
- The system will become the new workhorse within the MPGD community and beyond and replace APV25-based version
- Upcoming R&D projects and experiments rely on the system
  → highest priority: provide hardware
  → train users with current software and firmware
  → collaborate with experiments
- Secure continuation of developments
(personal) Ideas for the future
What will/should happen in the next years

SRS claims to be a multi-purpose readout system, implementation of VMM was/is big step forward:

- SRS VMM will replace SRS APV and become THE readout option in RD51 and projects even outside our collaboration and other research fields.
- System needs to be further developed to fully exploit the capabilities of the VMM and current SRS hardware.
- SRS users and developer groups must continuously improve the system such that it can be operated reliably in the lab and at experiments.
- Supply with hardware, firmware, software, training and know how must be organised.

⇒ more and more users (also running experiments or such in the design phase) will join

BUT: System and current ASIC implementations have drawbacks

- Application in harsh environments (radiation, magnetic field)
- Output bandwidth of FEC (limited to 1 GbE ⇐ up to 800 Mb/s/VMM)
- FPGA capabilities on FEC (XC6VLX130T, limited transceiver speed)
- Links to front-end (usually HDMI cables, limited bandwidth, frequency)

⇒ Hardware upgrade of FEC (from 2013) and other front-end ASICs and links needed for wider range of application and modern (streaming) readout.
(personal) Ideas for the future
What will/should happen in the next years (continued)

Implement new ASICs in SRS
- VMM implementation most advance (BrightnESS and AIDA2020)
- Timepix3 and GEMROC ongoing (AIDA2020)
- future candidates: SAMPA, a radiation hard ASIC of the SiPixel community

Upgrade of SRS core hardware (FEC)
Learn from state-of-the-art and ongoing developments in HEP (like CaRIBOu, FELIX, PCIe40, USBpix, SPIDR, RCE…) ⇒ design new FEC. Current ideas:
- Go from pure FPGA to System on Chip
- Significantly improve output bandwidth to handle data from larger system (streaming readout) and cope with high data rates of VMM (up to 800 Mb/s/VMM) and recent ASICs in general (e.g. Timepix3: 5.12 Gb/s), optimum would be 100 Gb/s Ethernet output
- FEC PCB layout for lpGBT/VL+ links and latest PCIe standard to implement radiation hard and high bandwidth ASICs
The End

Thanks for your attention
SRS APV

Maximum trigger rate with special firmware: 5 kHz

(K. Gnanvo @ RD51 Collaboration Meeting Aveiro 2016)
SRS Beetle

Common project with ATLAS NSW before VMM was available

Project had to be stopped

- ACTEL FPGA proposed for radiation hardness – could not be verified
- Company could not deliver hybrids due to problems with four row wire bonding
SRS VFAT

RD51 VFAT hybrid

Not successful:

- too much noise
- wrong information from designers

→ abandoned

But...
SRS VFAT

TOTEM DAQ upgrade

VME based electronics in LHC phase 1
for VFAT opto carrier board

SRS for phase 2:

• trigger rate 1 kHz → 24 kHz
• Zero suppression
• L2 hardware algorithms in FEC

SRS Timepix

Implementation in framework of feasibility study for a pixel-TPC at ILC → InGrid/GridPix readout

SRS SiPM

NEXT readout system

SRS in ATCA, upgrade for next White detector