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The VMM front-end integration in the Scalable Readout System: On the way to a next generation readout system for generic detector R&D and experiment instrumentation

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The Scalable Readout System (SRS) of the RD51 collaboration with the APV25 ASIC is driving R&D for gaseous detectors. Discontinuation of APV25 and demands on flexibility concerning e.g. detector capacitance and readout rate induced a replacement of the ASIC, for which the collaboration has chosen the VMM chip of the ATLAS New Small Wheel upgrade.

A prototype SRS VMM system was operated with small GEM detectors at test beams and hardware components are finalised. More than twelve groups signed as primary system users.

The readout chain and implementation of the VMM in SRS is outlined with applications and further developments.

Summary

Since 2010, when the RD51 collaboration introduced the Scalable Readout System (SRS) as a versatile and multi-purpose device, different front-end ASICs have been integrated as the Timepix, VFAT and the most commonly used the APV25. The architecture of the SRS simplifies the implementation of different chips due to a common hardware part. Only the on-detector electronics and an adapter card require redesign.

For R&D on micro-pattern gaseous detectors, the SRS became a standard and found its application in other fields of research like muon tomography. The APV25 front-end implementation plays a significant role for research on gaseous detectors with strip readout as for example R&D and quality control for the ATLAS New Small Wheel (NSW) or CMS GEM upgrade projects. Due to the scalability, table-top systems for small test detectors as well as large readouts for complete wheel panels with several 10000 channels are realised.

However, the APV25 designed for the CMS silicon strip detector in 2001 has drawbacks and will not be produced any longer. It has a fixed gain and shaping time and can only be used for detectors with a capacitance of up to 50 pF per channel.

To overcome these limitations and provide the community an improved continuation of SRS readout, the RD51 collaboration decided to implement the VMM ASIC developed in the scope of the ATLAS NSW upgrade in the SRS. This development is carried out in the framework of an Horizon2020 project related to the European Spallation Source, where one of the instrument prototypes and its readout is developed at CERN. It is also supported by AIDA2020.

In the past two years, FPGA firmware for the general-purpose SRS Front-End Concentrator (FEC) card has been developed. On the hardware side, on-detector circuit boards for the VMM as well as adapter cards to the FEC were designed, build in several iterations, tested and are now finalised. Slow control, data acquisition and online monitoring software are developed in collaboration with the ESS Data Management and Software Center to provide users a complete and ready to use package.

A prototype SRS-VMM system is operational and has been tested in several test beams at CERNs SPS and a neutron facility in Norway. Currently, the final hardware design is being fixed, such that first system will be provided to the community within the coming months. More than 12 groups of different fields have signed

as primary users for testing and supporting the developments. They will apply the system to generic detector R&D as well as medical science, neutron scattering, cosmic ray detection and fundamental physics research. The SRS with VMM will take over from the successful APV25 implementation and is expected to play a significant role in the next decade of detector R&D, but will also find its application in operational physics experiments.

The presentation will focus on the implementation of the VMM in the SRS with related hardware, firmware and software followed by an overview of its application and plans for further upgrades of the system.

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