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Design and status of custom-designed ASICs for the Phase-I upgrade of the ATLAS muon spectrometer

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The New Small Wheel (NSW) is an upgrade for enhanced triggering and reconstruction of muons in the forward region of the ATLAS detector at CERN's LHC. The NSW will compose two detector technologies: Micromegas (MM) and small-strip Thin Gap Chamber (sTGC). Both detectors will be used for muon triggering at the first-level trigger and for precision tracking. Four custom-designed ASICs are needed: one to amplify/shape/discriminate raw detector signals, two to handle the trigger signals from MM and sTGC separately, and the fourth one to readout precision data. We will present the design and current status of all ASIC prototypes.

Summary

The NSW frontend electronics include four custom-designed ASICs. For both MM and sTGC, the raw detector signal is first amplified, shaped and discriminated by a custom VMM ASIC. This ASIC has a silicon area of about 130 mm2 and can provide both precision (10-bit) amplitude and timing (20-bit) measurements for 64 channels after Level-1 Accept. In addition, it also provides a serial out 6-bit address serial out of the first signal occurred used for the MM trigger, and parallel prompt outputs with a 6-bit ADC of the signal amplitude measurement for the sTGC trigger. An Address in Real Time (ART) ASIC encodes up to eight addresses of MM channels with the earliest arriving hits from up to 32 VMMs and transmits them synchronously to the MM trigger processor. A Trigger Data Serializer (TDC) ASIC prepares the sTGC trigger data for both strips and pads, performs pad-strip matching, and serializes the strip charge data to the router board on the rim of the NSW. The router board removes null packets and sends useful data to the sTGC trigger processor via optical fibers. A fourth ASIC called Readout Controller (RoC) stores both timing and charge information in the buffer until it receives the Level-1 Accept. The Level-1 data will transmit from multiple front-end boards to a network called Front End LInk eXchange (FELIX) through a custom aggregator GBTx board called L1 Data Drive Card (L1DDC). GBT and SCA ASICs developed at CERN are also used for the data transmission and system configuration. We will present the design and the current status of all ASIC prototypes.

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