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TUTORIAL: Bits on Speed! –SERDES Design in Advanced CMOS Technologies

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Miromico AG has been developing high-performance I/O's in CMOS technologies for almost 15 years. The application span includes various chip-to-chip communication links, where the ICs are either sitting on the same PCB (C2C) or on different PCBs connected through a backplane (BP).

With the exponential growth of on-chip functionality and high cost of IC pads and interconnections, parallel data exchange is no longer an option for most applications and has been systematically replaced by High Speed Serial (HSS) links. The improvement of Si-technologies, bringing along an ever increasing rate of core processing clocks, continuously sets new targets in terms of I/O bandwidth. New industry standard are being defined at the 32, 56 and 112 Gbps/pad data rates, in order to accommodate the increasing demands of cloud computing and modern data centers.

Design challenges on analog side include the fact that further scaling in IC technologies is no longer accompanied by large gains in intrinsic device speed, so that performance improvement must also come from innovative system design and direct collaboration with technology developers. Furthermore and especially for BP applications, the channel response at the frequencies of interest is typically introducing significant losses and reflections that must be compensated in order to maintain the signal integrity. Adaptive signal equalization, in the continuous- and/or discrete-time domains, becomes a vital integral function in the design of modern I/Os.

The objective of this tutorial is to give a brief overview, spanning from industry trends and marketing requirements down to system solutions and specific analog functions. The focus will be on Physical Layer and full-custom analog/mixed-signal design techniques.

Summary

Author: GIOVANNI, Cervelli (Miromico, Switzerland)

Presenters: GIOVANNI, Cervelli (Miromico, Switzerland); GARDELLINI, D. (Miromico, Switzerland)

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