

# Design and tests VCSEL Array Drivers in 65nm-CMOS for HEP Applications

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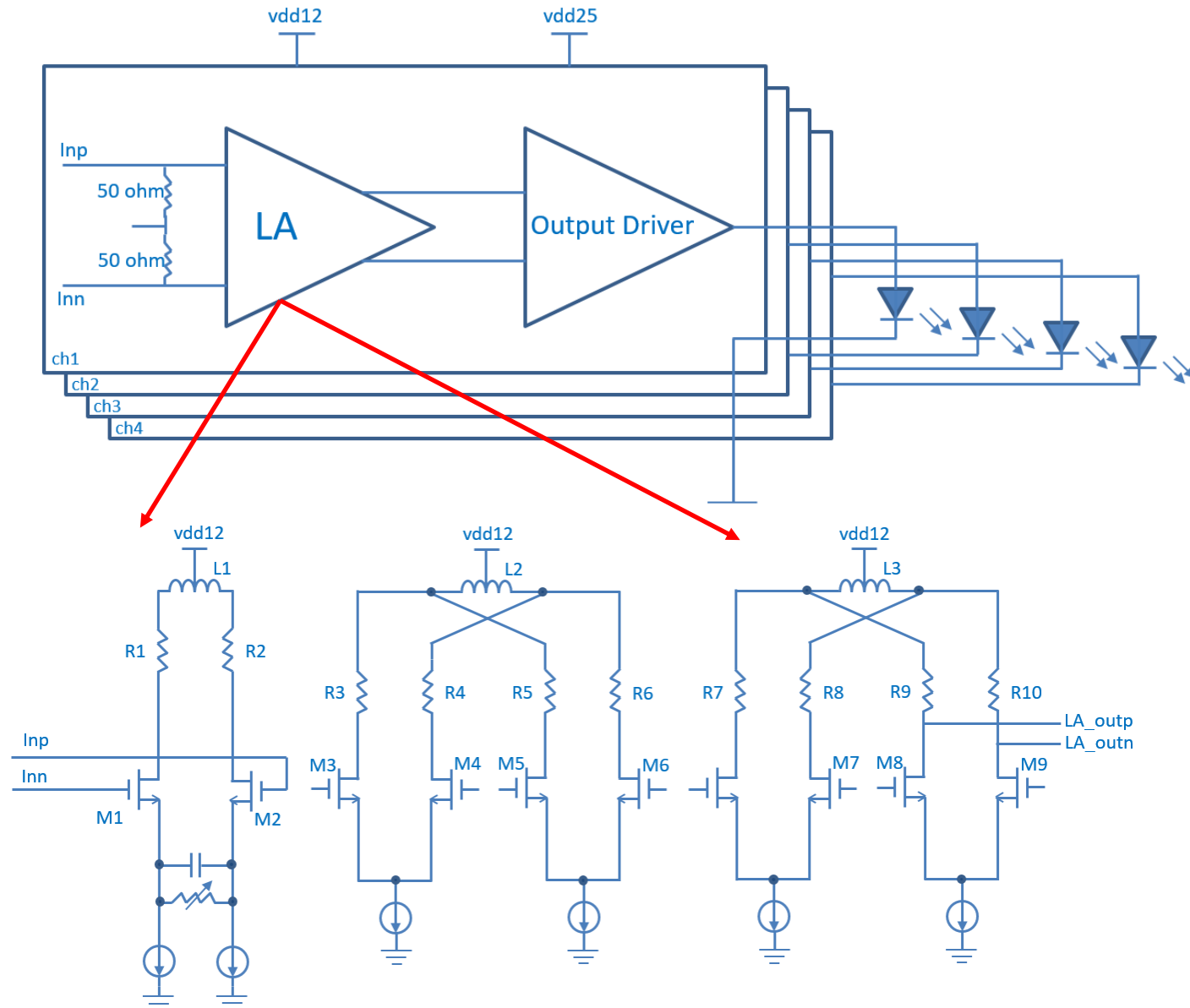
# Content

- Introduction and motivation of the work
- The designs of the 4x14 and 4x28 Gbps VCSEL array drivers
- The measurement results so far
- Summary and next steps

# What we wanted to achieve with these designs

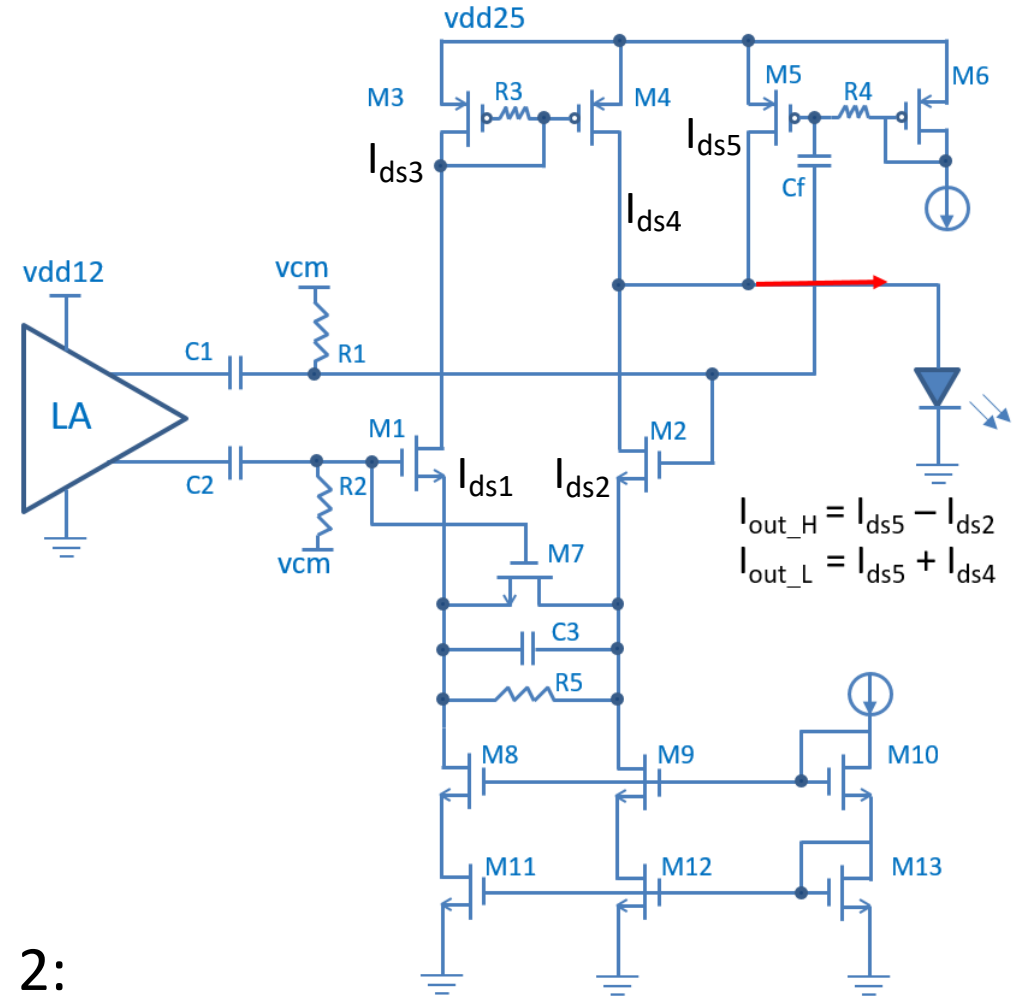
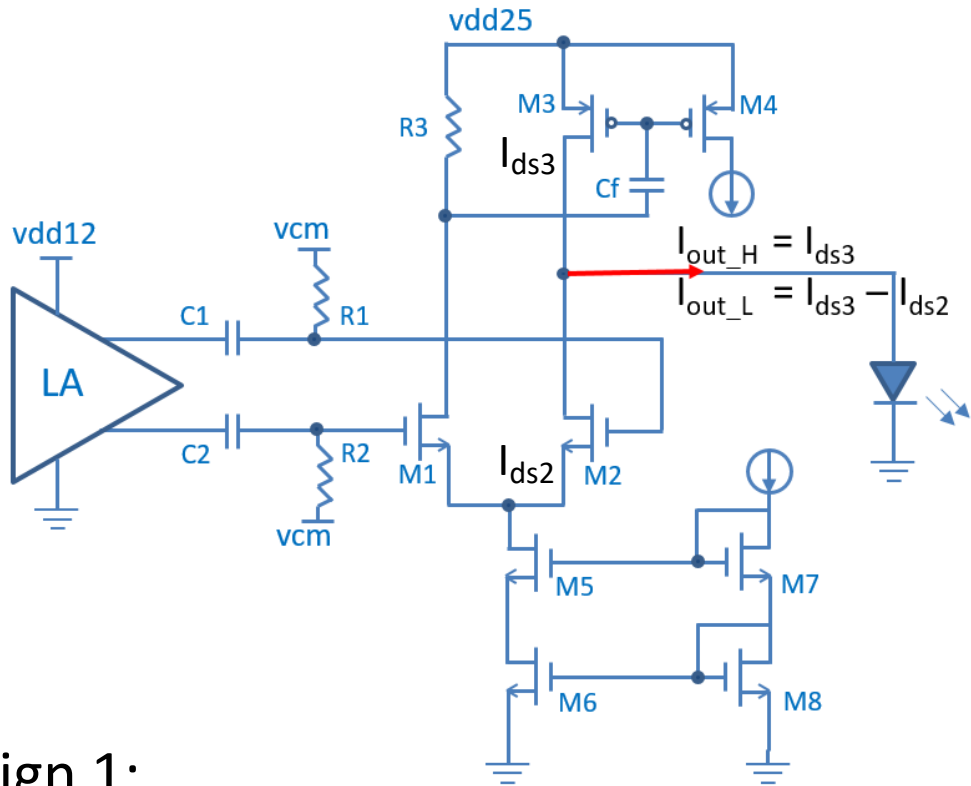
- ❑ In the current LHC experiments optical links that read out the detector front-end electronics operate up to 1.6 Gbps per fiber (example: ATLAS LAr FEB link)
- ❑ This changes to about 5 Gbps per fiber for the phase-1 upgrades.
- ❑ IpGBT and the optical modules from VL+ will deliver a speed up to 10.24 Gbps per fiber, and mainly for phase-2 upgrades.
- ❑ But higher speeds are common in industry (example: the FPGAs we use for the link receiving end and the back-end electronics), and should we adhere to industrial standards (QSFP14 and 28)?
- ❑ Based on this thinking, we R&D-ed three designs of 4-channel VcseL Array Driver (VLAD): two at 14 Gbps per channel and one at 28 Gbps per channel. The design work was in a collaboration with CERN.

# A few highlights in the design

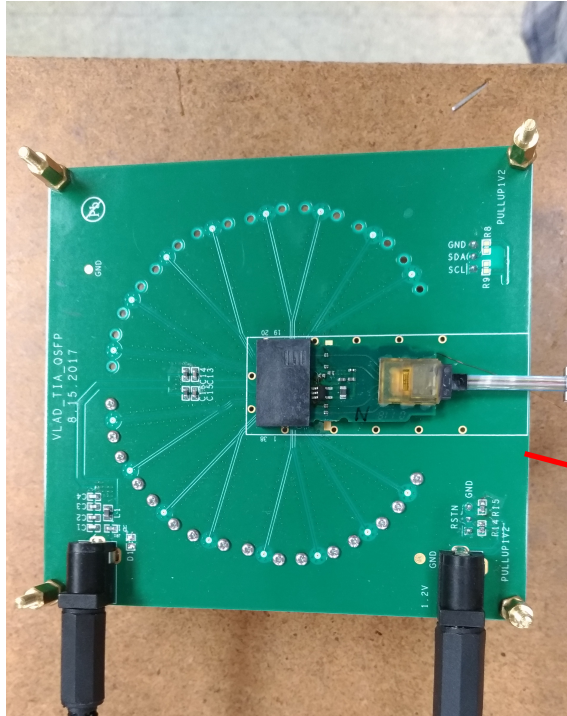


- The drivers have the same structure of a Limiting-Amplifier and an Output-Driver.
- The LA has three stages. Stage1 uses CTLE as the adjustable equalization, and a passive inductance is included to optimize the peaking frequency. Stage2 and Stage3 both employ shared inductors to boost the bandwidth.
- VLAD14 has two designs for its Output-Driver: one emphasizes on speed and one balances on power consumption. Both share the same LA.
- VLAD28 has its own LA and OD designs.

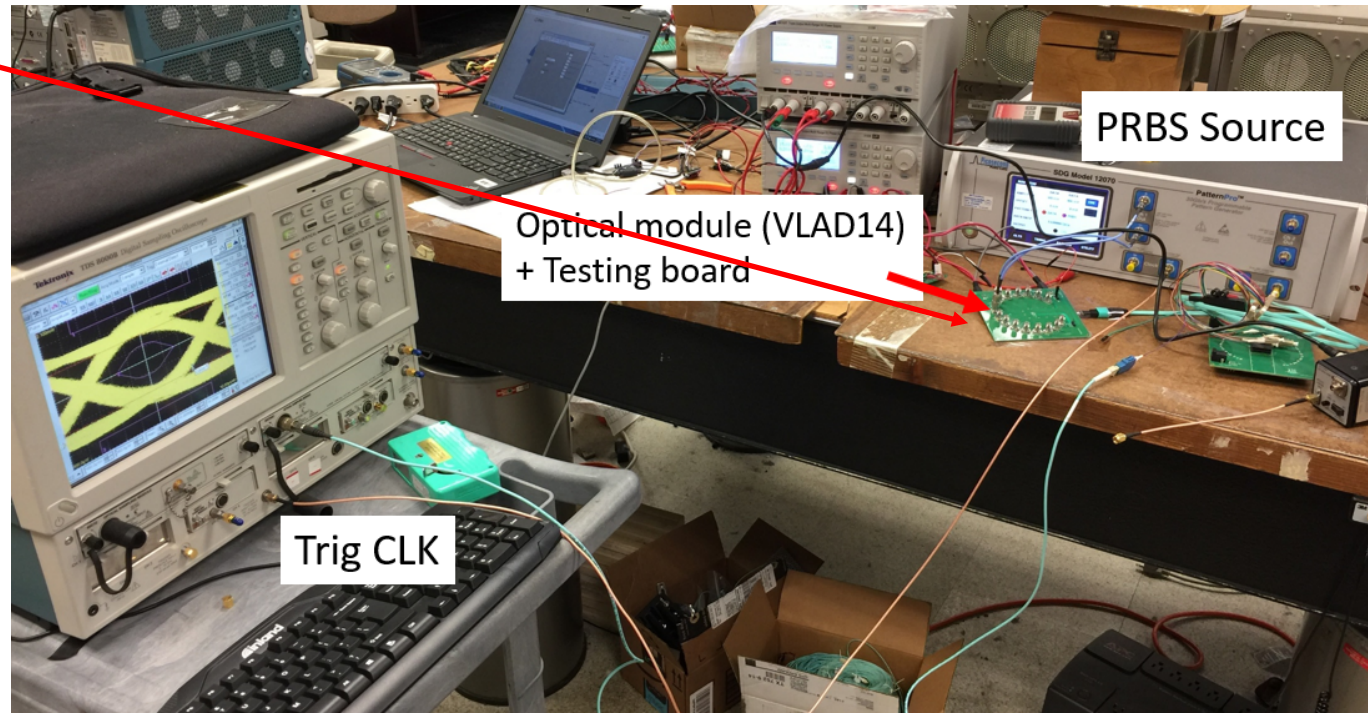
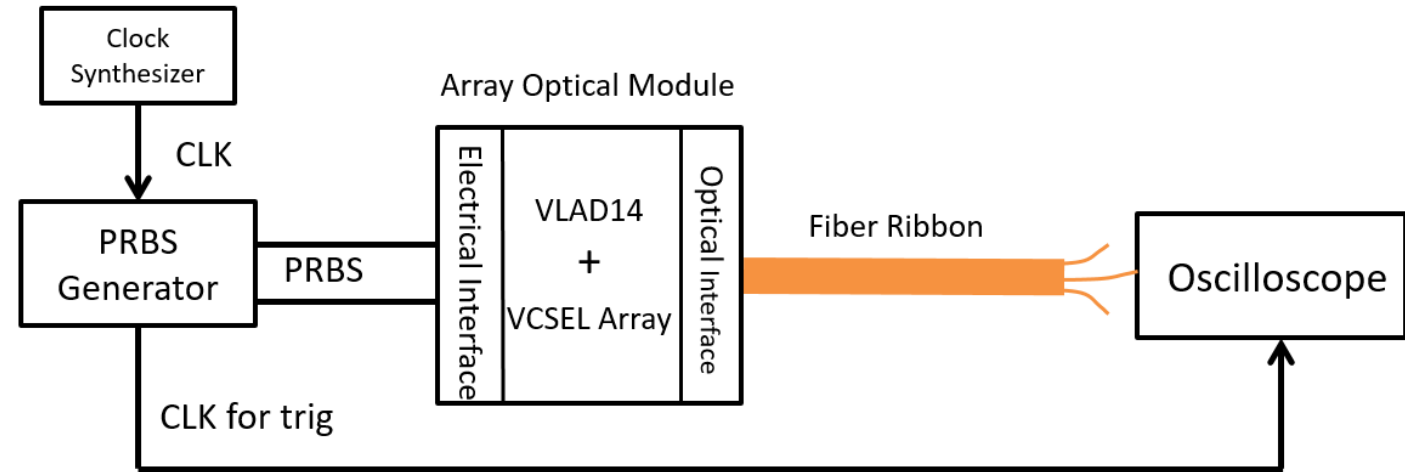
# The output-drivers



# More thorough tests of VLAD14 since TWEPP2017



A QSFP optical-engine like carrier board is developed and used as test vehicle.



# Typical eye diagrams at 14 Gbps

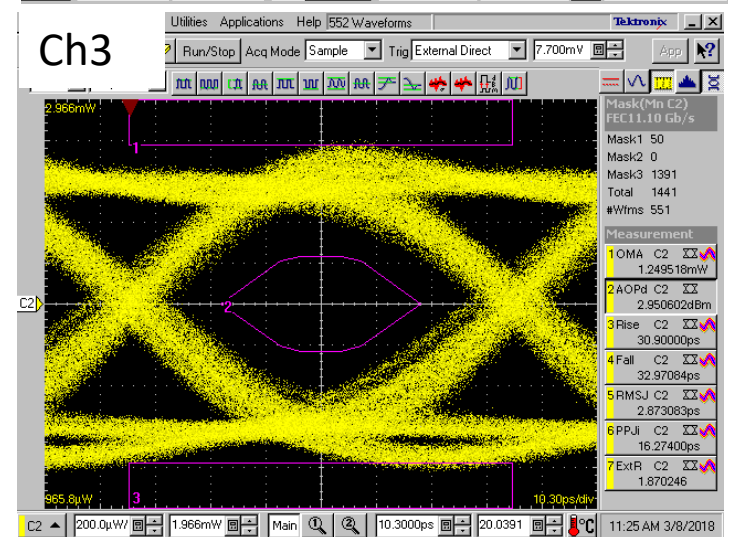
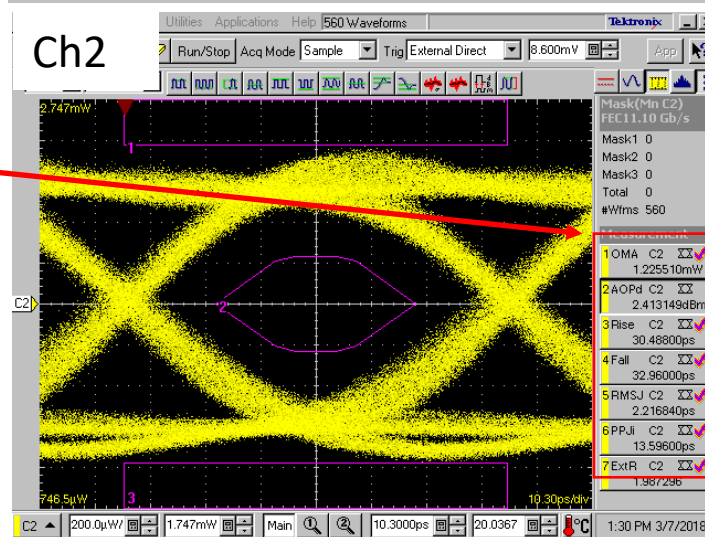
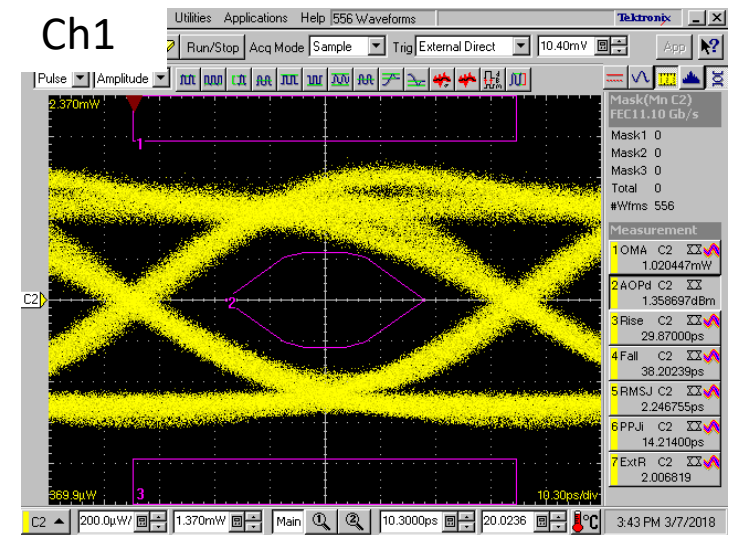
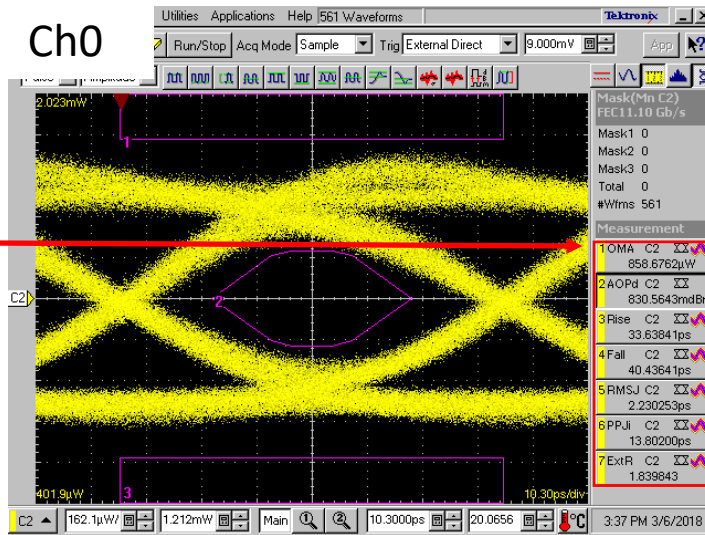
Design 1: Ch0 and Ch1  
Design 2: Ch2 and Ch3

## Performance

OMA 0.86 mW  
AOP 0.83 dBm  
Rise time 33.6 ps  
Fall time 40.4 ps  
Jitter (RMS) 2.2 ps

## Performance

OMA 1.23 mW  
AOP 2.41 dBm  
Rise time 30.5 ps  
Fall time 33.0 ps  
Jitter (RMS) 2.2 ps



**Power dissipation 198 mA @ 3.3V or 653 mW for the whole chip.**  
(with on-board 3.3V to 1.2V and 2.5 V regulators PAM2305)

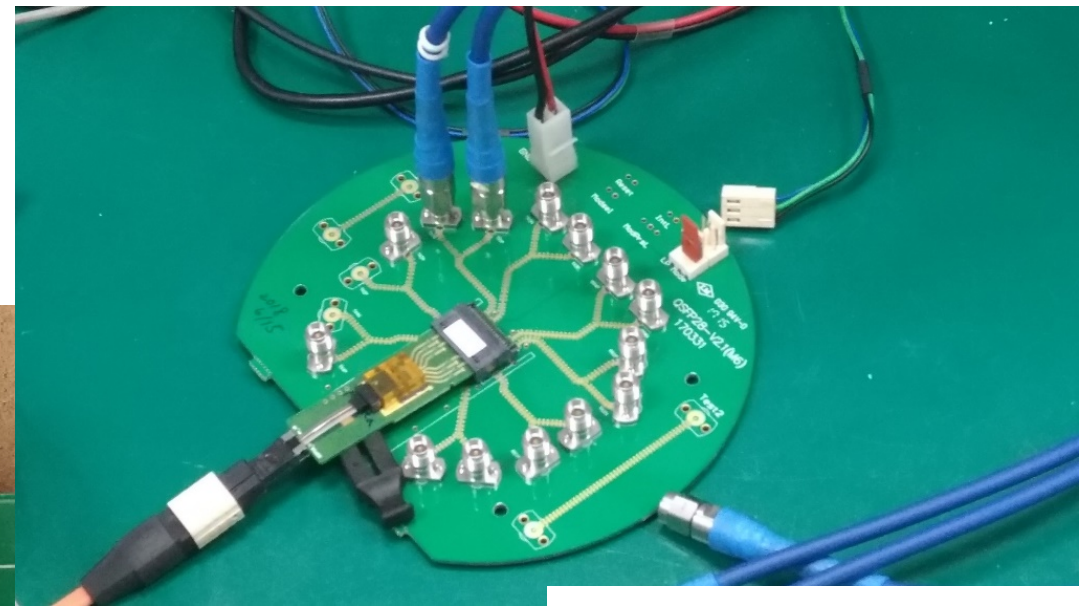
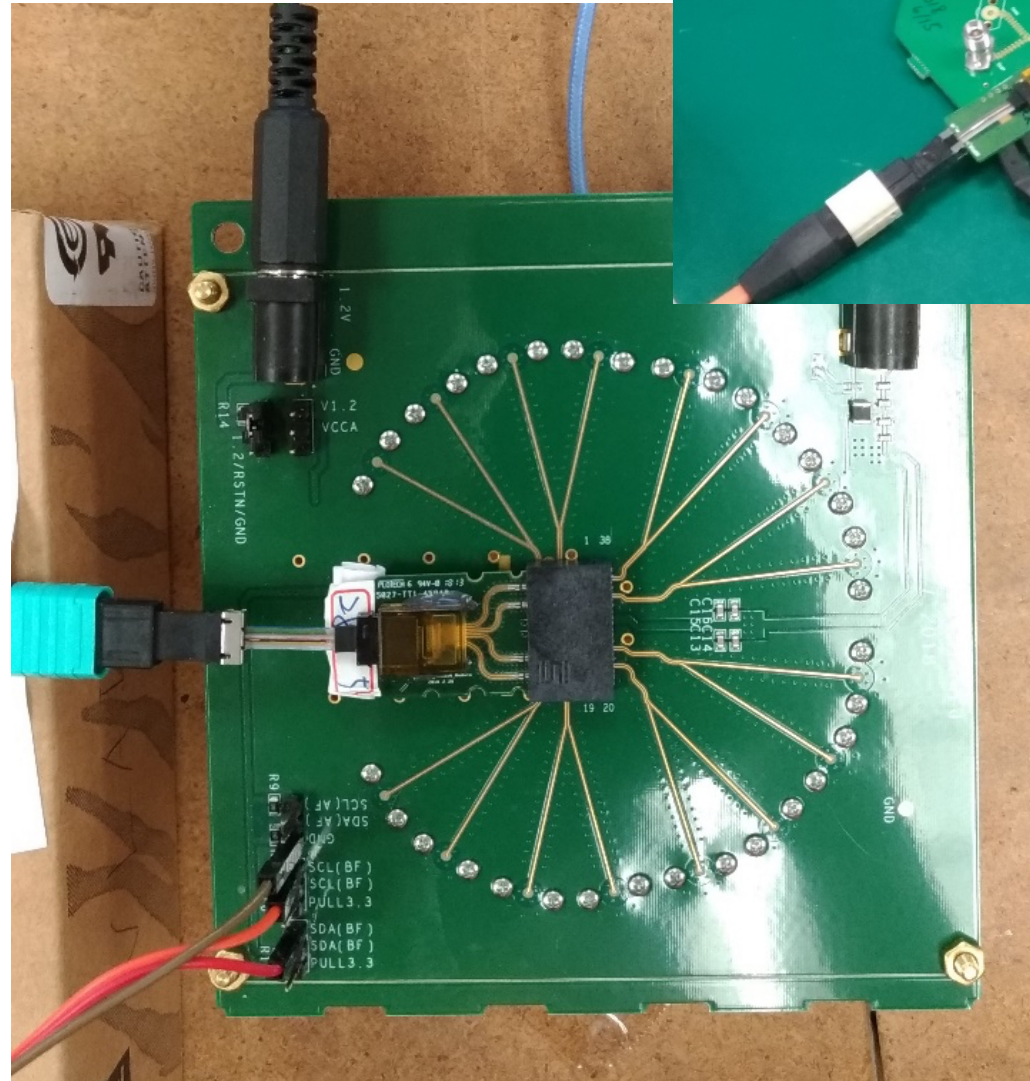
# Test setup for VLAD28



We again use QSFP optical engine as the test vehicle.

Signal source:  
Anritsu, MP1800A, PRBS 2<sup>31</sup>-1

Oscilloscope: Keysight DCA-X  
86100D



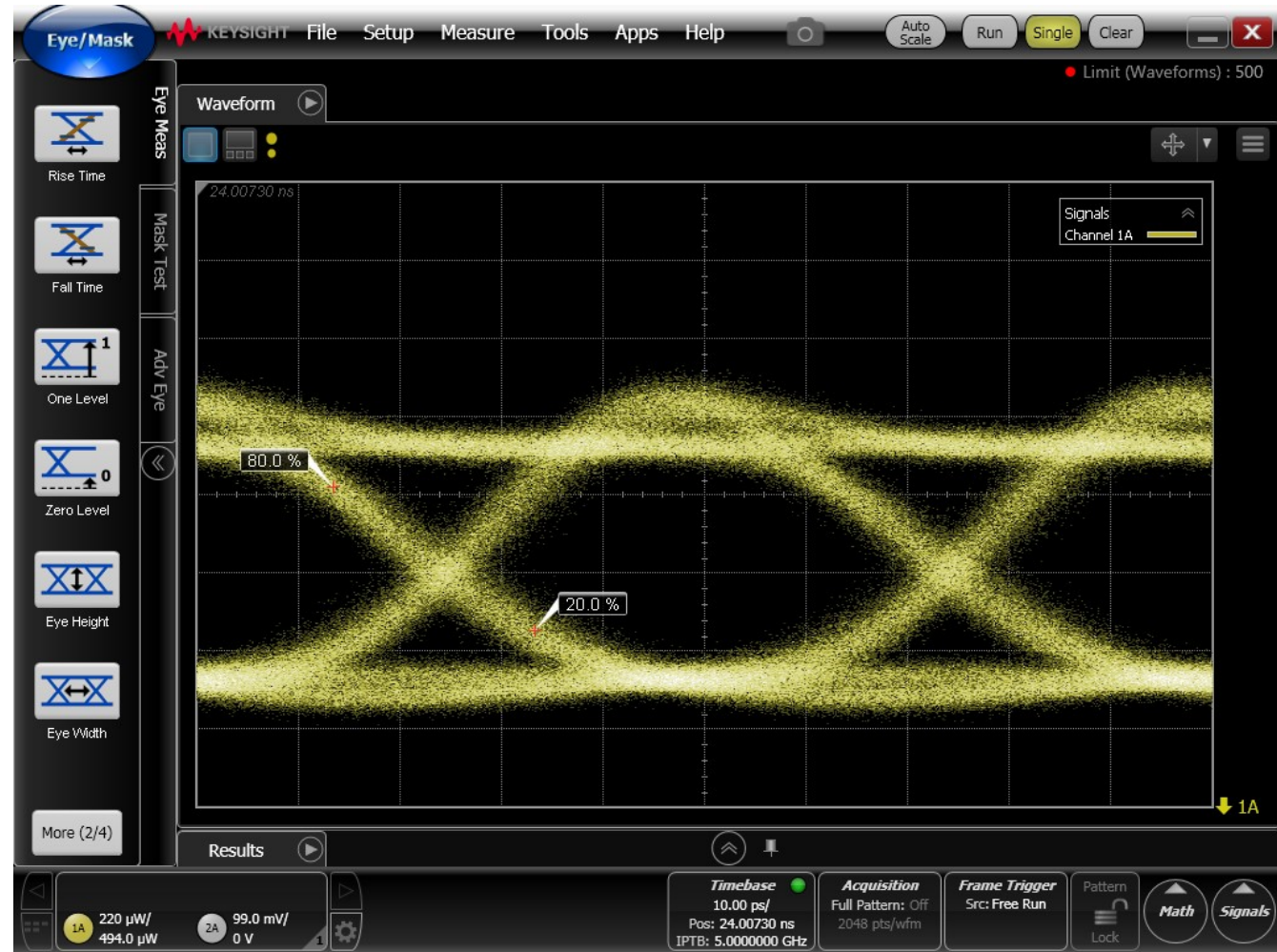
Compare: Commercial  
test board and module



# VLAD28: a typical eye diagram at 20 Gbps

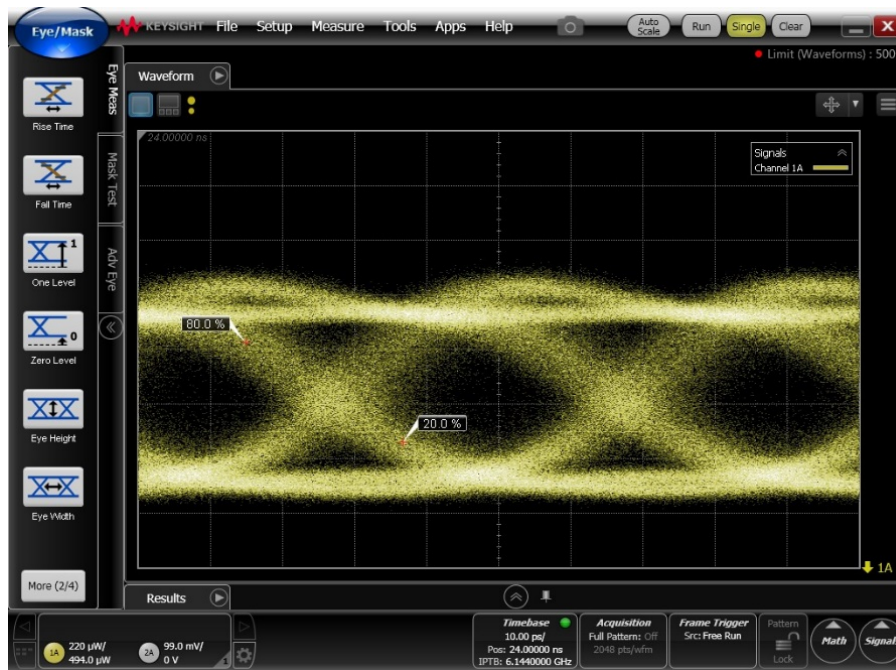
Rise time: 16.4 ps  
Fall time: 19.9 ps  
Jitter (p-p): 15.3 ps  
AOP: -1.3 dBm  
Ext. ratio: 4.3 dB

Power:  
251 mA @ 3.3V (with on-board regulators) or 828 mW (all 4 channels on)



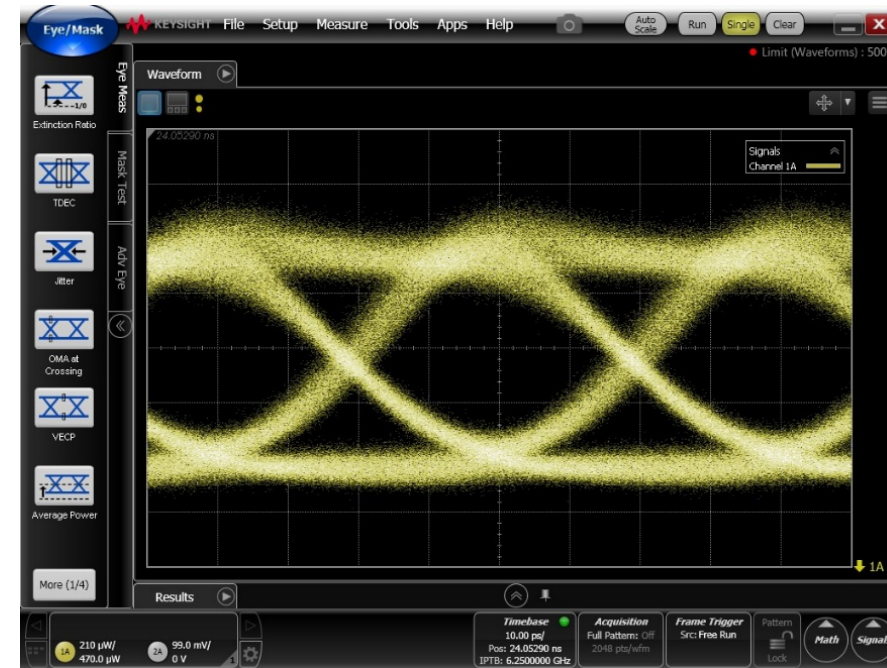
# Compare with commercial modules @ 25 Gbps

## VLAD28



Rise time	17.2 ps
Fall time	21.7 ps
Jitter (p-p)	39.9 ps

## COTS



Rise time	16.0 ps
Fall time	20.3 ps
Jitter (p-p)	11.1 ps

We suspect that the bandwidth limitation on the eye of VLAD28 @ 25 Gbps comes from the test system. We are re-designing the test boards to address this issue.

# Summary and next steps

- ❑ Both designs in VLAD14 test up to 14 Gbps per channel. Design 2 seems to be better than design 1.
- ❑ VLAD28 tests up to 20 Gbps so far. We suspect that the bandwidth limitation is in the test board and are re-designing the test board.
- ❑ More evaluations, including in radiation, will follow.

Backup slide

# Crosstalk: VLAD14

Monitor Ch1  
Input: open  
All other channels are ON  
Channel 2 input 250 mV

