Contribution ID: **135** Type: **Oral**

Two Designs of 4 × 14-Gbps VCSEL Array Driver in 65 nm CMOS for HEP Applications

Tuesday, 18 September 2018 09:50 (25 minutes)

We present designs and test results of a radiation-tolerant VCSEL array driver ASIC (VLAD14) fabricated in 65 nm CMOS technology. VLAD14 is a 4 × 14-Gbps driver with two designs implemented in four channels, delivers 2 mA bias and 5 mA modulation currents at 44 mW/ch and 52 mW/ch, respectively. Two designs have respective innovative structures at the output stage for high-speed and low-power operations. Widely-open optical eye diagrams at 14 Gbps have been captured for both two designs. Full channel optical test and radiation test will be carried out and reported at the workshop.

Summary

VCSEL-based, high-speed, low-power, radiation-tolerant short-range optical data links are in high demand for detector data transmission in the LHC upgrades as well as in other physics detector developments. VCSEL array driver ASICs are the key components in the optical links. Based on our continuous research on VCSEL array driver ASIC designs, we here report two 14 Gbps/ch VCSEL array driver ASIC designs in a 4 x 14-Gbps/ch VCSEL array driver (VLAD14). Both two designs have been tested and wide-open 14 Gbps optical eye diagrams have been captured. Further full link test and radiation test will be conducted and reported at the workshop.

VLAD14 has four independent channels, and two designs are implemented in channel 1-2 and channel 3-4, respectively. The driver die features a size of 2000 μm × 1230 μm, and the channel height is 250 μm to be compatible with the VCSEL array die. Both two designs receive 200 mVp-p differential CML signals as default inputs, and outputs a 2 mA bias current and a 5 mA modulation current at 14 Gbps/ch with the power consumption of 44 mW/ch and 52 mW/ch, respectively.

The analog core of each channel consists of the limiting amplifier (LA) and the output driver (2.5 V). Two designs have the same LA design, which consists of an equalizer stage (1.2 V) and a four-stage pre-driver (1.2 V). The equalizer stage uses CTLE structure with a 3-bit configurable RC degeneration to provide appropriate frequency peaking to compensates the high-frequency loss in PCB traces and bonding wires. The four-stage pre-driver adopts the shared inductor structure to enable peaking in four stages by using two inductors.

Two designs have different output structures. One design adopts the on-chip AC-coupling between the pre-driver and the output driver to increase the DC voltage, and a stacked tail-current source is used in the output driver to also increase the DC operation point. Hence, the cascode NMOS, used for the voltage drop at the output branch to sustain the output DC voltage to 1.8 V (due to the VCSEL forward voltage), can be removed from the design. The bandwidth is then effectively improved by the reduction of the output capacitance and elimination of the cut-off recovery from that cascode NMOS.

Another design also adopts the on-chip AC-coupling to raise the DC operation point and remove the voltage-drop MOS. Besides, a novel PMOS current mirror is designed as the load of the differential MOS at the output driver without the bandwidth degradation. The modulated current at the other branch now can also contribute to the output branch. The output modulation current can be –Imod ˜ Imod comparing to the 0 ˜ Imod in the regular design. The modulation efficiency is improved from the structure level.

VLAD14 design has been taped out, and both designs within VLAD14 have already been tested. Widely-open 14 Gbps optical eyes have been captured. Further full channel optical test and radiation test will be carried

out and the results will be reported.

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Session Classification: ASIC

Track Classification: ASIC