Presentation Summary

Main packaging challenges for High Energy Physics applications
- High-tech substrates or interposer
- Hybrid packaging technologies (Mix-technologies)
- Die targets: advanced die preparation
- Die placement challenges
- Power management considerations

Advanced Packaging Technologies overview
- Advanced technologies dedicated to die preparation
  (Bumping, thinning, optional post thinning operations, dicing)
- High-tech Substrates and Interposers
- High precision die placement and underfilling
Main Packaging Challenges for High Energy Physics Applications
Main Packaging Challenges for High Energy Physics Applications

High-tech substrates or interposer
- Pad pitch & spacing (50µm down to 40µm)
- High i/o’s density (17/mm² to 25/mm²)
- Up to 4-layers for routing (Buried and blind µvia technologies)
- Staggered wire bonding pads for 2nd level interconnection (Next?)
- Ultra-thin, ultra-light weight, ultra-low radius folding (Interposer?)
- Strong polymer materials (Mechanical and electrical behavior)

Hybrid packaging technologies (Mix-technologies)
- Standard Surface Mount Technologies (SMT, bi- to tri-step stencil)
- Flip-Chip (Precision placement)
- Undefilling (µgr polymer precision jetting)
- Specific connectors (SMT)
- Local hardeners / stiffeners / heaters (High-precision assembly)
- Partial coating (HV protection)
- Folding and placement (Low-radius, high-precision stacking)
Main Packaging Challenges for High Energy Physics Applications

Die targets: advanced die preparation
- Ultra low profile (Weight) – 50µm and below
- Ready for flip-chip interconnection (Thinning of bumped wafers)
- Bumping targets (Materials, pitch, diameter and density, height, bump-to-bump planarity)

Die placement challenges
- Spacing between detection die to die down to 150µm then 80µm (Placement accuracy < 3µm - detectors or opt couplers die)
- Die ultra-low pitch and high density interconnections (Equipment, tool management and thermal processes)
- Flip-chip technologies to target the micron (Equipment, substrate)
- Underfilling with high precision volume (µgr) – jetting

All of these challenges are discussed in term of technology drivers, development, availability and TRL, cost & reliability considerations.
Main Packaging Challenges for High Energy Physics Applications

Power management considerations
- Low Rd MOSFET transistor, low Qt and HV option (GaN / SiC)
- Back side metallization on low profile power die (Taiko, selective back side metal)
- Weight & space reduction: direct die soldering on substrate
- Power die soldering @ voids 3%: vacuum & vapor phase furnace
- Silver Sintering technologies for high Temp usage and reliability
- Substrate technologies (Power drains, power vias, high °C/mW)
Advanced Packaging Technologies Overview
Ultra Low Profile Wafer Thinning

Ultra Low Profile Bumped Wafer Thinning

Thinning – Dicing Combination

Stress less Dicing Technologies
Wafer thinning & dicing regular flow

Conventional Process for Wafer thinning (2 wheels) and dicing (2 spindles)

- Back Grinding
  - Tape Laminating
- Back Grinding
  - Stress relief
- Dicing Tape Mounting
- Back Grinding
  - Tape Peeling
- Full Cut Dicing

Note: The bumping process option is done before the wafer thinning

Conventional process limitation below 100µm thickness:
- Handling between thinning, stress relief and dicing (Flexible wafer)
- Very difficult back-side metallization processing after stress relief (Power)
- Mechanical risks during handling and processing until dicing operation
- Cumulative mechanical stresses during wafer thinning and wafer dicing
- Tape delamination residue (Pollution, additional cleaning processes)
- Stress induced on bumps/metal during thinning and tape delamination

Several advanced processes has been developed to secure each listed risk
Thin wafer technology by DBG
Dicing Before Grinding - Disco

Advantages & Drawbacks of DBG compared to conventional process flow:
- No thin wafer handling
- No mechanical damages during handling and processes
- No thickness limitation (In practice, 50µm is industrial reachable)
- Less mechanical stresses during partial sawing and relief during thinning
- No wafer back-side process completion (Back-side metal for Power, vias last, …)
- Still same cumulative mechanical stresses during wafer thinning
- Still tape delamination residue (Pollution, additional cleaning processes)
- Still stress induced on bumps/metal during thinning & tape delamination
- Die movement with mechanical risks during final grinding (Bumps deformation)
- Specific Taping/De-taping equipment (Additional Investment)

Note: The bumping process option is done before the wafer partial sawing
Thin wafer technology by DBG

**Dicing Before Grinding - Disco**

- No backside chipping and crack issue
  - Less dicing stress. (Full cut process on the soft dicing tape gives stress to the wafer backside.)
  - Dicing stress can be removed during fine grinding.
  - Higher die strength can be achieved.

- Higher cut speed and longer blade life because:
  - Shallow grooving into Si only.
  - No cut into tape, no clogging of blade

- Easy to process very small dies because dies do not move during half cut.

- Less number of dicers are required

- No issue of wafer warpage

- High yield because of zero wafer breakage
Ultra-thin wafer technology by Taiko process from Disco

- Easier handling of thin wafer
  - Wafer support by the outer rim
    - Decreased wafer warpage
    - Improved strength

- High temperature process for thin wafer
  - No support and no adhesion
    - Easy wafer handling in the post processes
    - No temperature limit without adhesive
    - No outgas

Discrete devices
Next generation 3D devices

Less warpage and higher wafer strength
Picture: $\Phi 300$ mm, 50 $\mu$m

Unloading to the standard cassette
Ultra-thin wafer technology by Taiko process from Disco

Patented
Ultra-thin wafer technology by Taiko process from Disco

Note: The bumping process option is done before the wafer thinning process

Advantages & Drawbacks of Taiko solution compared to conventional process flow:
- **No thin wafer handling**
- Less mechanical damages during handling and processes
- No thickness limitation (In practice, 20µm is industrial reachable)
- **Wafer back-side process completion** (Back-side metal, vias last, etc…)
- Still same cumulative mechanical stresses during wafer thinning
- Still tape delamination residue (Pollution, additional cleaning processes)
  - **Note: could be combined with CONDox (See after)**
- Still stress induced on bumps/metal during thinning & tape delamination
- Still bump deformation during thinning process
- **Additional edge grinding or edge circular sawing steps** (Additional costs)
Stealth Laser Dicing

Modified layer generation by laser, then mechanical die separation

No mechanical load applied to the wafer (Laser pulse)
- Dicing without front or backside chipping (Expandable tape)
- Completely dry process

Suitable for ultra thin die (s/e form factor), high count GDW & MEMS
Stealth Laser Dicing

- Extremely thin kerf
  - Greatly contributes to street reduction by the extremely narrow kerf

- High die strength for thin wafers
  - Effective for thin wafers less than 100 µm
  - High quality and high throughput compared to blade dicing

Kerf width: 0 µm
Chipping: 0 µm

Before tape expansion

After tape expansion

Higher dicing quality with less mechanical load
Suitable for fragile MEMS structure with dicing difficulty
Laser improvement with short pulse laser – Wafer scribing before dicing

<table>
<thead>
<tr>
<th>Laser grooving process</th>
<th>Pulse width</th>
<th>Before blade dicing (Laser grooving only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Laser scribing only</td>
<td></td>
<td>Current</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Short pulse</td>
</tr>
</tbody>
</table>

Wafer: 45nm CMOS (Low-k)

Achievement

**Quality**
- Less void
- High die strength
- No delamination
- Less burr

**Shape**
- Less tapered shape
- Flat bottom
Plasma Dicing

- Damage-less dicing process
  - No mechanical damage, no chipping
  - High die strength

- Entire wafer process
  - Process street all together
  - Especially tiny die can have high UPH

- Narrow street capability
  - Possible < 10um
  - More productivity for high GDW, small kerf

0.2 x 0.2 mm die  WLCSP

- Non-straight street by mask shape
  - Rounded corner on dies
  - Polygonal dies, MPW (Multi Project Wafer) capability

Rounded corner die  MPW

Suitable for 0-stress requirement, ultra low profile die, high-count GDW, non-squared die, specific MPW, MEMS or interposer
Plasma Dicing

- Narrow saw street width (Smallest kerf width: 10μm)
- Effective for processing small die
- High die strength
- No additional mask

No metal on street: Grinding → Tape mounting → Plasma Dicing
Metal on street: Grinding → Tape mounting → Laser Grooving → Plasma Dicing

DIASCO Key Technology

Laser Grooving
Plasma Dicing
Wafer Bumping
Wafer bumping technologies

Why bumping is required
- Foot print reduction

<table>
<thead>
<tr>
<th>Die Size (mm)</th>
<th>2x2</th>
<th>3x3</th>
<th>4x4</th>
<th>5x5</th>
<th>6x6</th>
<th>8x8</th>
<th>10x10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduction (%)</td>
<td>69%</td>
<td>44%</td>
<td>32%</td>
<td>25%</td>
<td>21%</td>
<td>16%</td>
<td>12%</td>
</tr>
</tbody>
</table>

- Interconnection yield loss reduction: especially for high i/o’s devices
- Die-bonding UPH, operation cost and investment level optimization (No wire-bonders)
- Specific device with active area free of top interconnexion (LED, Sensors, MEMS, …)

Interconnection way of working:
- Wire bonding interconnexion from top die-pad to substrate to be replaced by bumps interconnection (Bumps)
- Flip-Chip operation is then required to interconnect bumps to the substrate: Wafer Level Chip Scale Package or (WL)-CSP
Wafer bumping technologies

Depending on the bumping and flipping processes, wafers needs to be adapted in term of pad size opening and/or pad location

- Bump on IO :
  Requires special bond pad design (Round shape)

- Repassivation and Resizing :
  Single layer BCB / Polyimide (PI) / Other
  Resizes bond pad + round-shape

- Redistribution and Optional Resizing
  Dual layer BCB / Polyimide (PI) / Other
  Relocates bond pad
  Resizes bond pad + round-shape
Wafer bumping technologies
Re-Distribution Layer

1. Incoming

2. Repassivation – 1st layer

3. Metal Deposition

4. Runner Patterning

5. Repassivation, UBM/Stud

6. Solder Print, Reflow
**Wafer bumping technologies**

Electro migration risk assessment for ultra low track spacing

Figure 1: Electromigration in RDL traces becomes relevant when L/S shrinks.

**Electromigration background**

Figure 2: Two forces (red and blue) act on metal ions of Cu. The blue arrow corresponds to the electric field interaction on metal ions and the red arrow is the resulting force due to momentum transfer between electrons and metal ions from crystalline structure [2].

UBM Free Integration (TSMC)

UFI WLCSP: cost down + reliability increase (Drop & thermal cycling)
Wafer bumping technologies

Fan-in / Fan-out (WL)CSP (Years 2003-2008)
- FO-WLCSP (Fan-Out Wafer Level CSP – IBM)
- eWLB (embedded Wafer Level BGA – Infineon + STATS-ChipPAC)
- RCP (Redistributed Chip Package – Freescale + NXP)

Suitable when the bump number cannot be generated within the native die footprint.

A specific die redistribution + redistributive-wafer molding processes needs to be done before to operate the RDL and bumping processes
Wafer bumping technologies

Medium pitch: Pad diameter > 150µm, Pad pitch > 300µm
ENiG / ENEPiG UBM (Cost effective for these bumping technologies)
- Pactech equipment and technologies fully matured until 12” wafer

Solder Printing / Solder balling + Reflow + cleaning
- Overprinting technologies, Stencil opening form and thickness (5x max MESH or 7xmean MESH solder paste), paste type - MESH
- Stencil technologies: thickness < 80µm, dual-step thickness, aperture technology (laser, electroformed), MESH temporary stencil...

Solder alloy complexity
- SAC solder composition vs reliability: N-SAC, Bi-SAC, Pearl-balls
- Solder technologies type 6 (5µm - 15µm), advanced Type 7 (2µm - 11µm)
- Solder balling down to 80µm

Solder Printing / Balling + reflow: Bump spacing < pad spacing)
- Bump height dispersion < 10%
- Bumps geometry (1,1 x D for bump diameter vs 0,9 x D for bump height
- Voids < 5% (Vacuum + vapor phase furnace)
Wafer Bumping technologies

Bumping processes requires specific metal above the die pad metal (Al, AlCu or AlSiCu mainly): Under Bump Metallization or UBM.

All UBM stack is composed with same structure
- Adhesion layer (Ni, Ti, TiW, …)
- Diffusion barrier/wet ability (Ni)
- Anti-Corrosion layer (Gold flash)

ENiG Process
Wafer Bumping technologies

- Solder balling (Wafer level processing). Requires flux printing first
  Pitch > 150 µm, Solder ball diameter min. 80 µm. Yield > 99.8%

- Solder jetting (bump to bump process). Laser Jet-SB2 from Pactech
  Thermal ramp-up may impact! Two laser processes available
Wafer Bumping technologies

- Solder printing processes (Wafer level process)
- Pitch from 100µm to 300µm

IC Metallization

Particle size (µm) (Paste type)

Finger-type (FP) pastes

- Type 5: 15-25µm
- Type 6: 5-15µm

Ultra-fine pitch (UFP) pastes

- NEW Type 7: 2-11µm
- NEW Type 8: 2-8µm

Pitch (µm)

500µm | 300µm | 100µm | 70µm | 40µm

150µm bump pitch on 8” Wafer before and after Reflow
Wafer bumping technologies

- **Fine pitch**: pad diameter > 40µm, Pad pitch > 50µm
  - Galvanic growing (SnAg, SnAgCu) over seed layer
  - Redistribution capability (Fan-in CSP or Fan-out CSP)
  - Reflowed bumps (Bump diameters > pad opening)
  - Bump height dispersion < 5%
  - Voids < 1% (Density / Vacuum + vapor phase furnace)

- **Ultra-Fine pitch**: pad diameter > 20µm, Pad pitch > 35µm
  - Galvanic growing (Cu (Ni) + SnAg(Cu), over seed layer
  - Copper or Gold pillars (High stand-off, small diameter)
  - Redistribution capability (Fan-in or Fan-out CSP)
  - Bump diameters ~ pad opening
  - Bump height dispersion < 5%
  - Voids < 1% (Density / Vacuum + vapor phase furnace)
Wafer bumping technologies

Fine pitch / Ultra Fine pitch Solder bumping and Copper Pillar
Wafer bumping technologies

- Wafer test after bumping
  - Cantilever not allowable
  - Vertical probing (With post reflow)
  - Rf testing (Advanced)

- 100% AOI after bumping and wafer testing
  - wafer mapping combination (Electrical + visual failures)
  - Map compatibility with flip-chip bonders map format
High-tech Substrates and Interposers

Flexible substrate

Si-interposer with embedded passive

Glass interposer
Substrate requirement

Electronic component is more and more required to be used in direct die to substrate bonding (Miniaturization, Power dissipation, RF/HF signal integrity, power consumption, 3D access...)

Substrate technologies roadmap should be part of the CMOS node roadmap, even if advanced CMOS nodes are packaged first.

The mains technical targets to be addressed by substrate suppliers:
- Pad pitch < 60µm - Pad size < 45µm
- Tracks Spacing and Width < 45µm
- 4-layers substrate with high density routing (17 i/o’s per mm²)
- Low level substrate profile < 120µm
- Burred vias and blind µvia drilling < 35µm diameter, 60µm depth
- Permittivity levels of polymers (High frequency data transmission)
- Fully protected by stretchable polymer (Low radius folding flex)
- High temperature up to 260°C
Substrate requirement

Substrate application domains has to deal with:

- High resolution alignment tool and controlled pressure lamination tool in order to preserve pitch and spacing accuracy
- Fully automatic controlled plating line to fulfill 3:1 depth/diameter aspect ratio dedicated to burred and embedded µvias
- High resolution photomaskable equipment to preserve a correct over-etching ratio for the metal stacks (lower than 1/3)

Design limitation is driven by flex and rigid substrate technologies. Silicon or Glass interposers is well placed in term of design geometry but not fully in accordance with HEP application and cost requirement.

65µm buried µvia

4-Layers & 150µm profile
Substrate requirement

Such design target is not limited by technology stoppers. Limitation is driven by economical point of view (R&D and investment payback).

- High volume production for an acceptable R&D payback (Mobile phone, memories, consumer electronics, smart-card)
- Flex substrate is more driven by smartcard which not requires high i/o’s density (Screen smartcard market was not successful in 2008)
- High volume market flex and rigid produced mostly in Asia is not requiring such drastic designs
- Mobile phone developed Si and Glass interposers since 2005 which has been more or less stopped for cost down timetable (Only CCD imagers is using in mass production and some medical applications), replaced by Fan-Out CSP for Tx/Rx SiP module.
- Japanese, American and European advanced companies is working on such design constraints with limited tools.
Substrate requirement

Up-to-date TSV design reachable (ASE source)

- TSV MEMS or Sensors
- HBM Memory + logic
- 2.5D Si interposer
- TSV MEMS

<table>
<thead>
<tr>
<th>Diameter (µm)</th>
<th>TSV MEMS or Sensors</th>
<th>HBM Memory + logic</th>
<th>2.5D Si interposer</th>
<th>TSV MEMS</th>
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<tbody>
<tr>
<td>1-5</td>
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<td>30 – 100</td>
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High precision die placement

Flip-Chip technologies

Underfilling technologies
High precision die placement

Die placement may be categories within 3 class of technologies

Die bonding family: low placement accuracy / footprint consumption
- Glue dispensing / DAF + die placement + wire bonding
- Combination DAF or liquid DAF with Grinding or DBG tape (build-up limitation)
- Linked to glue expansion, accuracy placement > 20µm
- Some low shrinkage epoxy from Henkel would limit die shift
- Solder bonding or Silver Sintering technologies for power die (Back-side metal)

Wire bonding technologies interconnexions: +/- 15µm accuracy
- Gold or Copper ball bonding [15µm-50m] - Dall diameter # 2 x Wire diameter
- Fine Alu or Gold wedge bonding [15µm-75µm] - L x l stitch # 2 x 1.5 wire diameter
- Heavy wedge bonding Al, Cu or CuCorAl [150µm-500µm] Power – Wire cutter !
- Ribbon bonding Al, Cu or CuCorAl [Various] Power
- Copper/Alu and Copper/Sn limitations in high Temp application
- Option small and ultra-small pitch tool for ball and wedge bonding
- Option deep access tools for wedge bonding
- Front cut or rear cut for heavy wedge bonding
- Mode standard (1st stitch or ball / loop / 2nd stitch) or Reverse
High precision die placement

Option stacked die: extension of the 1st bonding family
- Pyramidal or overhanging with spacer technologies (DAF requires)
- Poly-focus wire-bonding CCD up to 7 stacks (High loops with sweeping risks)
- Reverse ball-stitch on ball (rbsob) to have low loop at die pad
- Warning on wire damaged when direct contact with upper die

- Developed for Automotive and mobile phone first
- Specific technologies developed by PCB manufacturers (AT&S, Deaduck, Würtz, Schweizer, STAT ChipPAC…). Proprietary and patented technologies.
- RF and Si-capacitor die in production
- Power die under qualification
- Accuracy placement down to +/-12µm (Lamination process)
- Flip-chip and direct bonding options
- Copper electro-plating for die to laminated embedded layer interconnexion
High precision die placement

Flip-Chip family: focus of this presentation
- Standard accuracy: +/- 15µm
- Low UPH for recognition + substrate/die co-design: +/- 7µm
- Ultra-low UPH for recognition + substrate/die co-design: +/- 1µm

Several technologies depending on bump materials and capabilities
See after

Requires Underfill process: organic fill-in into die-to-substrate cavity
- To protect against aggressions (Gas, liquid, foreign solid particles)
- To improve thermal cycling and/or drop tests results
- Specific design material to avoid CTE mismatch and high strengths

Several technologies depending on bump materials and capabilities
See after
MASS REFLOW PROCESS

All die placement on substrate, then global reflow

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Reflowable bumps - Flux requires for wettability and heat transfer
Flux dipping option into flip-chip bonders
Voids limitation with vacuum or vacuum/vapor-phased furnaces

Self alignment in pad mirroring design:
Placement +/- 15µm
After reflow: misalignment from +/- 7µm to +/-10µm
UPH up to 3500
LOCAL or IN SITU REFLOW PROCESS

Die placement and thermal profile die after die

Diabolo shape: thanks to z-up head process

Reflowable bumps - Flux requires for wettability and heat transfer
Flux dipping option into flip-chip bonders
Specific bond head (T). Head/Chuck planarity.

After reflow, Die misalignment is the die placement accuracy
After reflow: from +/- 15\(\mu\)m to +/-1\(\mu\)m according to equipment
UPH could be up to 800 (heating time constraint)
THERMO-COMPRESSION (Gold)

Die placement and thermal profile die after die

- UP TO 420 °C
- UP TO 350 °C

Chip

Substrate

- UP TO 350 °C

Non Reflowable bumps – Gold-Gold Interconnect (GGI)
Pressure: from 15gr/bump to 50grs per bump thanks to diameter Specific bond head (T° and P) - Head/Chuck planarity

After thermal profile, die misalignment = die placement accuracy
From +/- 15μm to +/-1μm according to equipment
UPH could be up to 800 (heating time constraint)
Die-to-Substrate Interconnexions

**Underfilling step included**
with ACF/ACP/NCF/NCP

Underfilling step to be done after flip-chip process
Post flip-chip underfilling technologies: (Capillary effect increased with heat)

By dispensing: high volume dispersion
- Bleeding > 1mm (dispense side) – Bleeding > 500µm (other sides)
- Build-up material over the die

By jetting: high accuracy control (µg precision)
- Bleeding < 350µm (jet side) – Bleeding < 150µm (other sides)
- No build-up material over the die

Void control only by acoustic tomography
Copper global repartition to be checked at substrate design phase
Low $T^\circ$ profile flip-chip process to be preferred (Technology)
Underfill material design to be adapted (CTE mismatch)
Ramp-up & ramp-down during polym lower as possible (0.5°C/sec)
THANK YOU FOR YOUR ATTENTION

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