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- **250 nm**
- **130 nm**
- **65 nm**
- **28 nm**
Design kits support  TSMC-65nm

Metal stacks available:

- 6+1 metal stack
  4 thin – 1 thick – 1 UltraThick – RDL

- 7+1 metal stack  ← NEW
  5 thin – 1 thick – 1 UltraThick - RDL

- 9+1 metal stack
  7 thin – 1 thick – 1 UltraThick - RDL

Standard cell libraries available:

- 7 tracks  Std-$V_T$
- 7 tracks  Low-$V_T$  ← NEW
- 7 tracks  High-$V_T$  ← NEW
- 9 tracks  Std-$V_T$
- 9 tracks  Low-$V_T$  ← NEW
- 9 tracks  High-$V_T$  ← NEW
- 12 tracks  Std-$V_T$  ← NEW
- 12 tracks  Low-$V_T$  ← NEW
- 12 tracks  High-$V_T$  ← NEW

6+1 Metal Stack
Design kits support  TSMC-130nm

Metal stacks supported:
- 7+1 metal stack
  - 5 thin – 1 thick – 1 UltraThick – Aluminum RDL

Standard cell libraries available:
- 9 tracks  Standard-$V_T$
tcb130ghp
- 9 tracks  Low-$V_T$
tcb130ghplvt
- 9 tracks  High-$V_T$
tcb130ghphvt

7+1 Metal Stack
Supported design tools for CERN Design-Flow:

- **CONFRMAL** (equivalence checking) **CONFORML_16.10.240**
- **QRC** (Extraction) **EXT_15.26.000**
- **GENUS** (Synthesis) **GENUS_16.12.000**
- **VIRTUOSO** (Analog design) **IC_6.1.7.704**
- **INCISIVE** (Digital simulation) **INCISIVE_15.20.010**
- **INNOVUS** (Place and route) **INNOVUS_16.13.000 / 17.12**
- **MMSIM** (Analog Simulation) **15.10.627**
- **PVS** (Physical Verification) **15.17.000**
- **TEMPUS** (Timing closure) **SSV_16.13.000**
- **VOLTUS** (Power closure) **SSV_16.13.000**
- **UVM** (verification methodology) **VIPCAT_11.30.044_UVM**
Digital-on-top flow - Available scripts

Digital design flow scripts:

- For **synthesis** with Genus
- Digital **back-end flow** with Innovus
  - For wirebonded designs
  - For Flip-Chip (bumped) Peripheral-IO Designs: ← Under development (Available soon)
  - For Flip-Chip (bumped) Area Array Designs: ← Development will follow (Available soon)
- **Timing signoff** with Tempus
- Activity based **power verification** with Voltus
- VCD based **Power verification** with Voltus ← Under development (Available soon)
Macro-blocks available  TSMC 65nm

- **Rad-Tolerant SRAM**  \textit{Silicon Proven}
  - Compiled at request
  - Only Standard-$V_T$ and 4 metal levels used
  - Operation 80 MHz at 1.2 V
  - Dual-port
  - TID and SET tolerant

- **TSMC Static RAM**  \textit{Silicon Proven}
  - Compiled at request

- **E-Fuse IP block**  \textit{Silicon Proven}

- **Rad-Tolerant Bandgap Reference Voltage generator** Diode Based  \textit{Silicon Proven}

- **Rad-Tolerant Reference Voltage generator** DTN MOS Based  \textit{Silicon Proven}

- **Rad-Tolerant ESD structures for Periphery IO**  \textit{Silicon Proven}

- **Rad-Tolerant ESD structures for Area array IO**

- **Rad-Tolerant CERN IO pads - CMOS driver/receiver 1.2V**  \textit{Silicon Proven}

- **Rad-Tolerant SLVS Drivers/Receivers**  \textit{Under development}

- **Seal ring**
Macro-blocks available  TSMC 130nm

- Rad-Tolerant SRAM  *Silicon Proven*
  - Compiled at request
  - Only Standard-$V_T$ and 4 metal levels used
  - Operation 80 MHz at 1.2 V
  - Dual-port
  - TID and SET tolerant

- E-Fuse IP block  *Silicon Proven*

- Rad-Tolerant Bandgap Reference Voltage generator  *Silicon Proven*

- Rad-Tolerant ESD structures for Periphery IO  *Silicon Proven*

- Rad-Tolerant CERN IO pads - CMOS driver/receiver 1.2V  *Under development*

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<td>Mem Depth</td>
<td>64</td>
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</table>
Macro-blocks available  GF 130nm

- Radiation Tolerant ESD structures for IO pads  *Silicon Proven*
- Radiation Tolerant 12-bit, 32-input monitoring ADC  *Silicon Proven*
- LVDS drivers and receivers  *Silicon Proven*
- sLVDS drivers and receivers  *Silicon Proven*
- SRAM generator (40MHz, dual-port synchronous)
- eFuse (1- and 8-bit; 3.3V-10mA-burn in <1ms for 8 bits)  *Silicon Proven*
- Bandgap (diode based, current output 597 ± 4 mV over p,V,T)  *Silicon Proven*
- DAC: 8-bit, current output, 40nA LSB  *Silicon Proven*
Design kits, Macro blocks and Digital flow – Get access

**CERN**  ➔ Development of Mixed Signal PDK and digital on-top design flow
Support for the Digital-On-Top design flow

**IMEC**  ➔ Distribution of the CERN Mixed Signal PDK and support of the native foundry PDK

To get access to the **Design Kits and PDK**:
- For already inscribed institutes  ➔ Contact epsec@imec.be
- For new users  ➔ Contact foundry.services@cern.ch

To get access to the **Digital design flow** scripts:
- For inscribed institutes  ➔ Download: https://espace.cern.ch/asics-support/
- For new users  ➔ Contact foundry.services@cern.ch

To get access to the **Macro-Blocks**:
- For inscribed institutes  ➔ List is available at: https://espace.cern.ch/asics-support/
- For new users  ➔ Contact foundry.services@cern.ch
Website:

- Distribution of CERN digital flows
- Training material and workshops for digital design tools
- Information about the TSMC130nm and 65nm technologies
- Distribution of the Global Foundries 130nm design kit
- Information about the available macro cells

Coming soon:

- Blog/Forum where you can find and share recommendations about Analog and Digital design. The forum is under construction and will be available in the following months.

Access:

- Link: [https://espace.cern.ch/asics-support/](https://espace.cern.ch/asics-support/)
- To get access contact: foundry.services@cern.ch