Introduction to the LpGBT-FPGA

TWEPP 2018 – FPGA Working group

Collaboration (CERN EP-ESE)
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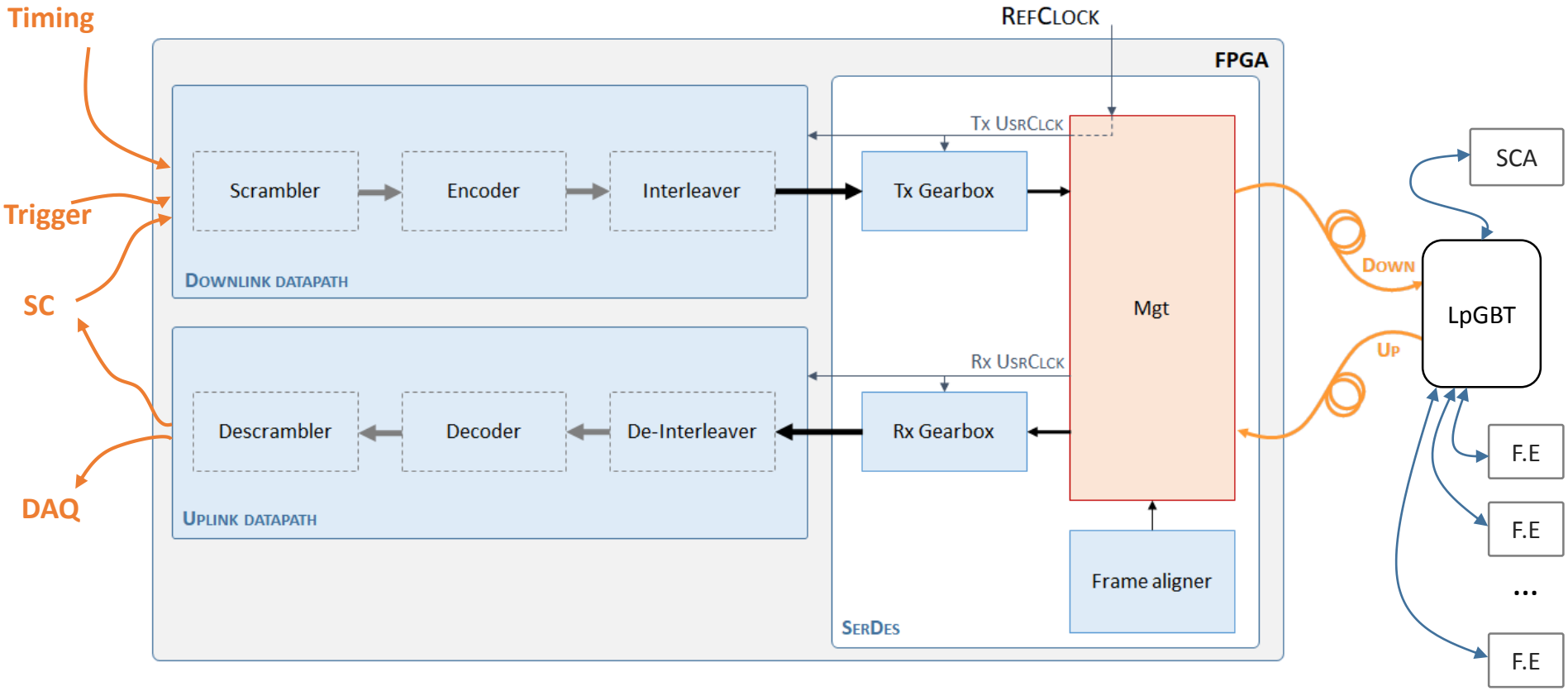
LpGBT-FPGA Architecture

- LpGBT-FPGA is the FPGA counterpart of the LpGBT ASIC.
  - Made to be implemented into the back-end FPGA for HEP.

DOWNSTREAM:
Line rate: 2.56Gbps
FEC: FEC12

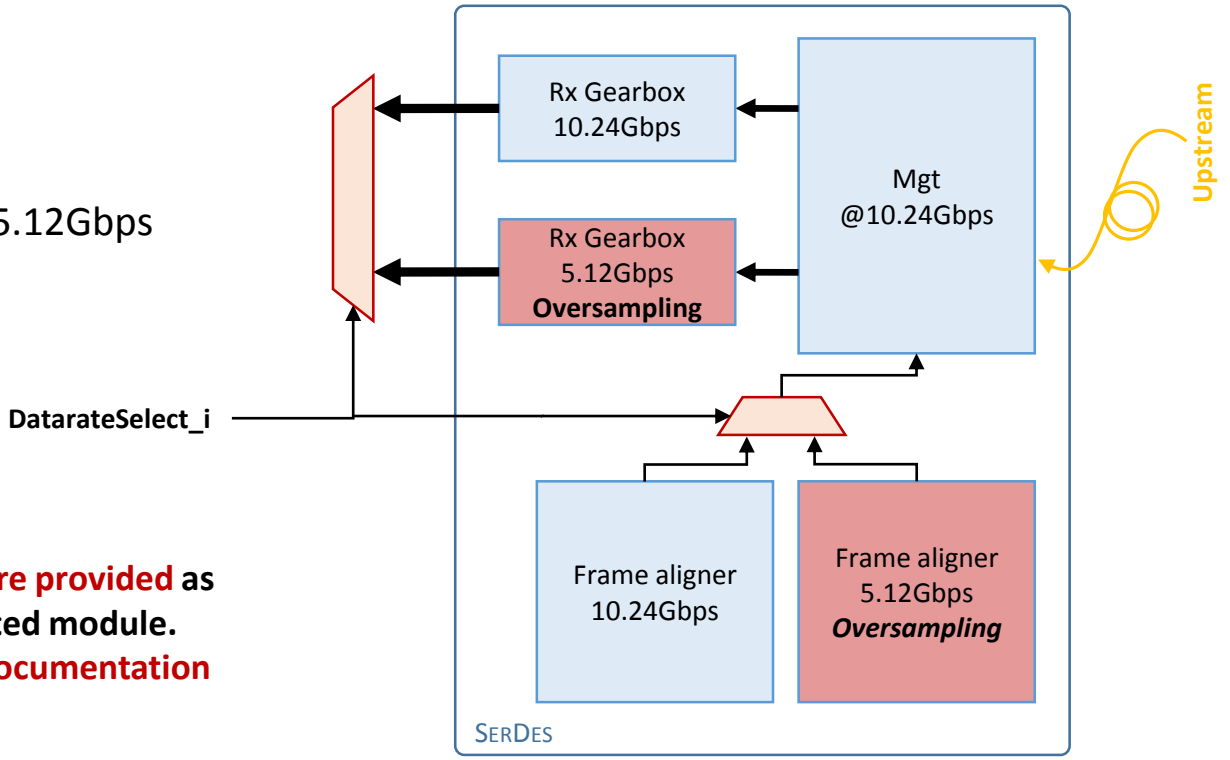
UPSTREAM:
Line rate: 10.24 or 5.12Gbps
FEC: FEC12 or FEC5



Multi-configuration capability: versatility vs. complexity

- Data rate configuration: MGT configuration and/or oversampling
  - Impact on resources and **timing constraints**.
  - Having only one configuration for both speed is binding.

32 bit word size
when only 16 is needed at 5.12Gbps

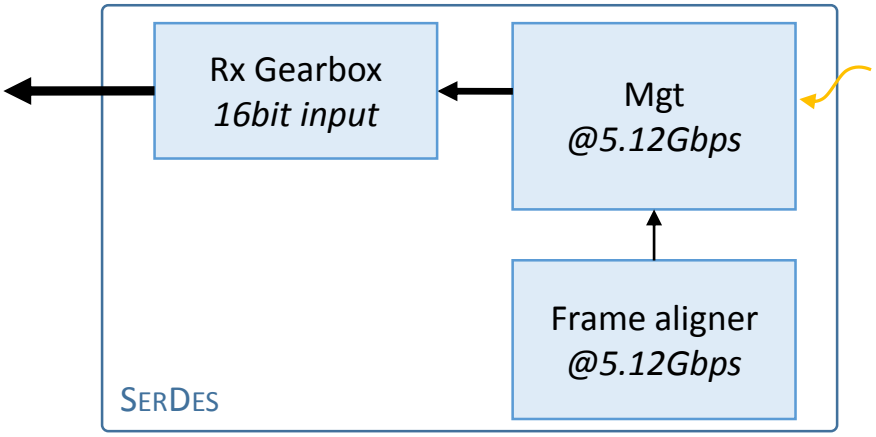


Example of a dynamic data rate instantiation

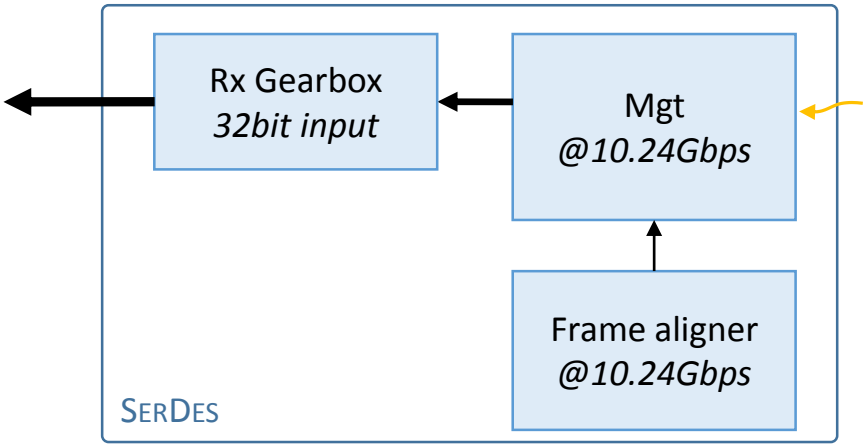
SERDES part is not anymore provided as a single and fully integrated module. However, example and documentation are available.

Multi-configuration capability: versatility vs. complexity

- SERDES design for static configuration



Example of a static 5.12Gbps instantiation



Example of a static 10.24Gbps instantiation

- Static vs. Dynamic:

Static:

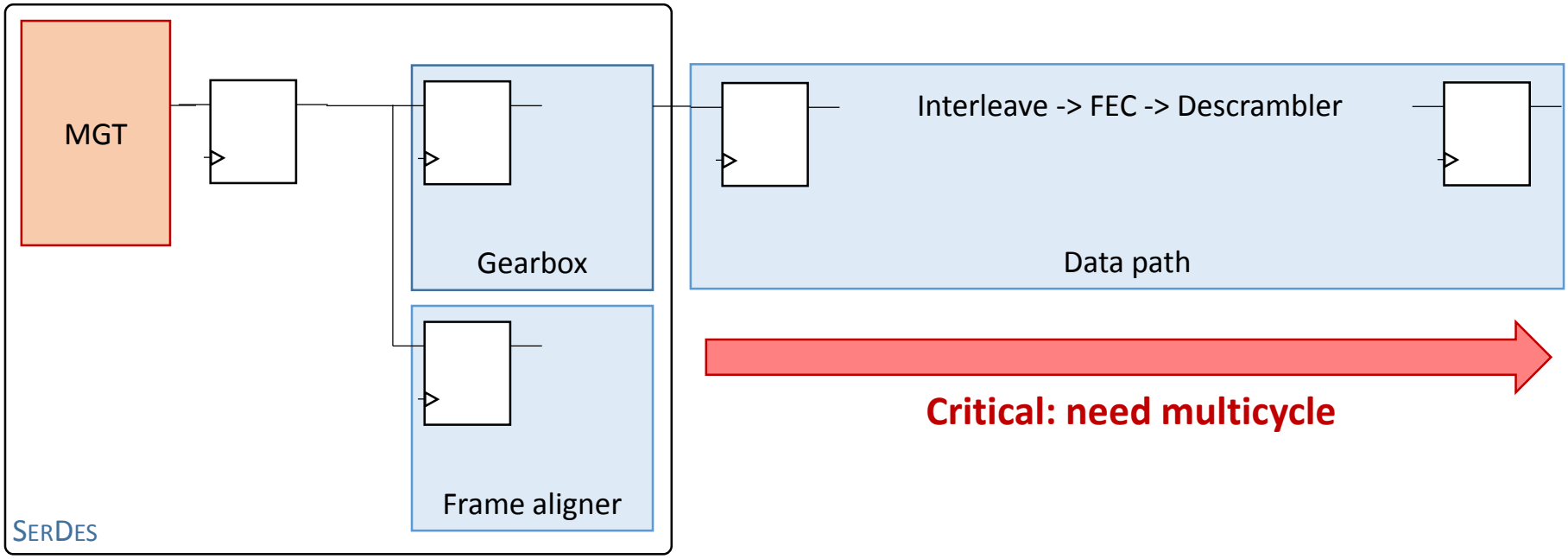
- Performance
- Resources
- "Easy to implement"
- Timing closure

Dynamic:

- Versatility

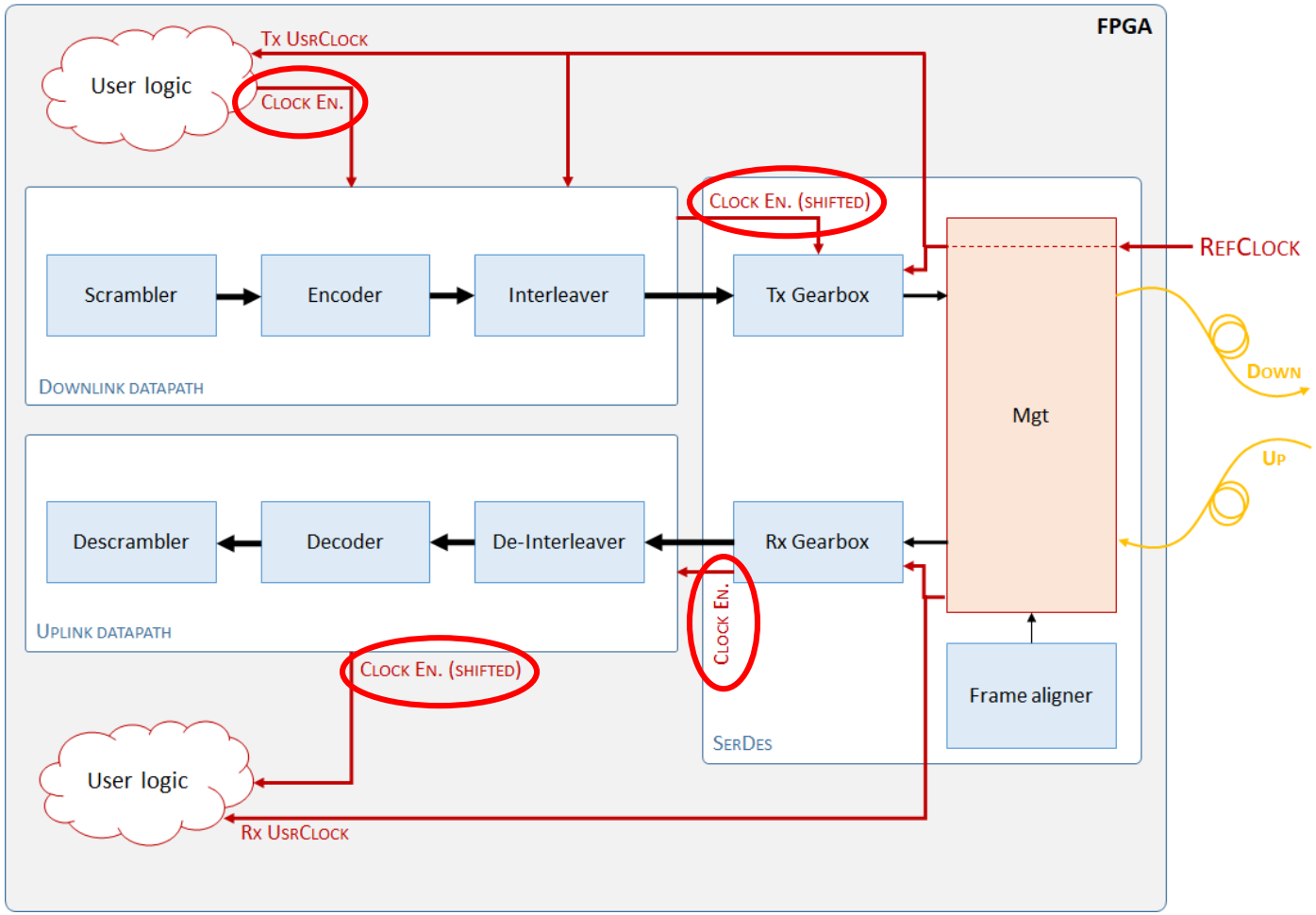
Timing challenges

- Working with the UserClocks @320MHz implies:
  - 3.125ns between 2 registers for each bit (up to 255bit buses in uplink data path)
- Routing cannot be achieve without pipeline and multicycle
  - Especially on the Rx side (decoding)
  - More and more difficult when number of links increases



Timing challenges

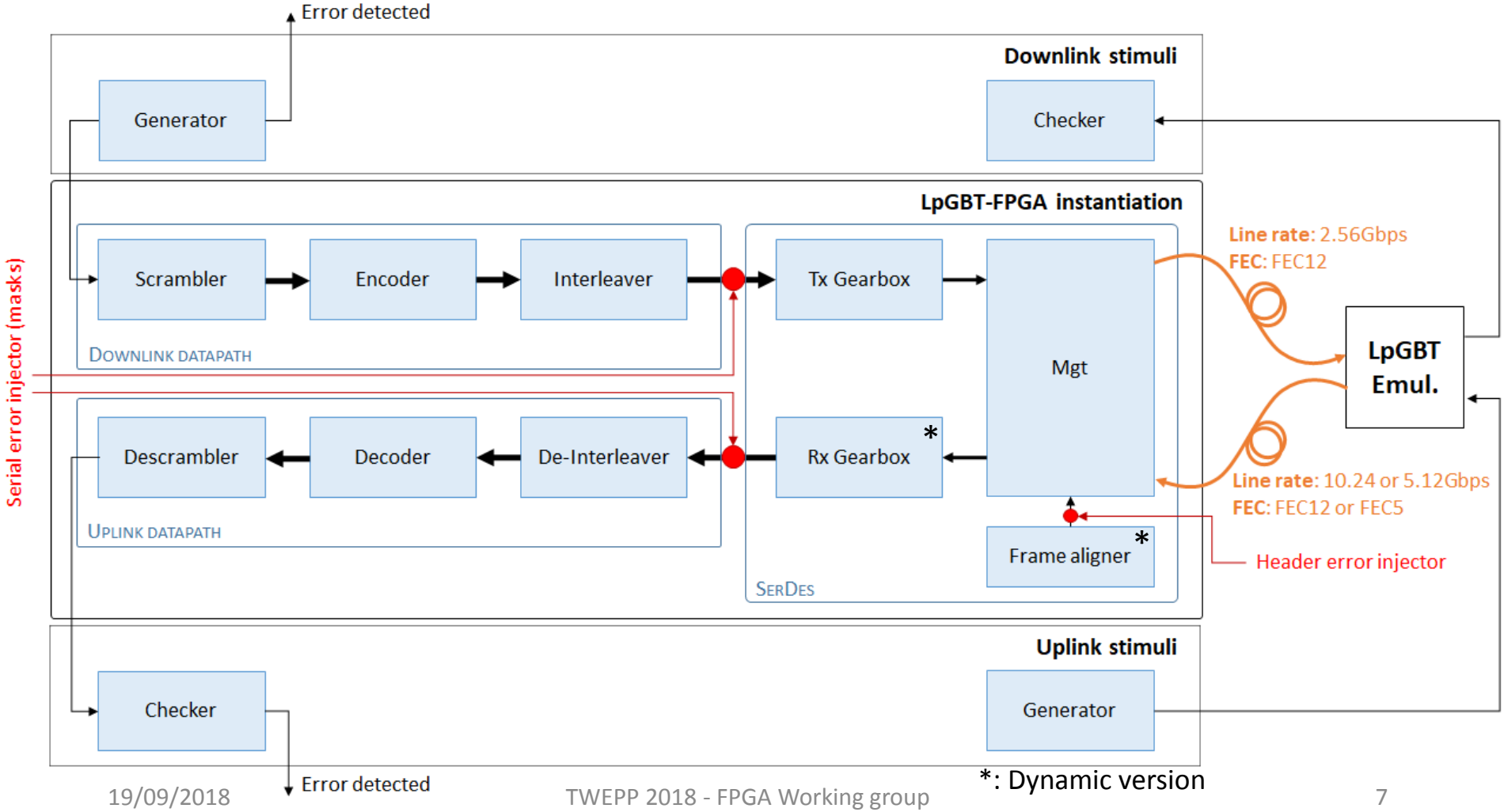
- Multicycle based on clock enable signal (shifted in the datapath)



Test benches

UP/DOWN ASYMMETRY:
Loopback cannot be used

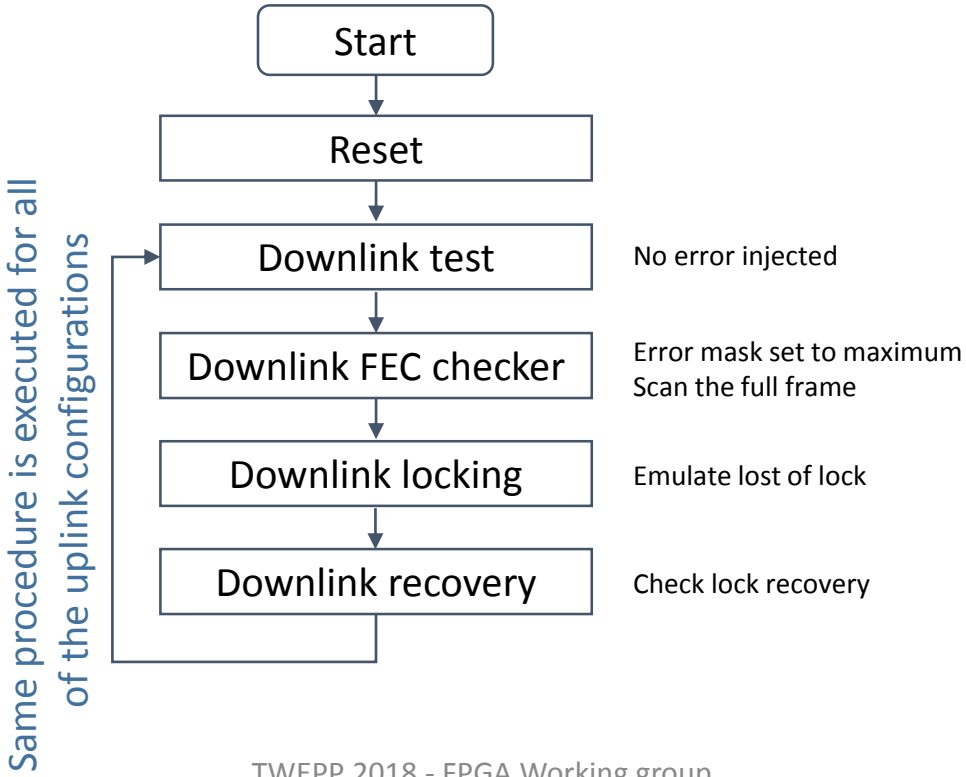
- Two test benches: simulation and KCU105



*: Dynamic version

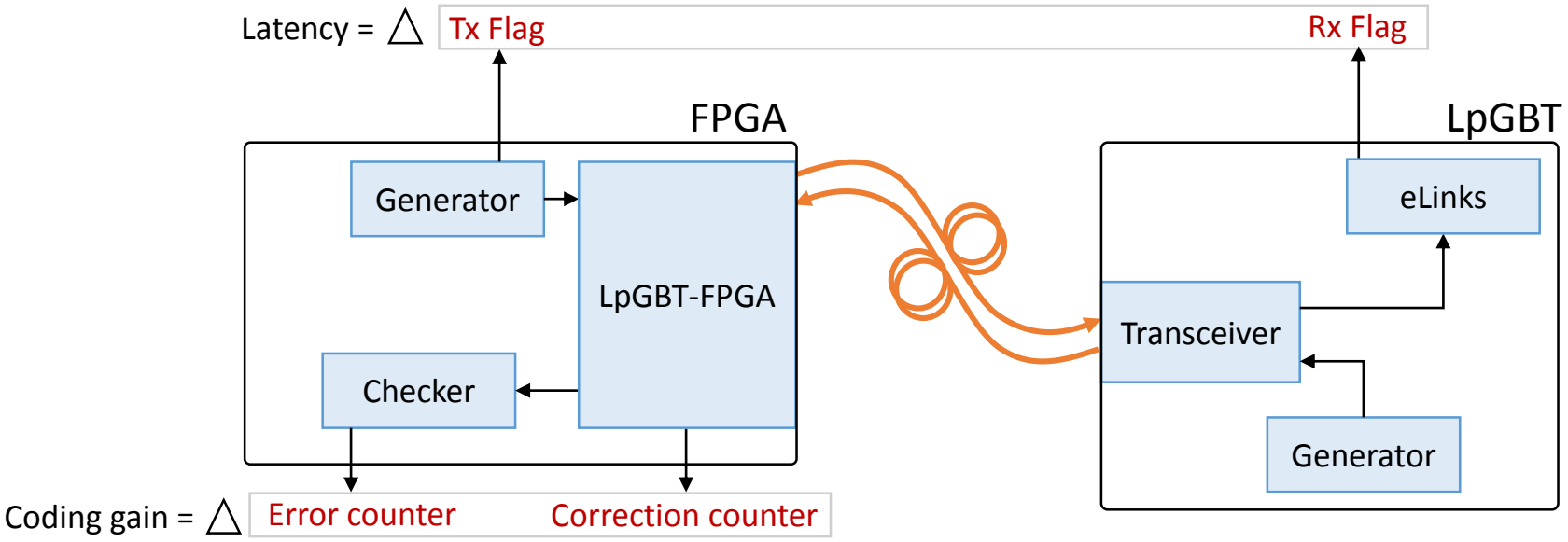
Test benches

- Simulation test bench: behavioral test
  - Continuous integration for automatic testing
  - Inject error in burst to validate the FEC capability (FEC5, FEC12 at 5.12 and 10.24Gbps)
  - Test the header locked functionality



Test benches

- KCU105 test bench: timing and real hardware
  - Check routing feasibility (timing)
  - Future plans: Latency and coding gain qualifications



Summary

- LpGBT-FPGA is ready to be used
  - LpGBT-FPGA IP: https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga
  - Simulation test bench: https://gitlab.cern.ch/gbt-fpga/lbgbt-fpga-simulation
  - KCU105 test bench: https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga-kcu105

- Philosophy changed since the GBT-FPGA IP because of the complexity of the ASIC
  - Design of the SerDes part is left to the user (documentation available)
  - Documentation: http://lpgbt-fpga.web.cern.ch
    - Automatically deployed using Doxygen and Openshift

- Test benches are designed to test and qualify the IP core.
  - First downlink latency measurement (using "LpGBT emulator"): 155ns
  - Stability of the downlink latency between reset (using HPTD module): 12ps

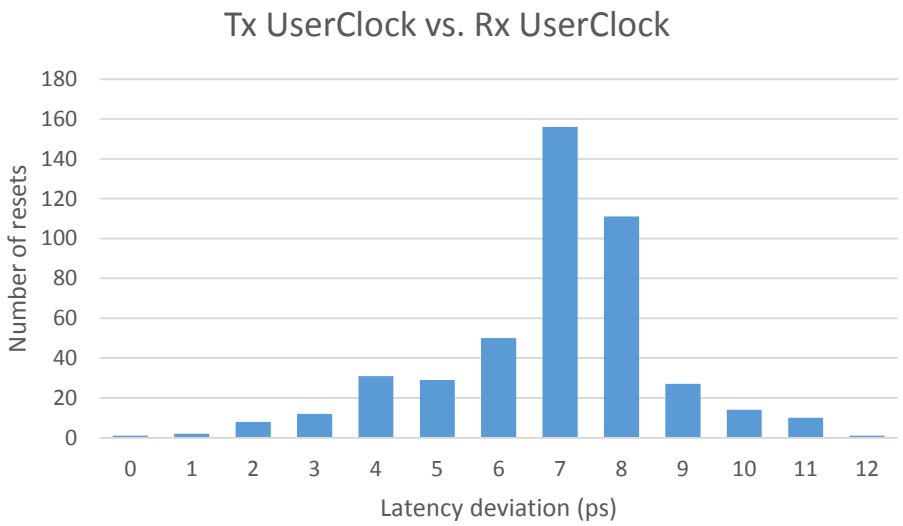
Thank you for your attention

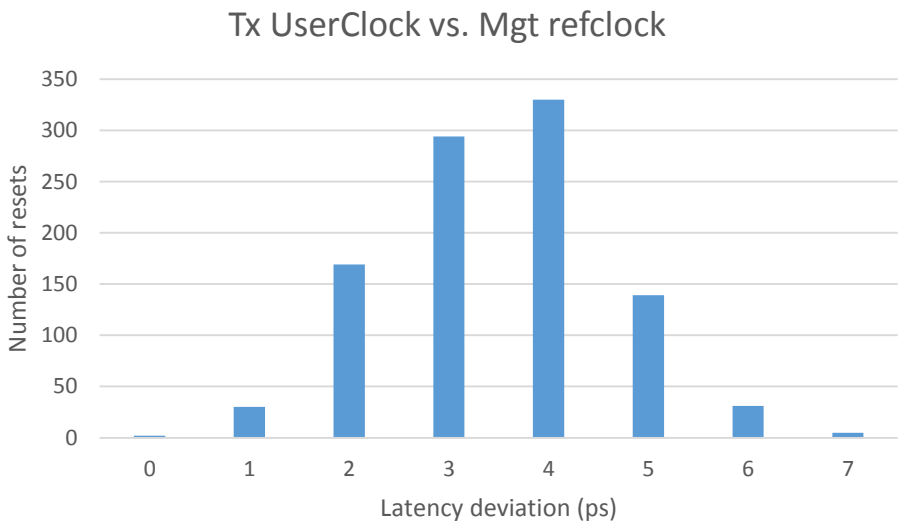
GBT-FPGA Team: GBT-FPGA-support@cern.ch

Backup: latency measurements

Preliminary measurements carried out with the HPTD module implemented and receiver's equalizer set in static mode.

Additional tests have to be performed.





Multi-configuration capability: versatility vs. complexity

- Oversampling:
  - **Tx:** Allow having only MGT configuration for both sides
    - Oversampling ratio: number of times each bit shall be duplicated
  - **Rx:** Allow working in dynamic data rate mode.
    - Oversampling ratio: space between each bit

- Managed by the Tx and Rx gearboxes using 3 parameters:
  - Input width: Input word size (fixed by the data path)
  - Output width: Output word size (fixed by the transceiver's configuration)
  - Clock ratio: ratio between input and output "clocks" / **multicycle** value
    - E.g.: When the data path works with a clock enable of 8, the clock ratio is 8

TX ORATIO = CLOCK RATIO / (OUTWIDTH / INWIDTH)
RX ORATIO = (CLOCK RATIO * INWIDTH)/ OUTWIDTH