Phase Noise Studies on the Si5345 PLL

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With help from CERN EP-ESE

High-Precision Timing Working Group @ TWEPP18

Context

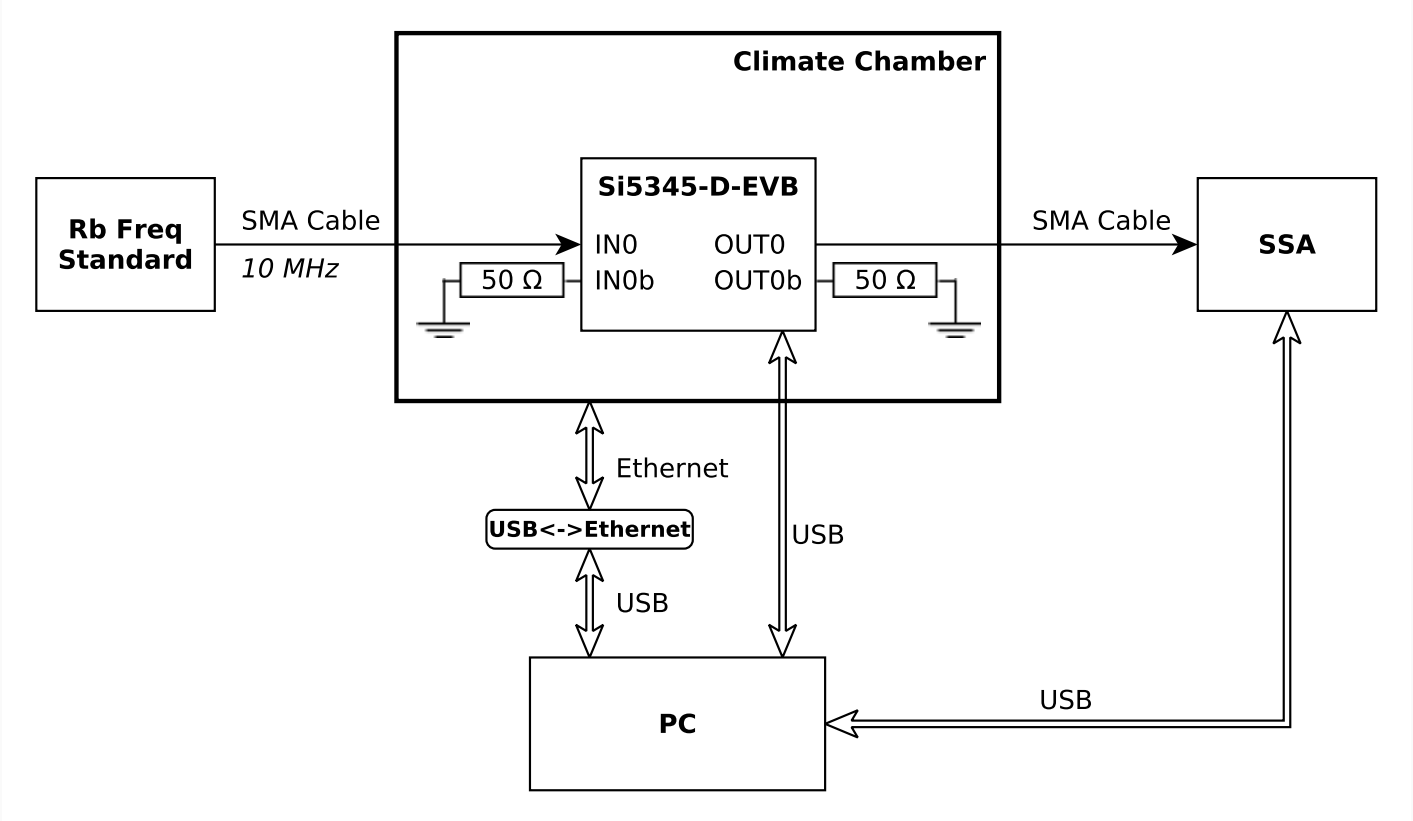
First studies done with components chosen (on paper) for the CMS Phase-2 DAQ and TCDS Hub (DTH).

(See also 'Design and development of the DAQ and Timing Hub for CMS Phase-2' on Thursday morning.)

Intention is to:

- Validate choice of jitter attenuator (Si5345)
- Validate combination of jitter attenuator and crystal/TCXO as Si5345 reference clock
- Gain experience with the SiLabs devices
- etc.

Measurement setup



Input clock source 10 MHz Rubidium clock source: SRS FS725

Signal source analyzer Agilent Technologies E5052B

Climate chamber CTS T-65/50

Software Based on (Python) libraries provided by EP-ESE

Test procedures

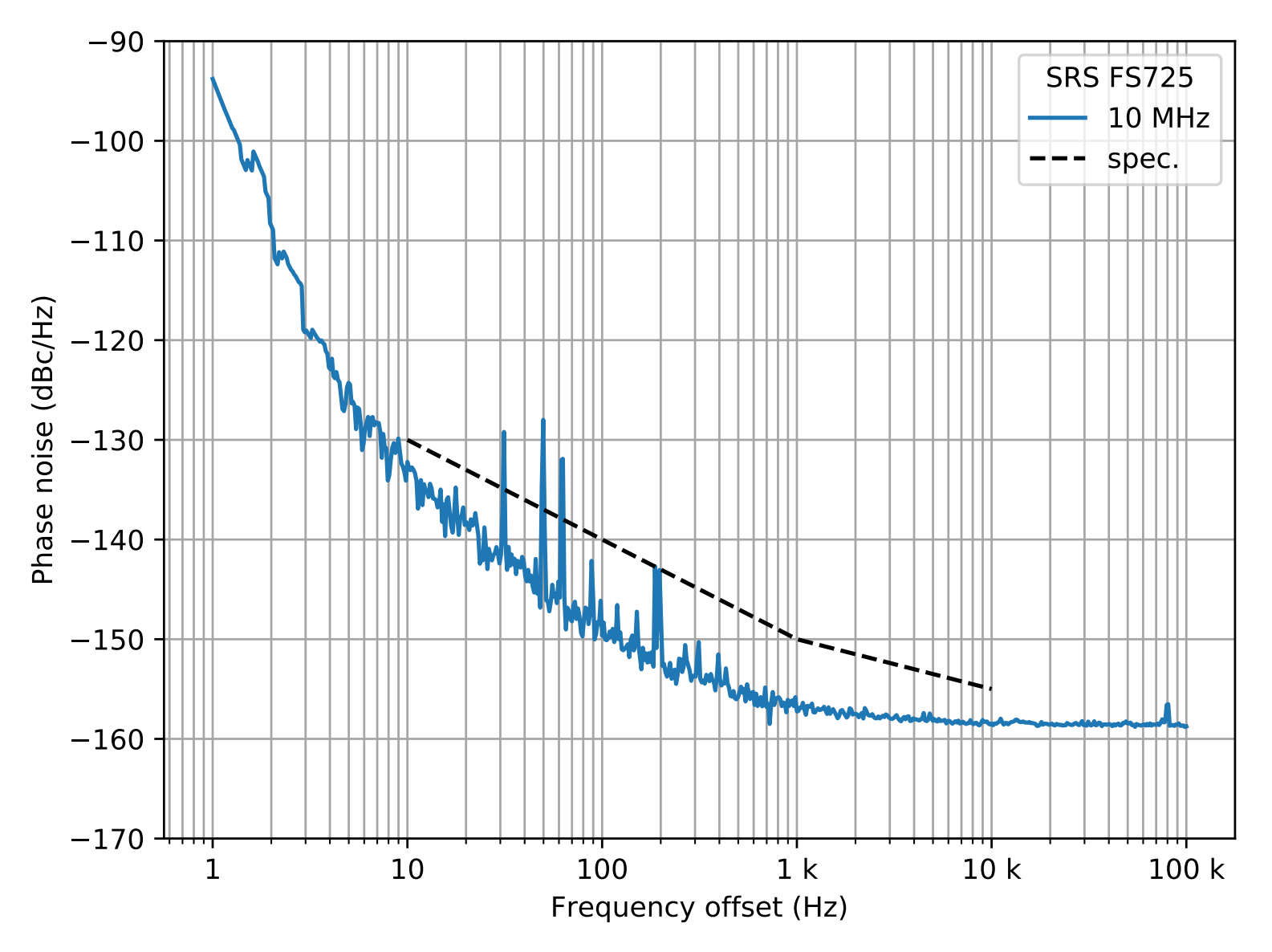
Two kinds of tests:

- Si5345 evaluation board at room temperature, varying PLL bandwidth or generated output frequency
- Si5345 evaluation board running with fixed PLL bandwidth and output frequency, varying ambient temperature

Notes:

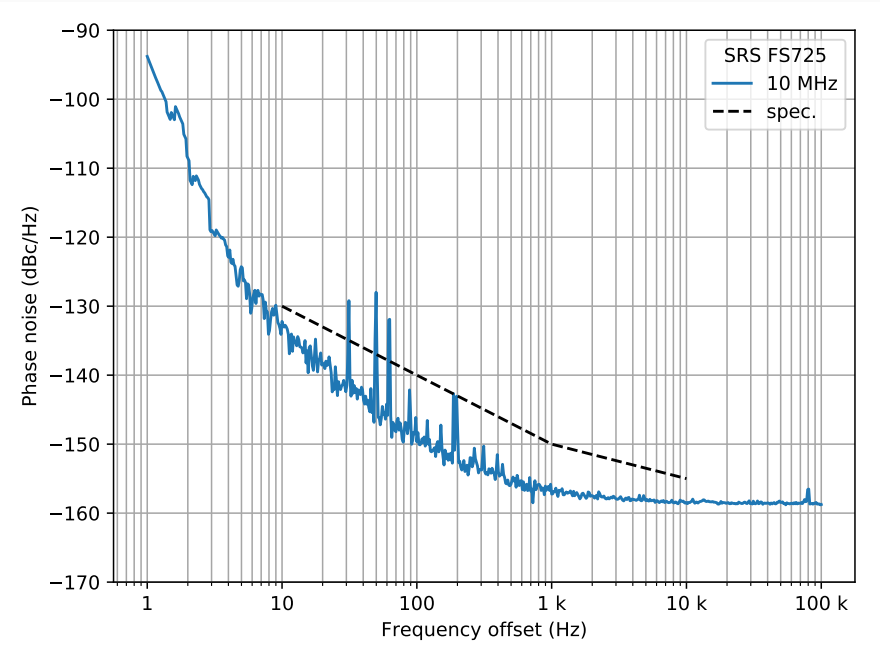
- Si5345 always running in locked mode
- Temperature always required to be stable before measurements
- Climate chamber always switched off before measurements

Intermezzo: phase noise

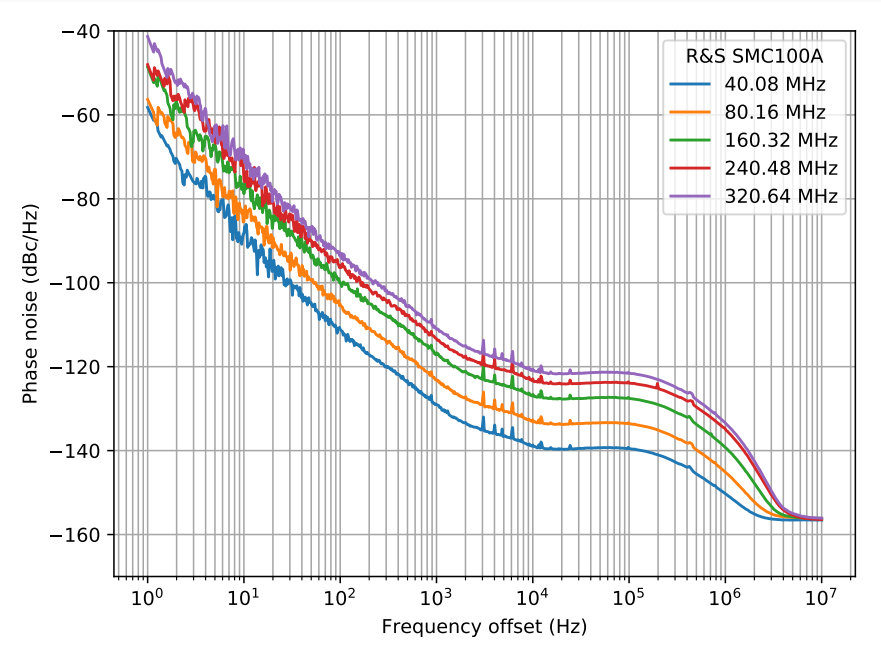


First a look at the generator itself

SRS FS725

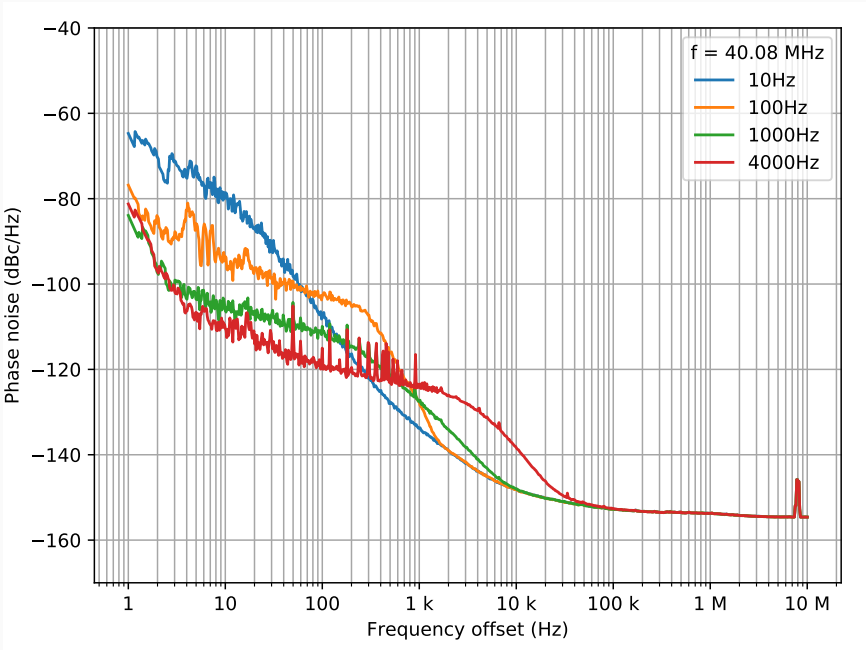


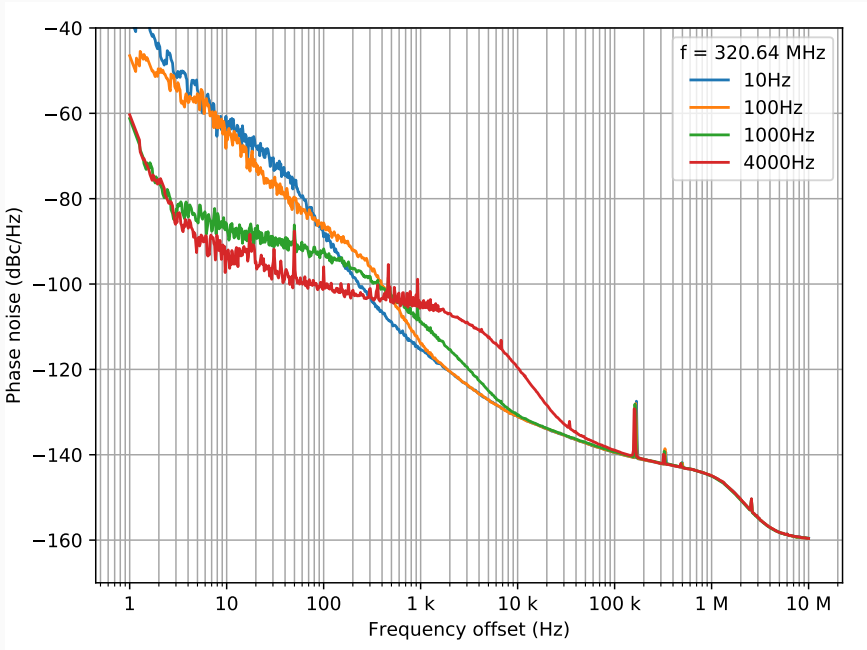
Rhode&Schwarz SMC100A



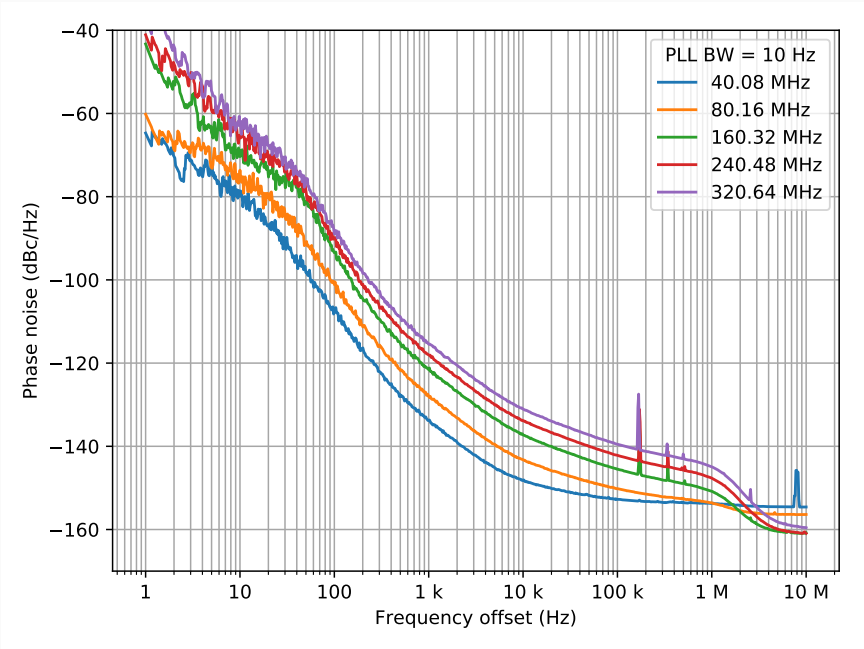
- *Note* the difference in vertical scales
- Generator phase noise in principle behaves as one would expect, apart from some features (probably related to the setup)
- All measurements done for different output frequencies ranging from 40.08 MHz (i.e., the LHC bunch-crossing frequency) to 320.64 MHz (i.e., the lpGBT FPGA reference clock requency)

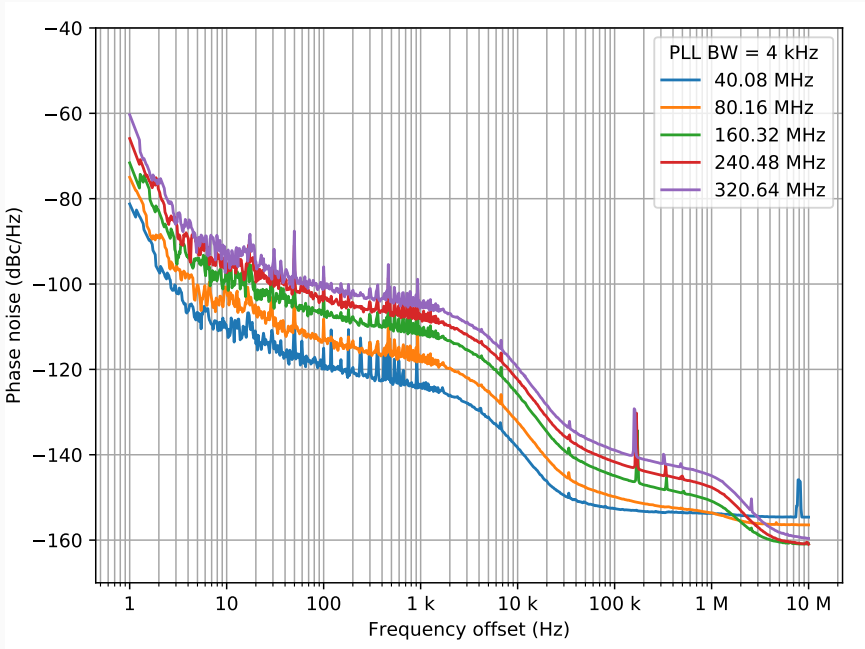
Changing PLL bandwidth (at fixed output frequency)



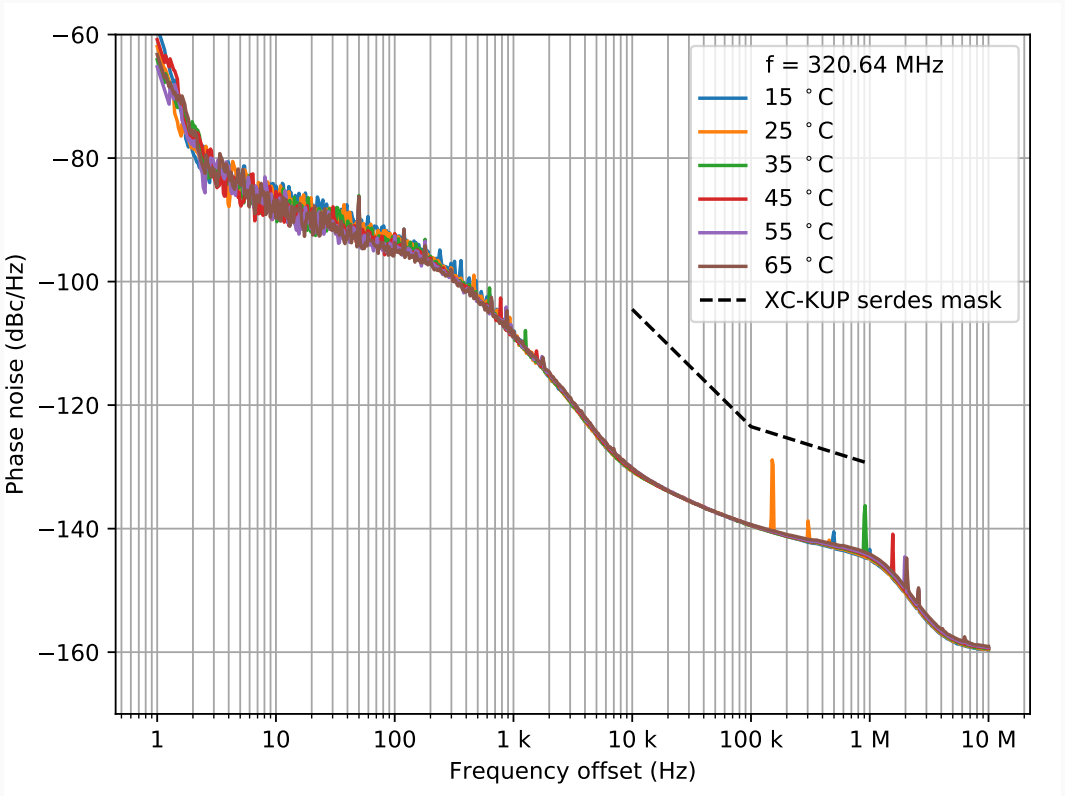


Changing output frequency (at fixed PLL bandwidth)



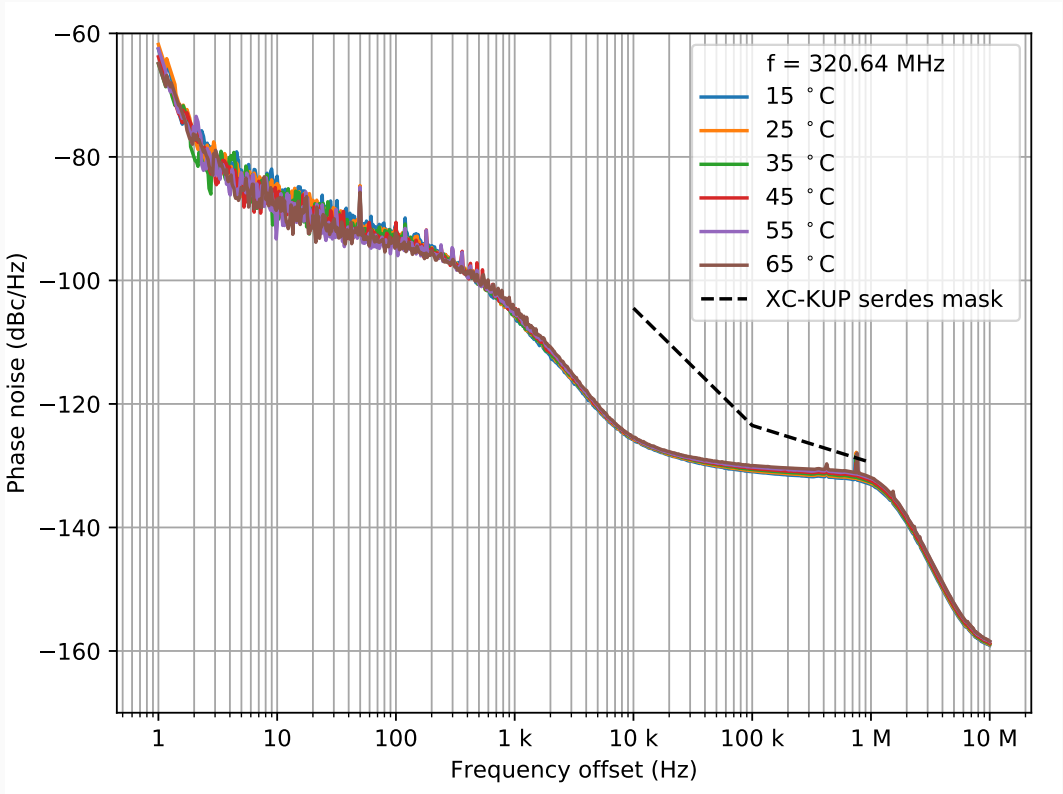


Temperature dependence



- Phase noise much less sensitive to ambient temperature than expected
- In general: jitter cleaner junction temperature ≈10 °C higher than ambient
- *NOTE:* Did not try (steady or fluctuating) air flows across jitter cleaner

Replacing the crystal with a TCXO



- As expected: TCXO better at lower frequencies than at higher
- *Not* as expected: TCXO gives worse performance than simple crystal, even at low frequencies

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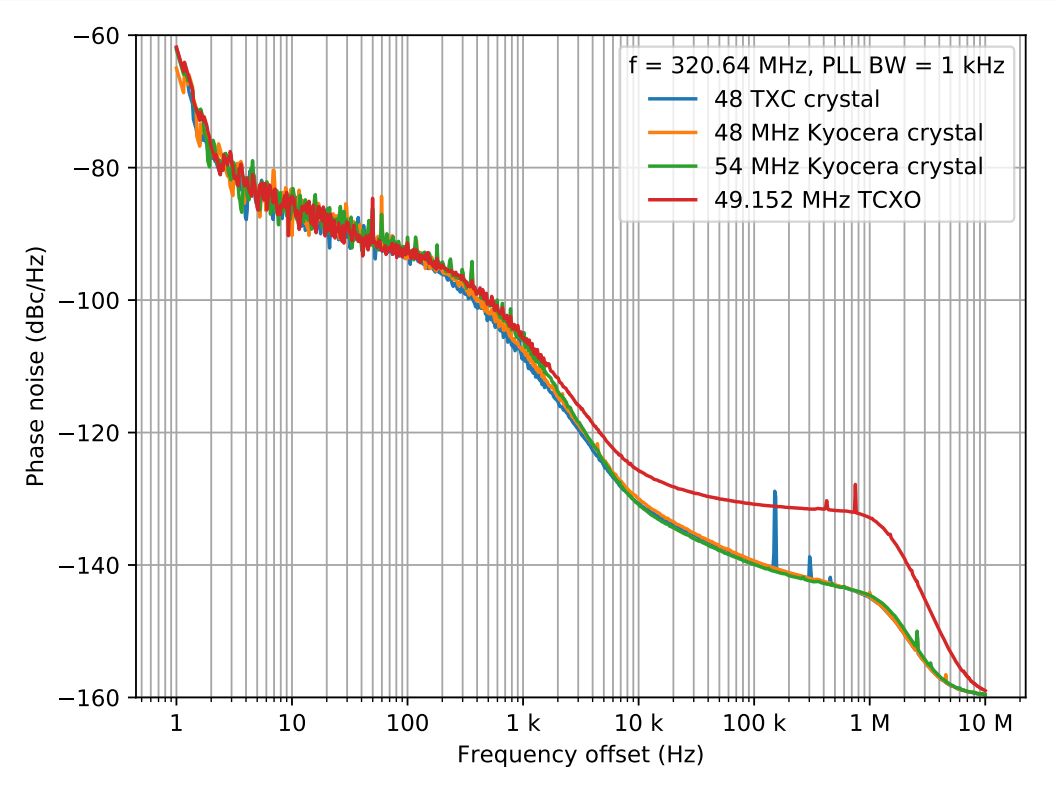

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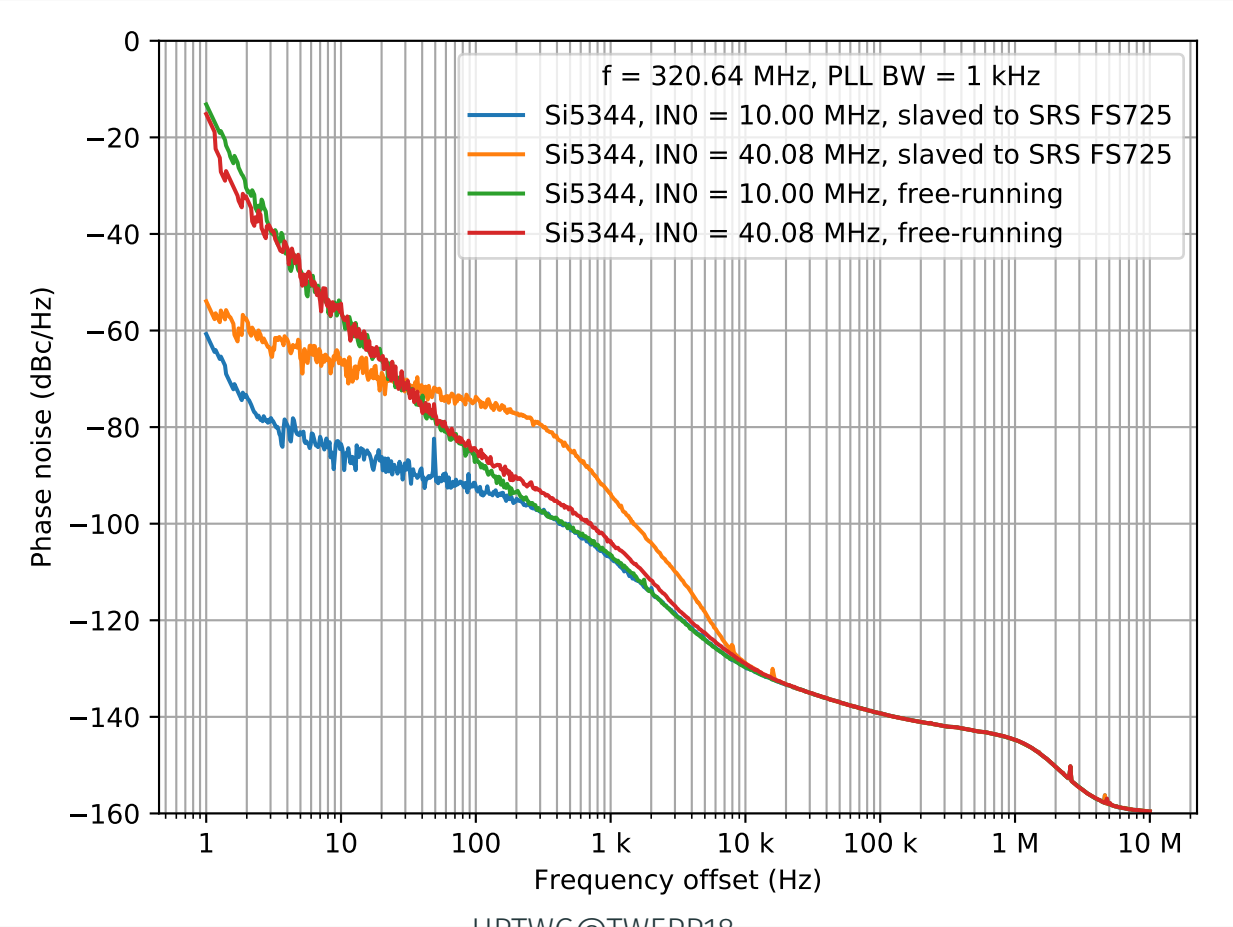
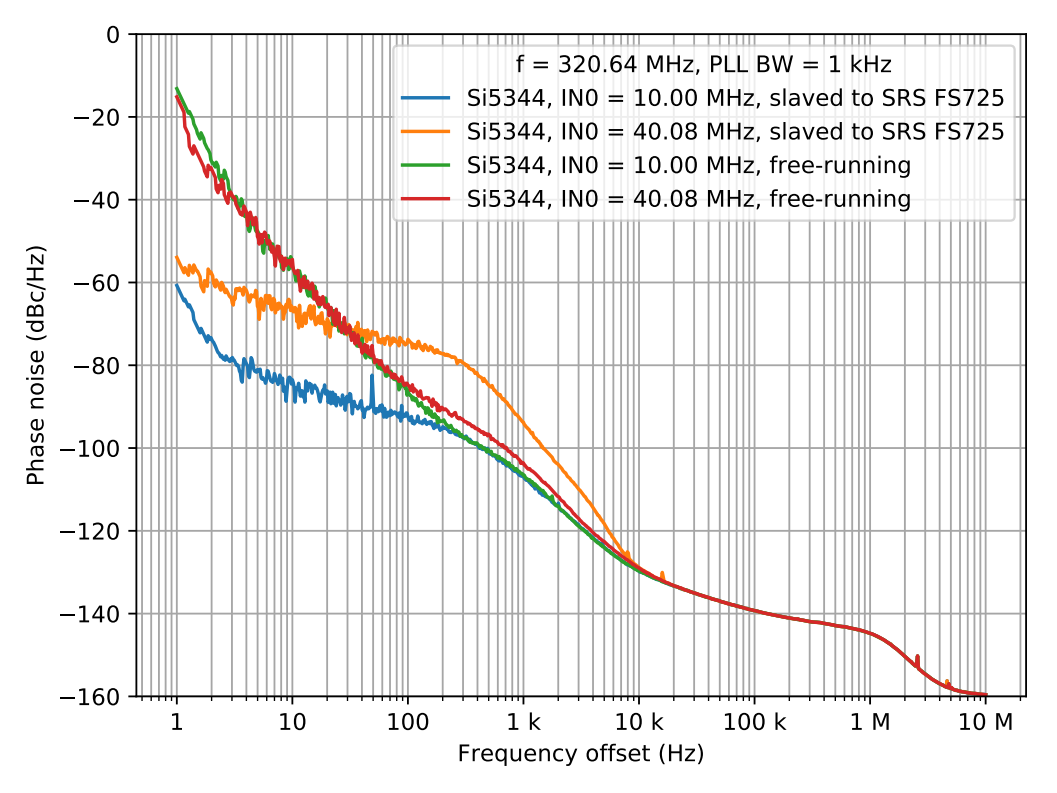
Something more realistic

Chaining two jitter cleaners (à la TTC machine interface and DTH, for example): Si5345 driven by Si5344 (on its own EVB):

- Stand-alone vs. slaved from the SRS FS725
- Generating an intermediate frequency of 40 MHz vs. 320 |megaHz



Something more realistic



- The ‘free-running’ phase noise curves clearly show the ‘crystal shape’
- The bump in phase noise for the 40 MHz ‘slaved’ curve clearly needs optimizing for use in Phase-2 CMS
- For the moment: Si5344 and Si5345 had the same PLL bandwidth. There is (configuration) phase space to be explored here.

Conclusions and plans

- With the SiLabs devices it is easy to generate a good-quality clock. It is even easier to accidentally reduce the quality...
- The Si5345 is much less sensitive to ambient temperature than expected
- Ergo: may not need TCXOs for Si5345 reference clocks, but simple crystals
- All to be verified with real (DTH P1) hardware
- More importantly: start looking into channel-to-channel phase stability

A more complete and descriptive document, with more details and figures, is available on the HPT WG web site:

`https://espace.cern.ch/HighPrecisionTiming/Evaluations/Components%20Evaluations/cms_dth__component_phase_noise_studies.pdf`

Thank you