PROCEEDINGS OF SCIENCE

PACIFIC: The readout ASIC for the SciFi Tracker of the LHCb detector

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PACIFIC is a 64 channel mixed-signal ASIC designed for the scintillating fiber tracker readout and developed for the LHCb upgrade in 2019/20. It connects without any extra components to the 128 channel double-die SiPM arrays sensing the fibres output signal. The analog processing chain begins with a current conveyor followed by a tunable fast shaper and a gated integrator. The signal is digitized with three configurable discriminators at 40MHz. The results of every four channels are encoded to two bits per channel, serialized and transmitted at 320MSa/s over a differential SLVS data link. PACIFIC has been designed using a 130nm CMOS technology and power consumption kept below 10mW/channel.

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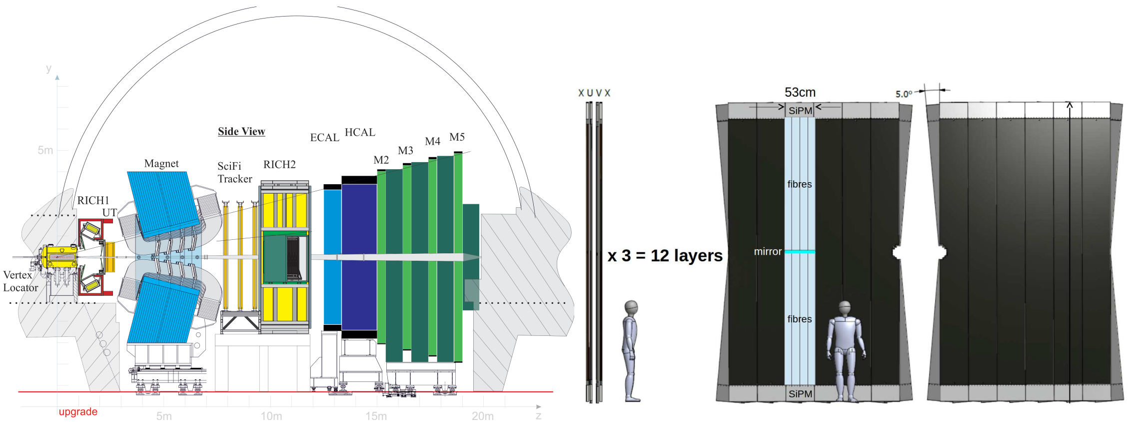
1. Introduction

During the Long Shut-down 2 (LS2) of LHC in 2019/20 and as a part of the LHCb upgrade, the tracking detectors will be replaced in order to cope with a higher instantaneous luminosity and to read out the data at 40 MHz using a trigger-less read-out system. The current LHCb main tracking stations downstream from the magnet will undergo a technology change, being replaced by a single homogeneous detector based on scintillating fibres (see figure 1) and covering the complete 5m$\times$6m acceptance area of the detector [1].



(a) SciFi in LHCb detector (b) SciFi stations

Figure 1: SciFi location and structure (source: LHCb collaboration [1])

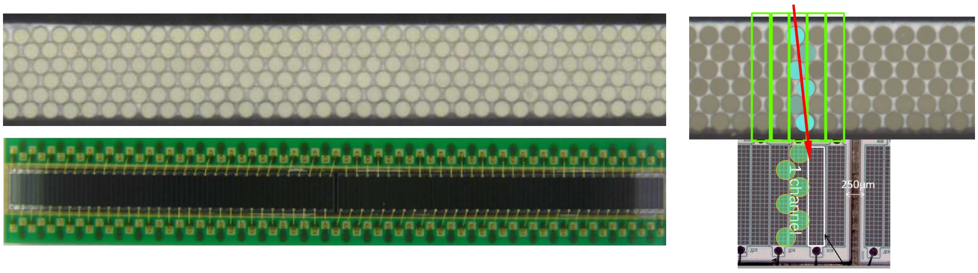
It will be built from Kuraray SCSF-78 blue emitting scintillating plastic fibres with a diameter of 250μm. Six stacked layers of scintillating fibres will produce fibre mats with a length of 2.5m. The scintillation light generated by the particle passing through the mat is guided to both ends and reflected in the inner detector end (using a mirror) and converted into an electrical signal in the outer end using arrays of multi-channel SiPMs. The delivered signals are then processed by a custom readout ASIC, the Low Power ASIC for the sCIntillating FIbre traCker (PACIFIC). The measured raw digital PACIFIC data is processed by an FPGA before being sent by optical links to the readout farm.

As the current detector, the SciFi tracking will comprise three stations, each split in two halves which can be opened and closed around the beam pipe. Each station includes four planes (see in figure 1) denoted as X,U,V,X layers and are placed either vertical (X) or tilted by $\pm 5°$ (U and V respectively). This arrangement provides an excellent single hit resolution in the horizontal direction ($< 100\ \mu$m) and information on the vertical hit position with smaller resolution.

The detector layers are built from full-height (0.5 m $\times$ 4.8 m) individual modules each comprising eight fibre mats (four top and four bottom). To maximize the light collection, mirrors at the inner ends of the fibre mats reflect the light towards the outer ends.

The scintillating light of the fibres is detected by a custom designed SiPM array[3] with a small channel size and reduced channel pitch (250μm) is used based on two 64-channel dies packaged together.

The SiPM channels are not aligned with the fibres. The light signal is therefore split among several channels (see figure 2). Downstream from PACIFIC, an FPGA will run the clustering



(a) Fibre mat cross section and SiPMs view

(b) Signal distribution

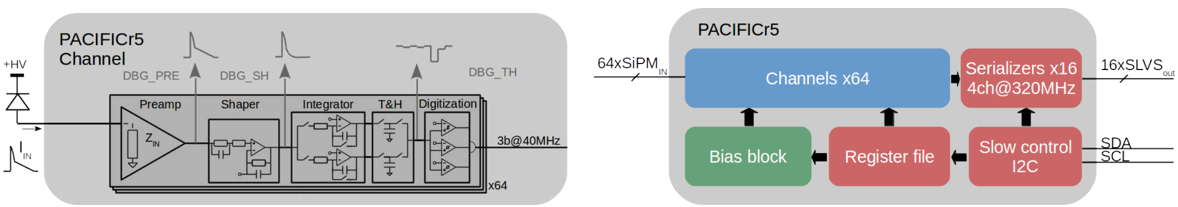
Figure 2: SciFi mat section and SiPM with signal distribution (source: SciFi collaboration)

algorithm on the digitized hit data to determine the cluster position and to reduce fake clusters produced by dark noise hits.

The electronics readout is performed by a processing chain that includes several boards with active devices connected by high density connectors for the sensors and communication between boards (standard FMC connectors have been used for that purpose). The first element of the readout electronics is the SiPM array mounted on a flex circuit. This is connected to the PACIFIC board containing four PACIFIC ASICs. Once the analog signal is digitized, it is sent to the Cluster Boards to perform the cluster algorithm. In the last step the digital cluster data is sent through optical links on the Master Board to the central DAQ.

2. PACIFIC architecture

The low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) grants the 40MHz read-out of the scintillating fibres with reduced dead time. It connects directly to the anode of the SiPMs, performing the sensor signal analog processing and digitization of 64 channels. The power budget was limited to 10mW/channel. The 130nm CMOS process was chosen for its reduced featured size, low power and wide use in radiation-tolerant applications.



(a) Analog channel signal processing

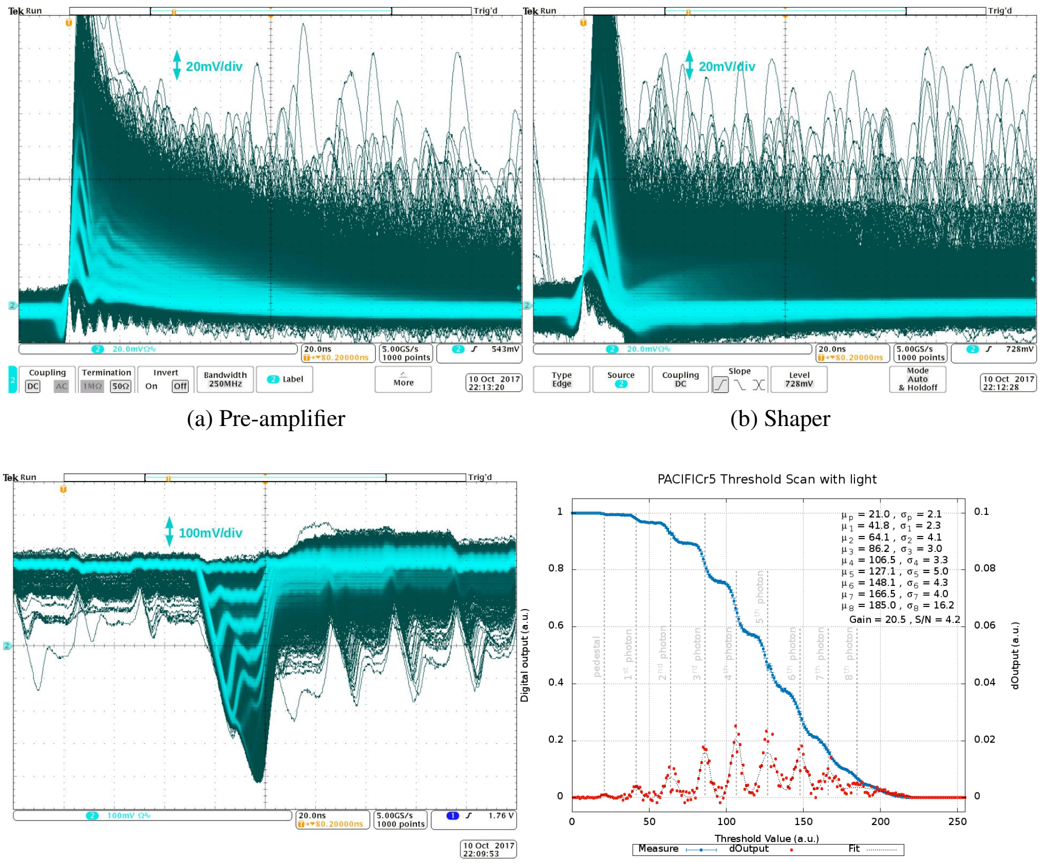
(b) Control and data output

Figure 3: PACIFIC analog chain and control blocks

The analog processing chain can be observed in figure 3. The input stage is a current mode amplifier composed of a current conveyor and a closed-loop trans-impedance amplifier, based on previous prototypes produced in other technology [4]. The current conveyor is based on double feedback approach and optimized for SiPM arrays with anode connections. The double loop provides independent control over the anode voltage and the input impedance over the full bandwidth

(>250MHz). This stage has a low power consumption (<2mW) and a selectable gain that assures a good single cell resolution for calibration.

The signal received by the ASIC extends over several LHC clock cycles, mainly due to the recovery of the SiPM. Additionally, the distribution of the time of arrival of the scintillation light spreads over 60% of the LHC clock cycle. The goal of the shaping stage is to reduce the pulse width to allow a 25ns integration, thus minimizing spillover and the effect of the signal arrival time. A tunable double pole-zero shaper allows to independently cancel the longer exponential decay related to different SiPM capacitances and quenching resistors, as well as the shorter time component, associated with parasitic capacitance and the amplifier input impedance. It is a closed-loop design based on an OTA with high gain-bandwidth product (>300MHz), low power consumption (<700μW), and high load-driving capability, for a fast rising edge. The output offset is controlled using an additional ultra low slew rate baseline restoration feedback loop.



(a) Pre-amplifier

(b) Shaper

(c) Track and Hold

(d) Threshold scan digitized output

Figure 4: PACIFIC analog debug signals and threshold scan data.

The previous fast pulse is integrated with a double gated integrator with high slew-rate. The integration time was set close to the full clock period to cope with the dispersion of the signal time of arrival, so two integrators had to be interleaved to allow time for reset. At the output of the integrators a Track and Hold merges the signals into a continuous output. The bottom plates of the

Track and Hold capacitors, as well as the different switches, are delayed by small time to avoid undesired charge circulation among the different nodes.

Three hysteresis comparators with tunable references complete the 2bit nonlinear flash ADC operating at 40MHz. A serializer generates a 320MS/s stream from the data of four channels.

2.1 Performance

The analog processing chain has several key points multiplexed to some output buffered pads. For this reason, once a SiPM is connected and illuminated with low light intensity, the number of photons can be directly counted in the different intermediate processing points (see figure 4).

The effect of the aggressive shaper removing the tail of the signal is clear and also the gain introduced by the integration. This produces even more clearly distinguishable steps after the track and hold.

Sweeping the threshold of one of the DACs on the signal generates the step like plot produced in figure 4 (d) where every step corresponds to the signal of one photon.

During 2018, a test-beam campaign has been carried out at CERN using final PACIFICr5 production devices packaged and mounted on carrier boards together with prototypes of the final readout electronics. The outcome of the test-beam (to be released as an internal note) measures the single hit resolution better than $100\mu m$ and efficiency higher than 99% with nominal conditions and the full system.

3. Conclusions

PACIFIC has been designed and evaluated focusing on the performance parameters for the final detector. At this stage, all requirements have been fulfilled and the final mass production testing is ongoing.

The proposed architecture has proved to match the detector needs keeping a low power budget and simple integration in the system without the need of more components in the electronic boards.

Radioactive sources test together with test-beam campaigns validated the performance of the electronics and sensors connected to the final modules and scintillating fibres.

We are confident that the construction of the detector and its installation and start-up will be a huge success thanks to the electronics developed.

References

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