PROCEEDINGS OF SCIENCE

System level serial powering studies of RD53A chip

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Serial powering is the baseline choice for low mass power distribution for the CMS and ATLAS HL-LHC pixel detectors. The RD53A prototype chip (65 nm CMOS) integrates 2 shunt-LDO (SLDO) regulators that allow providing constant voltage to each power domain (analog and digital) within a serial power chain with constant current. This paper presents a detailed analysis based on simulations and measurements of the RD53A chip behavior at system level. SLDO performance and system transient behavior (start-up, load changes, parasitic components implications).

Topical Workshop on Electronics for Particle Physics (TWEPP2018)
17-21 September 2018
Antwerp, Belgium

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1. Introduction

The unprecedented radiation field and hit rate present at the HL-LHC inner trackers pose a very strong requirement on the front-end electronics. To cope with this challenge, the RD53 collaboration [1] was established across the CMS and ATLAS experiments, dedicated to the development of a pixel readout ASIC. The RD53A [2] is a large-area, full-fledged prototype readout chip (ROC) based on a 65 nm CMOS technology.
The extreme high rate operation of the ROC requires the use of a modern high density low power CMOS technology with low supply voltage (1.2V), resulting in a pixel chip that must be supplied with significant current levels (~400mA/cm^2). The ATLAS and CMS pixel detectors designs contain serial power chains of 3 to 14 pixel modules long with 2 to 4 chips per module connected in parallel. Locally, two Shunt–LDO (Low Drop Output) regulators [3] integrated on the pixel chip are needed to allow serial powering connection. During the last years, extensive studies have shown that a serial power distribution system is the only technically viable scheme (within the present state of the art) to supply the ATLAS and CMS pixel detectors with the required power within an acceptable material budget and power cable losses [4][5].

2. Shunt LDO regulator

While the LDO part is a standard and fast (BW ~1 MHz) voltage regulator, the shunt part is the key of the regulator that has 2 main goals:

- Ensuring constant equivalent input impedance to allow serial connection of chips.
- From input point of view it has a resistive behavior to allow parallel connection with balanced current sharing.

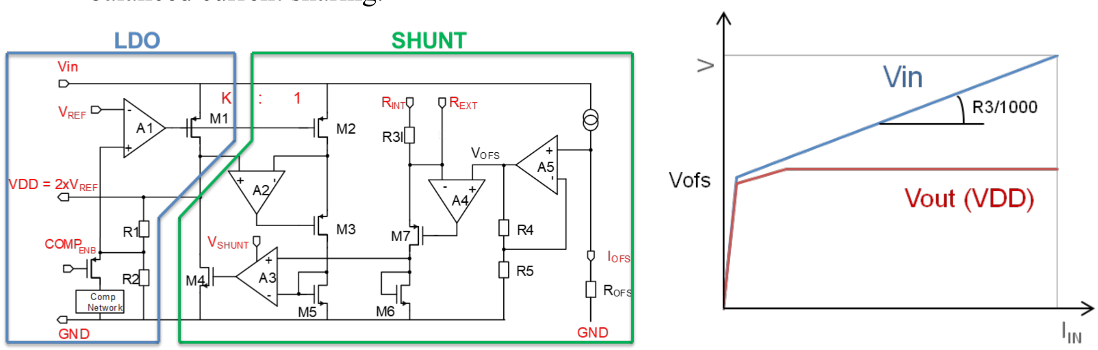

Figure 1: Shunt-LDO simplified circuit and Vin-Iin curve.

The shunt-LDO equivalent circuit (figure 1), from the Vin perspective, is that of a Zener diode (Vofs) in series with a resistor (R3/1000), as shown in figure 1 (right). Both parameters, as well as Vout (VDD), are configurable through external resistors. Finally, two band-gaps are in charge of generating the reference voltages for each SLDO: Vref for the output voltage and Vofs for the offset voltage.

3. Simulation model and measurement set-up

A realistic Cadence Virtuoso model of the SLDO regulator and external components has been used to carry out these studies. The basic model for a single SLDO consists of: SLDO core

(SLDO version implemented on RD53A), decoupling capacitors (needed to assure the stability of the regulator), parasitic components (resistive and inductive elements due to wire-bonds and PCB traces, and on-chip capacitance) and a current source. This basic model is scaled with several SLDO connected in series and parallel for system level analysis.
The main component of the serial powering set-up used for these tests (figure 2) is the RD53A chip mounted on a Single Chip Card (SCC). The chip read-out system (BDAQ53) [6] has been implemented over a commercial Xilinx development board, using an FMC adapter [7] card to be able to connect to the SCC [6]. A current source [7] has been used to power the chip.

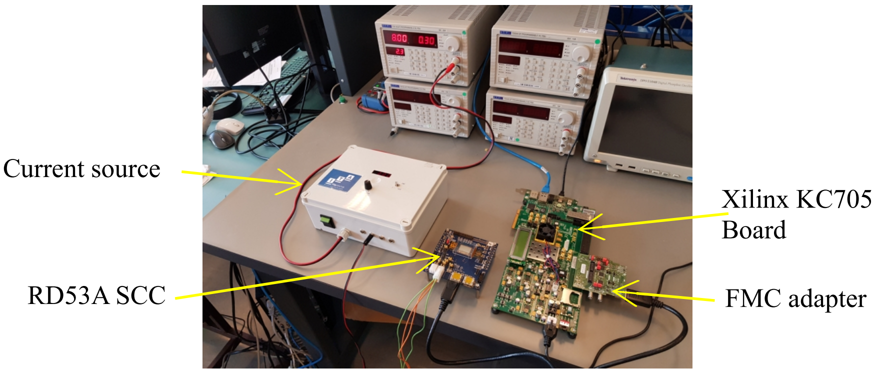

Figure 2: RD53A serial powering test set-up

4. Results

4.1 Dynamic response analysis

In this section, the dynamic response to load changes of the regulator output (Vout) and the effect of parasitic elements on this, are analyzed. Both the simulation model and test system are used. Figure 3 (right) shows the Vout response to load steps of 0.2A→0.8A→0.2A.

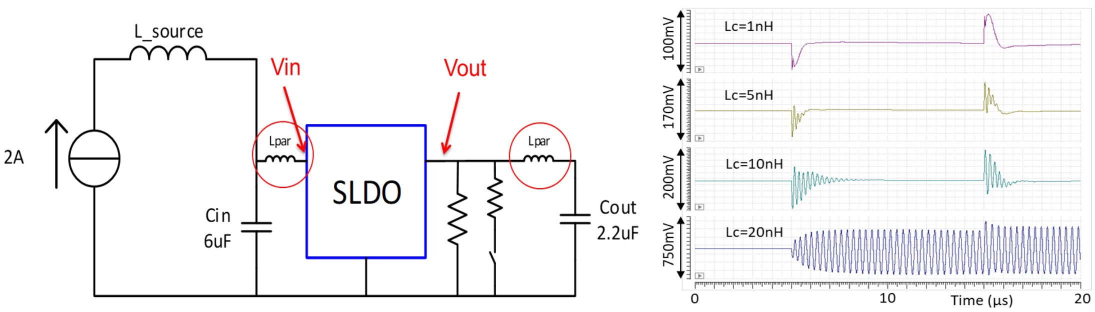

Figure 3: Dynamic response simplified test-bench and results

It shows the impact on the output voltage stability for different values of parasitic inductance between the regulator output and decoupling capacitors. This parasitic inductance that derives from the chip wire-bonding and the PCB routing, is typically in the order of few nH, and will mainly depend on the PCB layout. The simulation confirms that a low inductive connection is essential to ensure the regulator stability, and sets a maximum of ~5nH where the output starts generating high frequency ringing. In Figure 4, simulation and oscilloscope measurements of RD53A chip are shown. Load steps of 0.5A→0.3A→0.5A are generated on-chip by means of enabling and disabling parts of the digital circuitry. These measurements match accurately the simulation of SLDO dynamics, and it can be concluded that the SCC routing is well optimized from parasitic inductance point of view, as there is no high frequency ringing. The plot on the right shows that analog Vout is not affected at all by digital domain transients.

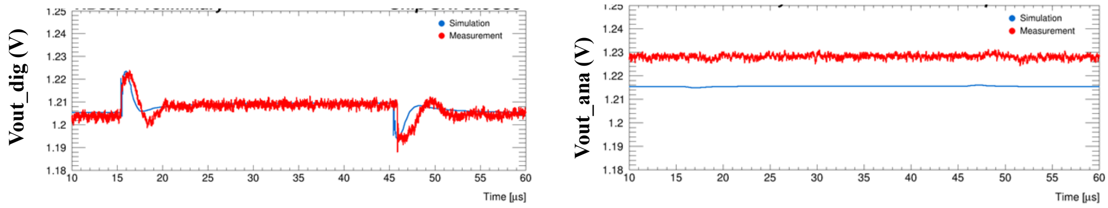

Figure 4: Dynamic response of digital and analog SLDO output to a digital load transient

4.2 Start-up

The main issue during power-up of the RD53A SLDO is related with the band-gaps minimum voltage and current needed to start-up (figure 5). This effect can be observed in the V-I curves of both simulation and measurement.

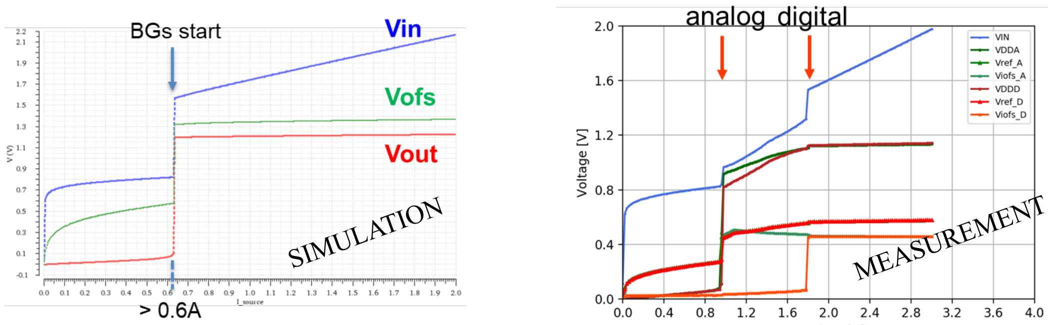

Figure 5: Band-gaps start-up issue simulation and measurement

In the simulation plot, it can be seen that a minimum current of 0.6A is needed to set Vofs. On RD53A measurements, where there are 2 SLDOs in parallel, analog and digital, the same issue is observed. Furthermore, there is a high variability on start-up behavior between different SLDO, which can generate current sharing distribution issues during start-up. This behavior is being solved in the next SLDO version using a new band-gap scheme.

4.3 Transient propagation on a serial chain

A simulation model including two SLDOs in series is used to analyze the propagation of digital load transients to the rest of the chain (figure 6). Realistic load model from digital simulations is applied in one of them (Vout2), and the effect is monitored on Iin and Vout1 of the other SLDO. A serial powered system needs constant current, and there are two options to obtain this: a current source or a voltage source controlled in current. A comparison of them has been done:

- In case of using a current source, transients on input current are completely filtered by the inductive output filter, therefore there is not effect on Iin or Vout of the other SLDO (this plots are not shown as there is no effect at all)
- In case of using a voltage source, the propagation of a transient will depend on the power cable parasitic inductance that is going to filter the transients. For long cables, the voltage source behaves very similar to a current source.

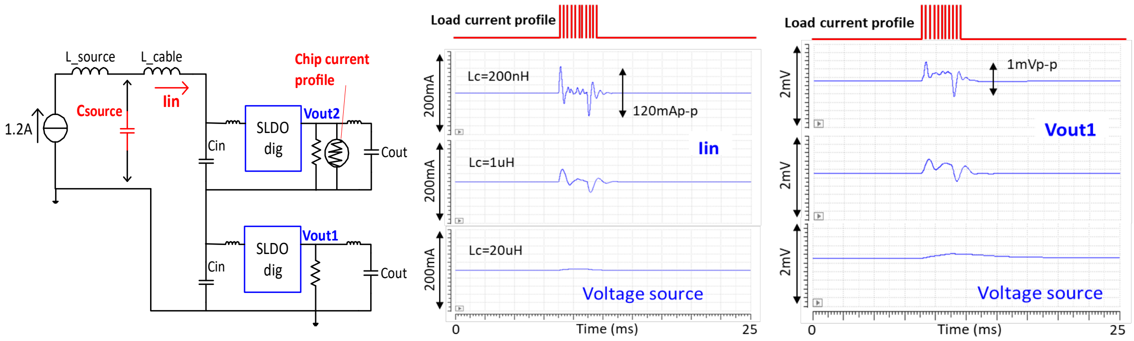

Figure 6: Simulation of transients propagation

The worst case shown on figure 6 is Lc=200nH (~2m of low inductive cable), where a 10% transient is propagated to the Iin due to the load transient. However this 10% on input current is translated into ~0.1% on Vout1, which is negligible. Due to the decoupling capacitors and the fast regulation of the LDO, the SLDO presents a very consistent PSRR (Power Supply Rejection Ratio).

5. Conclusions

Serial powering has proven to be very stable and reliable in all tests. Due to local regulation and decoupling, load transients are not propagated to the rest of the system. Parasitic inductance won't be a problem if it is taken into account during PCB or HDI design. Cable impedance, unlike in classical parallel systems, where it can be problematic, does not affect serial powering. SLDO has some known issues that are already fixed or being fixed for next chip submission: band-gap circuits have been improved with a new references scheme, and a dedicated start-up circuit, that allows low-current power-up, is being developed.
Simulation models reproduce SLDO behavior quite accurately at both local and system level. Serial power simulations of multiple chips in parallel and multiple of these in series have also been done and have been found to behave well (very similar to small scale model).
Testing of multiple chips in parallel and in serial is currently ongoing and so far seems to work well, and extended serial powering and EMC testing will be performed in the following months.

References

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