PROCEEDINGS OF SCIENCE

The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

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Electronics developments that will be implemented during the Phase-I upgrade scheduled in the LHC shutdown period of 2019-2020 have been pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter, which measures the energy of particles. The LAr Trigger Digitizer system, part of the frontend of the calorimeter readout electronics, digitizes 34000 channels at a 40 MHz sampling rate with 12 bit precision after bipolar shaping and transmits the signal to the LAr Digital Processing system off-detector to extract the transverse energies. Results of ASIC developments including QA and radiation hardness evaluations, performance of the final prototypes and results of the system integration tests will be presented along with the overall system design.

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1. Introduction

The ATLAS detector at the LHC, shown in Figure 1, is a multi-purpose detector with cylindrical geometry. It was designed in order to study elementary particles and their interactions and to search for new physics. It consists of several sub-detectors. ATLAS Liquid Argon (LAr) Calorimeter is one of those and its purpose is to measure the energy, position and shower shape of electrons and photons. A sampling calorimeter with accordion shape was adopted for the design.

The LHC Run 2 was started in 2015. A long shutdown (2019-2020) is planned before Run 3 planned from 2021 to 2023. Run 3 is expected to have two times higher instantaneous luminosity, $L = 3.0 \times 10^{34}$ cm $^{-2}$s^{-1} than in Run 2. The upgrade of some sub-detectors is planned for the long shutdown, referred to as the ATLAS Phase-I upgrade project. For the LAr calorimeter, a trigger readout upgrade will be done in order to improve the first level trigger (Level1) performance.

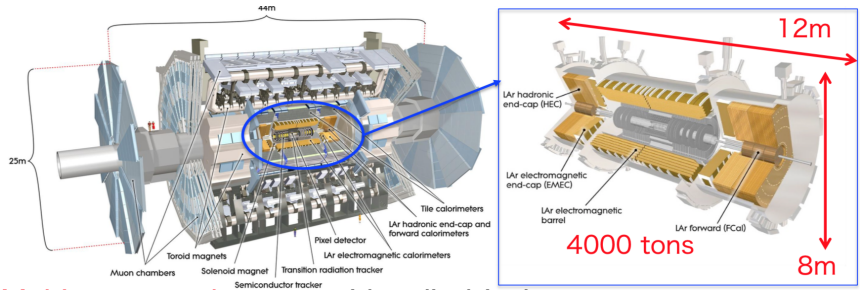

Figure 1: LHC ATLAS detector (left) and ATLAS Liquid Argon (LAr) Calorimeter (right) [1]

2. ATLAS LAr Phase-I upgrade project

The LAr calorimeter has four layers, called layer 0, 1, 2, 3, which are segmented in pseudo-rapidity η and azimuth ϕ directions. The left figure in Figure 2 shows the current trigger readout, where the unit of the readout segment is called a "Trigger Tower". The readout makes analog sums over cells of the 4 layers in a range of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ at the frontend electronics. The summed analog signals are transmitted via coaxial cables to the backend electronics, which digitizes at 40 MHz. The right figure in Figure 2 shows the new trigger readout, with the new "Super Cells". The summed analog signals are digitized for each layer separately in the frontend electronics and transmitted to the backend electronics via optical fibers. In addition, the range of the summation for the first and second layers is changed to be finer, $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$. The number of sums readout is ten in one $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ region.

In order to improve the readout, two new hardware upgrades are introduced as shown in Figure 3. One is the front-end LAr Trigger Digitizer Board (LTDB), whose main role is to digitize the Super Cell information on 12 bits at 40 MHz and transmit it into the backend electronics via optical links. The other is the backend electronics LAr Digital Processing Board (LDPB). The main role of the LDPB is to compute each transverse energy E_T and the bunch crossing at which the pulse is injected and transmit this information into the Level1 system via optical links.

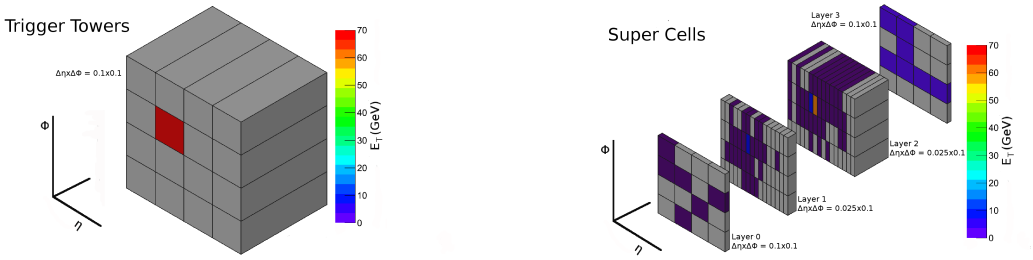

Figure 2: Comparison of the current trigger readout (Trigger Tower) and new trigger readout (Super Cells). Colors indicate the energy deposit in case a 70 GeV electron. [2]

Figure 3: The introduced two new boards. The left figure is LAr Trigger Digitizer Board (LTDB). The right figure is LAr Digital Processing Board (LDPB) [2]

2.1 Frontend electronics: LTDB

Figure 4 shows a schematic of LTDB, which transmits at most 320 Super Cells. The analog signals are digitized with 12 bits at 40 MHz using an analog-to-digital converter (ADC). This is done by a custom ASIC, the Nevis15 ADC. Then, the ADC data is serialized for several Super Cells and transmitted into the backend system. These functions are performed by custom ASICs, the LOCx2 chip and LOCId chip. In addition to these ASICs, 5 GigaBit Transceiver (GBT) links are used to provide LHC clock and Timing, Trigger Control information (TTC).

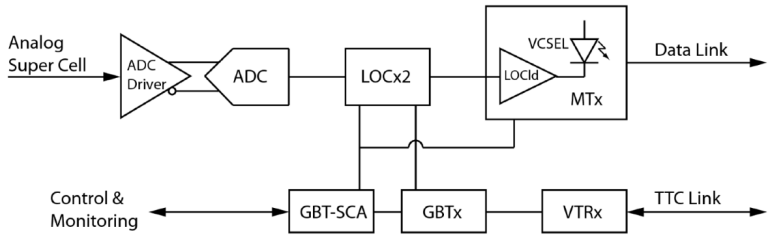

Figure 4: The schematic of the LTDB [2]

These electronics are on the detector, so they must be radiation-tolerant. The radiation tolerance requirement is that any electronics component should be stably functional after receiving 100 kRad of total dose [2], and pass the single event effect (SEE) tests with total fluency of 3.8×10^{12} hour / cm^2 [2]. The custom-made ASICs are designed in order to satisfy with this requirement.

2.1.1 Nevis15 ADC

The Nevis15 ADC shown in Figure 5 is based on a 130 nm CMOS technology of 3.6 mm $\times$ 3.6 mm in a package with 72 quad-flat no leads (QFN) pins [3]. The power consumption is less than 50 mW per channel, the latency is less than 200 ns and the dynamic range is larger than 11 bits. A radiation test was performed using components from the engineering production. These devices worked well up to 10 Mrad, with an observed SEE cross section of 10^{-12} cm^2 per channel.

2.1.2 LOCx2 and LOCId chip

Figure 6 shows the LOCx2, a 8$\times$14 dual channel ASIC that transmits serial data at 5.12 Gbps. The LOCId is a dual channel VCSEL driver. Both chips use a 250 nm silicon-on-sapphire technology. The radiation tests of these chips are also performed and established up to 200 kRad. The shape of the eye diagram in the optical data transmission test after irradiation are almost same as before the radiation, and is within the required specification.

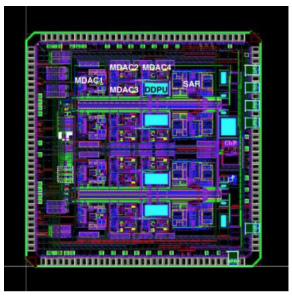

Figure 5: NevisADC [3]

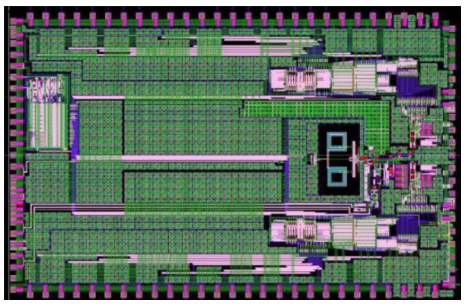

Figure 6: LOCx2 [4]

2.2 Backend electronics: LDPB

The LDPB is designed with the Advanced-TCA (ATCA) architecture and consists of two boards. One is the Advanced Mezzanine Card, the LATOME. The other is the ATCA carrier blade (LArC) with the RTM card. An LDPB consists of one LArC equipped with four LATOMEs. For Run3, a total of 124 LATOMEs and 31 LArCs are needed.

2.2.1 LATOME and LArC

Figure 7 shows the final version of LATOME. It has 48 links with 5.12 Gbps per link from the LTDB and 48 links with 11.2 Gbps to the Level1 trigger system. These data flows are the main stream for the Level1 trigger path. This high speed transmission is performed with 8 microPODs. All high speed links are connected to an Intel Arria10 FPGA, which computes transverse energy and the bunch crossing for all Super Cells. The PCB of the LATOME has 16 layers with a thickness of 1.6 mm. Figure 8 shows the final version of LArC. It provides LATOME's power, system clock, control signals and monitors the data transfer. The power consumption per each LATOME should be less than 80 W, therefore the LArC has capability to supply power up to 400 W per board.

A performance test was done in order to verify the hardware capabilities. As the result, LArC can provide the full load of power to four LATOME boards up to 80 W, and there is the voltage drop within tolerances on supplied voltage at the LATOME as shown in Figure 9. The data transmission

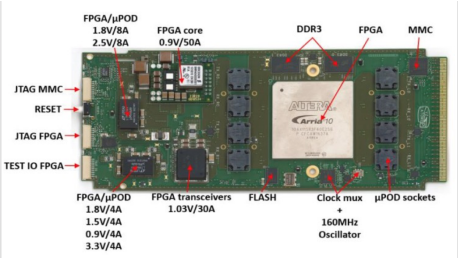

Figure 7: LATOME [2]

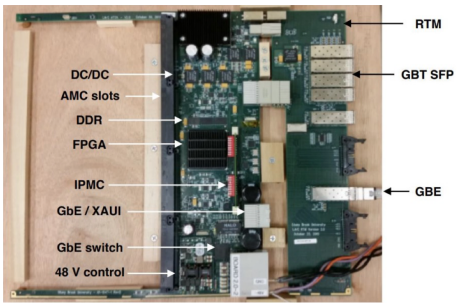

Figure 8: LAr Carrier blade [2]

from the LATOMEs and Level1 trigger system has also tested. All fibers have the bit error rate less than 10^{-14} with a data transfer speed of 11.2 Gbps.

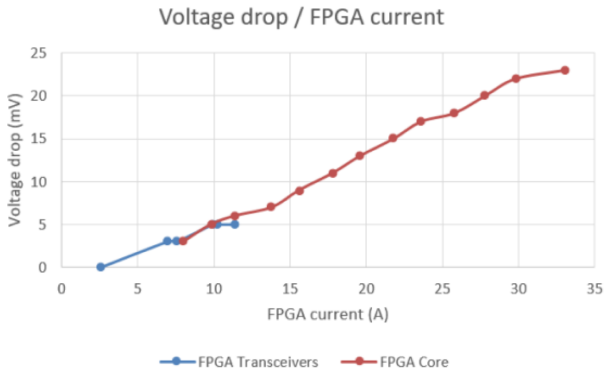

Figure 9: Voltage drop on the FPGA as a function of current load

3. Summary

New frontend and backend electronics in the ATLAS LAr Calorimeter will be introduced to increase readout granularity and precision in order to keep trigger rates at a manageable level in the Run 3 environment. For the frontend electronics, the radiation tolerant custom ASICs have been designed and tested. For the backend electronics, highend FPGAs for computing E_T with the correct bunch crossing are used. The power and data transmission tests show the hardware meets the specifications.

References

[1] ATLAS Collaboration, JINST 3 S08003 (2008)

[2] ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report, ATLAS Collaboration, CERN-LHCC-2013-017, ATLAS-TDR-022, https://cds.cern.ch/record/1602230

[3] A radiation-hard dual-channel 12-bit 40 MS/s ADC prototype for the ATLAS liquid argon calorimeter readout electronics upgrade at the CERN LHC, J. Kuppambatti, et. al., Nucl. Inst. and Meth.A 855 38

[4] LOCx2, a low-latency, low-overhead, 2×5.12-Gbps transmitter ASIC for the ATLAS Liquid Argon Calorimeter trigger upgrade, L. Xiao, et.al., JINST 11 C02013