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Status of the Readout Electronics for the Triple-GEM Detectors of the CMS GE1/1 System and Performance of the Slice Test in the 2017-18 LHC Run

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In this contribution, we will present the status of the readout electronics system for the triple-GEM detectors of the GE1/1 system, an upgrade which is planned for installation into the CMS experiment during the next LHC long shutdown (LS2) in 2019-2020. We will also report on the performance of the ten slice test detectors which have been present in the CMS muon endcap since the 2017 LHC run, which represent the first time that such large triple-GEM detectors have been operated within the LHC environment, and on the first results from the v3 slice test detectors that were added to the slice test in March 2018.

Ten slice test detectors were installed into the CMS muon endcap in January 2017. Data was recorded throughout the 2017-2018 run, using both cosmic ray muons and LHC collisions. Using the lessons learnt from this slice test allowed for the development of the final GE1/1 v3 electronics which will be used on the production chambers to be installed during LS2. These new detectors will be read out on the front-end by 24 VFAT3 chips, which runs at 320 MHz, four times higher than the frequency of the VFAT2 chip, as well as the v3 optohybrid (OH) board. The VFAT3 chips communicate with the OH through a 1m-long PCB, called the GEM electronics board (GEB), which has been re-designed to accommodate the faster VFAT3 digital signals. The on-detector electronics are powered via ten FEAST DC-DC converters. Optical communication to the back-end, which includes a microTCA crate containing CTP7 and AMC13 boards, is based on the CERN Versatile link, including GBT and SCA chips as well as VTRx and VTTx optical modules. Production and qualification of the v3 GE1/1 detectors is currently ongoing.

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1. Introduction

The GE1/1 project takes place in the context of the CMS endcap muon system, and details on the project, including its goals and purpose, can be found within Ref. [1]. The GE1/1 system will consist of 144 triple gas electron multiplier (GEM) detectors, which are gaseous particle detectors which have been used for many years across many experiments. In the case of the CMS GE1/1 GEMs, the gas mixture used is composed of 70% Ar, 30% CO_2, for an optimal balance between gas gain, drift velocity, and discharge suppression. More details on the triple-GEM detectors designed for the GE1/1 project can be found in Ref. [2].

As a proof of concept, 10 detectors were installed on the CMS YE-1 endcap in what is known as the *slice test*, details on which can be found in Ref. [3]. As of 2018, eight of the slice test detectors are outfitted with version 2 (v2) electronics, and two are version 3 (v3). Details on the different electronics versions and the results of the slice test will be discussed in this paper.

2. v3 Electronics

The v3 electronics sees many changes from the v2 electronics, several of which were made as a result of the experience gained from the slice test operation. The v3 set-up, and the differences between v3 and v2, can be found in Figure 1. In both versions, the detectors are read out by 24 front-end binary very forward ATLAS and TOTEM (VFAT) chips, with v2 read out by the VFAT2 chip and v3 read out by the VFAT3 chip. Each version communicates through a long PCB called the GEM electronics board (GEB) to a small FPGA-based mezzanine card called the Optohybrid (OH). From there, the front-end electronics communicate with the μTCA-based back-end electronics through optical fibers. The differences between v2 and v3 will be discussed.

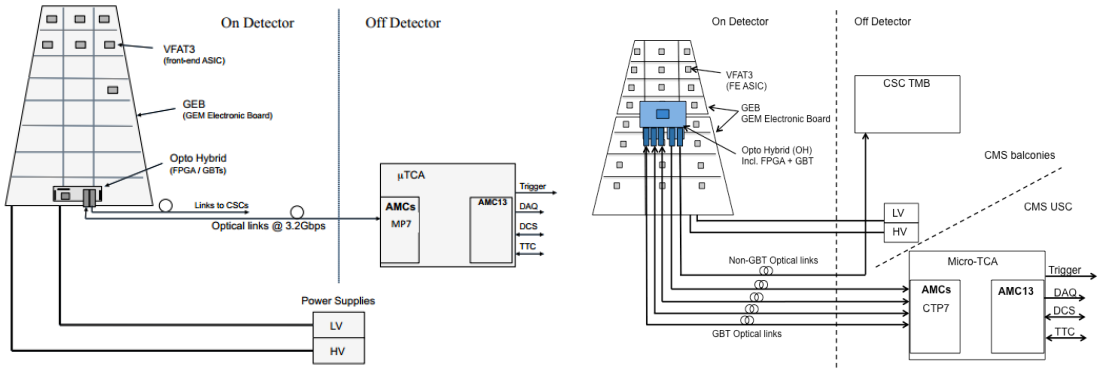

Figure 1: Side-by-side comparison of v2 (left) and v3 (right) electronics systems

2.1 The GEM Electronics Board (GEB)

In the v3 electronics, the GEB is split into two PCBs. This choice was made in part due to the fact that the 1m-long multilayer board of v2 was at the limit of commercial manufacturers' capabilities. A further consideration which led to this choice was concerns over signal integrity and dispersion of the LVDS clock at the VFAT3 operating frequency of 320MHz. Previously, long track lengths had been seen to cause reflections and distortions of the square signal. By splitting the GEB into two smaller boards with the optohybrid located at the center joint, the tracks are shortened, and signal integrity is improved in a simple manner.

Due to the existing mechanical constraints within CMS, the GEB is limited to a thickness

of ~1mm, which limits the possible layers to one power plane, one ground plane, two signal layers, and one shield layer. The shield layer between the GEB signal line and the readout board in v3 was added after experience from the slice test proved it to be necessary in order to reduce noise.

2.2 Front-End ASIC: VFATs

As in v2, in v3 the GEB and readout board are split into 24 sectors, each of which is routed to a VFAT chip, seen in Figure 2. Both VFAT versions send trigger and tracking data. The lower-granularity trigger data are sent at each LHC bunch crossing, while the full-granularity tracking data are sent only upon receipt of a CMS level-1 accept (L1A) signal. Due to the increased trigger rate beginning in LHC Run 3, CMS systems are required to cope with L1A rates of up to 1MHz. Whereas the VFAT2 could only cope with rates up to 100kHz, the VFAT3 operates at the 40 MHz frequency of the LHC collisions, derived from a clock running at 320 MHz, four times the frequency of the VFAT2 [2,4]. By using both edges of this clock, the VFAT3 chips can provide full-granularity trigger data in double data rate (DDR) mode for offline muon reconstruction.

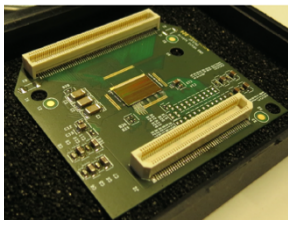

Figure 2: VFAT3

Whereas the VFAT2 had a fixed shaping time of 25ns that led to a ballistic deficit as a result of being shorter in duration than the signal of O(10ns), the VFAT3 has a programmable shaping time so it can integrate all of the signal charge, resulting in a higher signal-to-noise ratio than the VFAT2. And while the VFAT2 was designed to have an L1A latency of 3.2μs and a maximum programmable latency of 6.4μs, the VFAT3 has a latency of up to 25.6μs [2].

2.3 Optohybrid (OH) Mezzanine Card

Whereas the OH card was located at the wide end of the GEB in v2, in v3 the OH is moved to the center, attached to both halves of the GEB. As seen in Figure 3, the main features of this card are a Xilinx Virtex-6 FPGA and three GBTX chips [5]. Unlike in v2, the v3 OH does not require a PROM, allowing for programming of the FPGA directly from the calorimeter trigger processing (CTP7) card [6] in 70ms without reliance on a commercial component with known radiation failures.

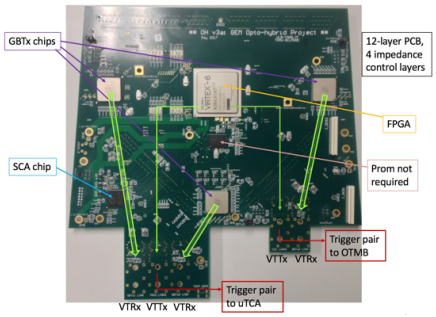

Figure 3: v3 optohybrid

2.4 Gigabit Bidirectional Triggers (GBTXs)

In v3 electronics, the GBTXs are responsible for the transmission of tracking and slow control data. They drive communication through bidirectional optical links to and from the back-end electronics [7]. One of the GBTXs is also coupled to a slow control ASIC (SCA). Through the SCA, the FPGA can be programmed from the CTP7 card, resets can be sent to the VFAT3 chips and other front-end electronics, and temperatures and voltages can be read.

We have chosen to minimally fuse the GBTXs such that they lock to the fiber link, recover the clock, and keep a certain configuration after power loss or other issues, where the presence of a GBTX watchdog prevents broken link and communication errors after a clock change. It is reset at power-on, controls the initialization procedure, and continuously monitors the GBTXs. In the case of a major link failure, it reinitializes the link automatically, without any needed input from

the detector operator. However, the watchdog was found to be non-functional on several previous OHs as far back as the GBTX v1 chip, where not all the fused GBTXs would lock to the fiber link. Because of this, the watchdog was not enabled on the GBTX chips used in the v2 slice test detectors, which made a manual power cycle necessary after every LHC clock change.

The cause of this watchdog failure was found to be twofold. For one, the power-on reset was removed too soon, prior to the GBTX power reaching a stable value. For another, the GBTX decoupling capacitance was too small. Both issues were solved by adding capacitors, increasing the time constant of the RC circuit and increasing the decoupling capacitance from 10μF to 47μF.

2.5 FPGA

In v3, the OH FPGA only transmits trigger data, since the GBTXs handle the tracking and slow control data. This is the same FPGA that was used in the slice test chambers and the CSC ME1/1 chambers, and so has been well-tested within CMS. The trigger data is transmitted through a dedicated link to the CSC trigger motherboard (TMB) and a GEM back-end trigger link.

3. First v3 Slice Test Results

Figure 4 shows the S-curves recorded from the 24 VFAT chips on two slice test detectors – one v2, one v3. Each plot illustrates the response of a given VFAT chip to the injection of internal calibration pulses by showing the probability that the calibration pulse is above a fixed threshold, as a function of the calibration pulse charge (y-axis) and for each VFAT channel (x-axis). More information can be found in Ref. [3]. The first v3 slice test S-curves are promising, being less noisy and more uniform than their v2 predecessors. However, VFAT position 5 was found to be non-functional on both v3 slice test detectors, as evidenced by the lack of S-curves in that position.

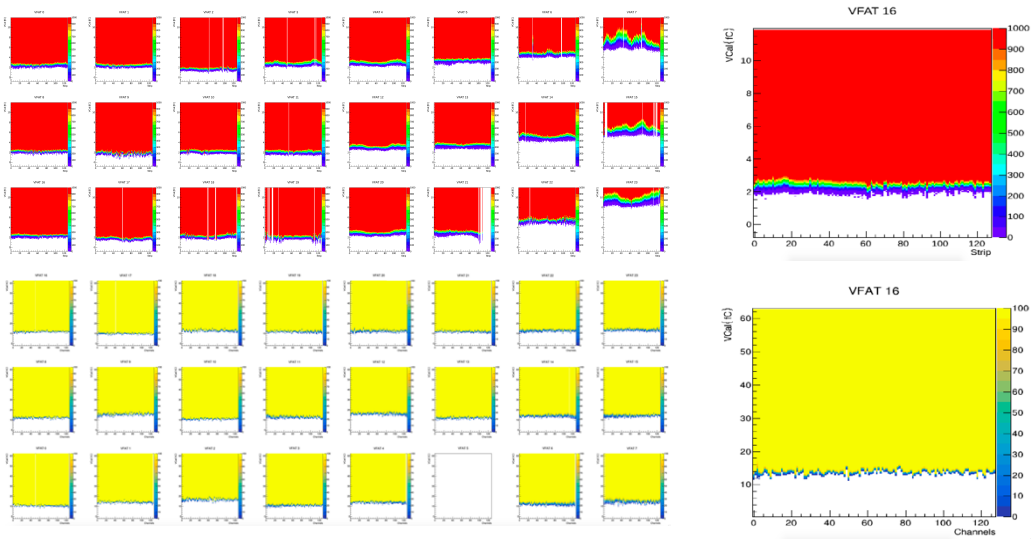

Figure 4: S-curves for v2 (top) and v3 (bottom) slice test detectors, with examples (right).

The reason for this was determined to be a mismatch in track length which prevented good communication with the optohybrid. The design of the GEB has since been changed to prevent this issue from happening in the final GE1/1 detectors by shortening the track length.

Despite this issue and the short period in which they have been inside CMS, the v3 detectors have successfully collected collision data. Figure 5 (right) shows the VFAT3 trigger data recorded

within CMS as a function of the VFAT3 threshold. The blue curve was recorded without detector gain, and therefore shows the electronics noise contribution. The red and green curves show the trigger data rates due to real particles. Detailed analysis of the slice test data is currently ongoing.

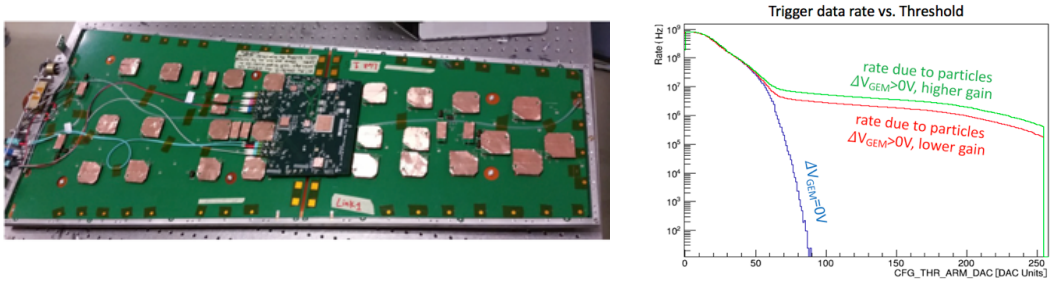

Figure 5: Fully-assembled v3 slice test chamber (left), and first LHC collision results from it (right).

4. VFAT Channel Stability and Loss

Over the entire 2018 LHC run, there is an overall loss rate of approximately 0.5% of channels per month for the v2 detectors, excluding one of the ten detectors which has shown anomalous behavior that does not manifest in the other nine detectors. These lost channels manifest themselves in time-series S-curve plots as having an abnormally low noise level of between 0.0414 and 0.109 fC. This channel loss has been preliminarily attributed to burn damage to the VFAT ASIC inputs as a result of discharges reaching the anode of the detector. Detailed studies are in progress, and mitigation strategies are being investivated to prevent damage to the ASIC, focusing on possible changes to electronics design, detector design, and detector operation.

5. Conclusion

Many changes were made to the GEM front-end electronics to allow for the required performance of GE1/1. The slice test proved invaluable in this regard, allowing us to identify problems such as channel loss and track length mismatches before the full production began.

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