PROCEEDINGS OF SCIENCE

The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment

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For the ATLAS experiment a new Silicon tracker is necessary for the High-Luminosity Upgrade of the LHC. The main building block for the strip tracker is a module which consists of a silicon sensor, readout ASICs and a hybrid PCB. Up to 28 modules are placed on long substructures. An End-of-Substructure (EoS) card provides common connections for data, commands and power to the off-detector systems. Prototypes has been developed based on the GBTx and GBT-SCA chip family and SFP+ optical links to understand the design issues, the behavior of the EoS and the detector level integration. Presented will be the design of the electronics, the exercised tests for electrical behavior, mechanical deformation and thermal behavior.

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1. Introduction

The High-Luminosity upgrade for the Large Hadron Collider (HL-LHC) will present a very challenging environment for the ATLAS detector. To cope with this, the ATLAS inner tracker (ITk) will be upgraded with a new silicon tracker, consisting of the pixel detector close to the interaction point and the strip tracker surrounding it.

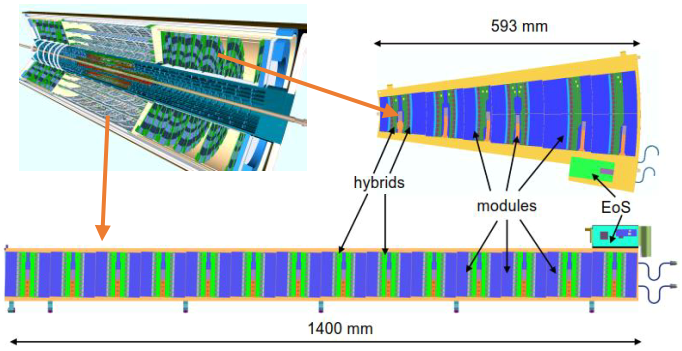


Figure 1: The location of the EoS card.

The strip tracker[1] consists of two geometries, the barrel, built from "staves", and the two endcaps, built from "petals". At the end of each stave or petal, there is an End-of-Substructure (EoS) card placed on each side of the "ear" of the carbon-fiber structure (Fig. 1), one side is the so-called master and the other the slave version. The EoS cards act as the interface between the on-detector modules of the corresponding stave or petal side and the off-detector components handling data, command, and power delivery.

1.1 The End-of-Substructure Card

The major active components of the EoS card are developed by CERN as radiation-hard ASICs. At the heart, up to two low-power Gigabit Transceiver (lpGBT) ASICs provide clock and control data for the front-end ASICs on the downstream and up to 28 "Elinks" for the upstream data each running at 640 Mbit/s. The bi-directional optical link (VL+) connects the EoS with the off-detector systems at 10 Gbit/s links. Additionally, there are two DCDC converters on the EoS, providing 1.2 V and 2.5 V for the lpGBT and VL+, respectively. These, along with other passive components, are populated on an industrial-standard multilayer PCB - the EoS cards.

The detector design and assembly requires the total thickness of the EoS to be less than 5 mm. On the other hand, there must be sufficient spacing between the high speed signals to limit the cross talk. After balancing the two requirements, the EoS PCB was designed to have twelve layers with a nominal thickness of 1.6 mm and a 1.8 mm maximum allowance. This makes it possible to fit every components within 5 mm after population but contains two inner impedance controlled 100 Ω layers and two high capacitance power-ground structures. Even if they are thick, the impedance control layers have to be inner layers because the lower layer will be glued to a conductive carbon-fiber structure. One exception is the DCDC converter, which has to follow a strict guideline developed by CERN DCDC

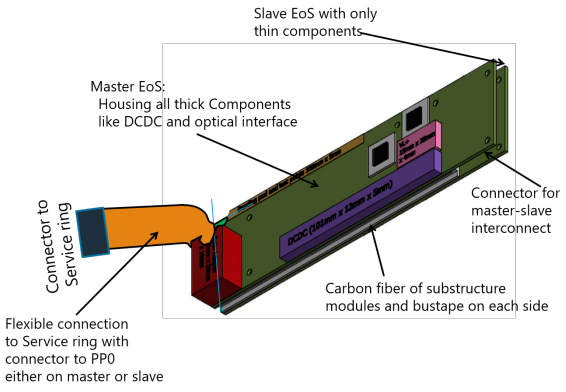


Figure 2: A 3D drawing of the EoS card.

converter team and will exceed the 5 mm limit when combined with a 1.6 mm PCB. To overcome this issue, the DCDC converter module will be developed separately using a simpler and thinner PCB design, and the EoS board will have a cutout in the PCB for its placement (See Figure 3). The 0.5 mm pitch ball-grid-area of the lpGBT is connected by two micro-via layers and buried vias.

The 5 mm limit on the PCB thickness also implies that there is no easy way to place a common connector for external power and monitoring on the main part of the EoS. Therefore a flexible part of the PCB has been added to connect to a separated stiff part that host these connectors. This makes it possible to locate the connectors for external cables where there is more space, easing the mechanical integration for the full tracker. An additional high density connector is introduced between master and slave to collect all signals from one EoS region into one external connector to cope with space and cabling requirements.

The EoS-cards will be designed in ten variants as a compromise between easier adjustments of a PCB design than general mechanical constrains and design, manufacturing quality control issues of more variants with lower production volumes. These variants cover master and slave, mirrored versions, different flex-lead connections and versions for 14 and 28 upstream Elinks. All tall components, specially the DCDC converters, will be located on the master side and signals guided through the interconnection of master and slave, to allow the slave side in most regions to be designed even thinner than 3 mm.

2. Prototypes

The lpGBT, VL+, and DCDC converter are still in development. To learn about the implementation of both hardware and software, we have built several prototypes using available components. Instead of the lpGBT, we used its predecessors GBTx[2] and GBT-SCA. They are the gigabit transceiver and dedicated slow-control ASIC, respectively. The VL+ is replaced with the small form-factor pluggable (SFP+). The 1.2 V and 2.5 V are supplied using a commercial DC power supply.

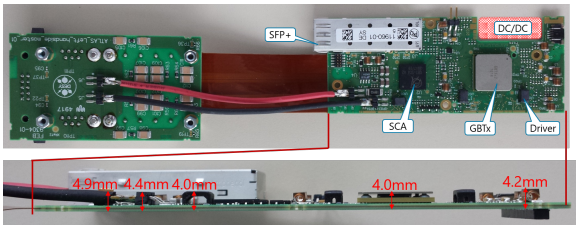


Figure 3: Master prototype of EoS

We have used CERN's reference design for GBTx and GBT-SCA implementation, the VLDB, as a starting point for both hardware design and software development. GBTx-based prototypes for masters and slaves has been developed (Fig. 3) in two iterations. Minor faults were identified in version 0 and have been fixed. The latest version 1 has no outstanding issue. All components except the SFP+ fulfill the height requirement. They can be reused including the circuit around for the final design. The SFP+ will be replaced by the specially developed VL+ device.

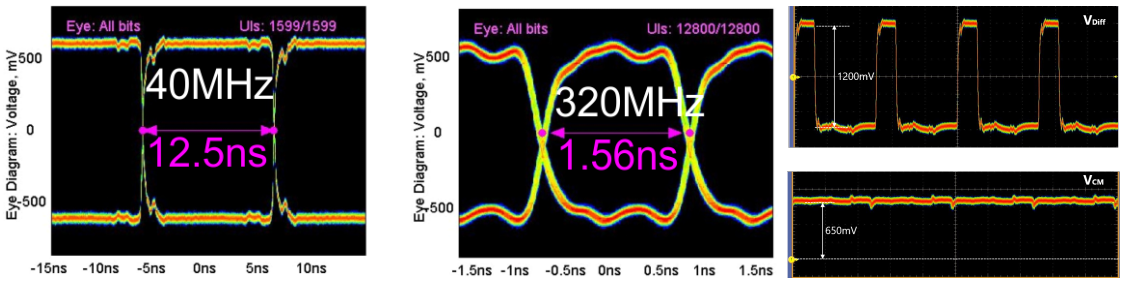
3. Test Results

3.1 Functionality Tests

The first set of tests are the basic property tests. We tested the isolation of the high-voltage (HV) lines, the line resistor of the low-voltage (LV), HV, and thermistor (NTC) lines. The electrical

strength and the residual current of the HV lines were tested at 1.5 kV for 60 seconds. The current on the LV lines had been checked. No issues were found on either master or slave prototypes.

The next step is to test the functionality of the active components. For that, the optical connection has to be established. A firmware for Xilinx KC705 FPGA board and an accompanying PC software to configure, read, and write to both GBTx and GBT-SCA had been developed. The GBT-SCA had been tested; we can read the unique ID, as well as controlling the I^2C bus, general purpose input/output, ADC, and DAC on the chip. The clock and Elink signals from GBTx had been measured. The eye diagrams show open eyes, and the signal quality is good, as seen in Fig. 4.



(a) Clock at lowest and highest frequencies

(b) Elink: Differential and common mode for repetitive pattern "0001" at 160 Mbit/s

Figure 4: Output signals from the EoS.

3.2 Thermal and Flatness Tests

Preliminary thermal and flatness tests can help identify any potential cooling issue. The thermal measurement was done without active cooling using an infrared camera. The EoS was put in front of a mirror so both side can be measured simultaneously. However, this implies that the results for the front side will be off by a certain number (the exact number is not necessary for our current needs). The GBTx warmed up quickly after powered on and the PCB was shown to be a good heat spreader. These results show no problem for the EoS or the ATLAS design.

The flatness measurements showed that both EoS prototypes are a bit thinner (up to $\sim 100\,\mu$m) at the corners, most likely due to the lack of copper in the PCB for those regions. This is, however,

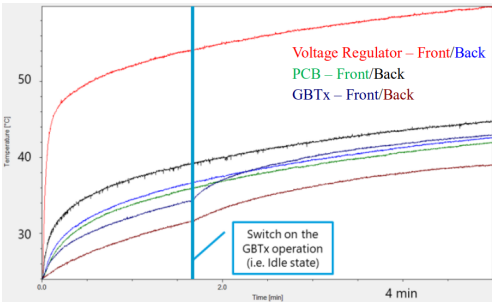


Figure 5: Infrared measurement of the EoS prototype. The lines represent various part of the board.

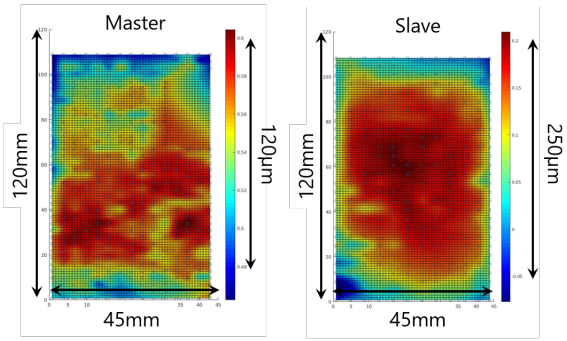


Figure 6: Flatness measurement of the master (left) and slave (right) EoS prototype.

within the specification (maximum of 200 μm over the nominal thickness) and not a problem for cooling of the EoS.

3.3 Bit Error Rate (BER) Test

Preliminary BER tests with ad-hoc setup had been done with a data path like what would be in a real system; the data went from the FPGA passing through the Elink, over the optical link, and back to the FPGA. Many configurations have been tested: 160 or 320 Mbit/s, all or only the Elink under test on, with or without a metal case around the EoS, with or without twisting the power cable, and with a prototype DCDC converter or regular power supply. All configurations were able to run error-free for more than 15 hours (BER $< 10^{-13}$). Two extended runs for 70 hours also had been run error-free. These results are already better than our BER $< 10^{-12}$ goal, and we expected even better results with a dedicated BER test setup.

3.4 EoS Running with a Real Stave

An EoS master prototype had been assembled together with a real stave built from two full electrical modules at the ends and eleven mechanical modules in between by our colleagues at Rutherford Appleton Laboratory. The LV/HV lines and connections to negative temperature coefficient (NTP) thermistor pipe were tested. Configurations and readout of all modules were done successfully through the EoS. The noise measurements are consistent with the result without the EoS. In short, the EoS worked as designed.

4. Conclusion

We built EoS prototypes as a proof-of-concept that our design can meet the constrains from detector design and integration, and to learn how to implement, connect, and control them. Functionality tests had been done to ensure they are built correctly. Thermal, flatness, and BER test results showed that our prototypes are within the specification. One of the boards had been used with a stave prototype and was shown to work well.

New EoS designs with lpGBT and VL+ based are made according to the current information about them. Still, a lot of information is missing and the 640 Mbit/s Elink in the lpGBT is an unknown territory. However, using experience from these prototypes, we plan for tests needed to quickly detect and react to issues in the future productions.

Acknowledgement

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References

[1] ATLAS Collaboration, "Technical Design Report for the ATLAS Inner Tracker Strip Detector," CERN-LHCC-2017-005, ATLAS-TDR-025.

[2] The GBT Project, "GBTx Manual," http://cern.ch/proj-gbt.