Design of a HVCMOS pixel sensor ASIC with on-chip readout electronics for ATLAS ITk upgrade

Mridula Prathapan[*][b][†] **, Pierre Barrillon**[a] **, Mathieu Benoit**[f] **, Raimon Casanova**[e] **, Felix Ehrler**[b] **, Patrick Pangaud**[a] **, Sourav Pusti**[d] **, Rudolf Schimassek**[b] **, Eva Vilella**[g] **, Alena Weber**[c,b] **, Winnie Wong**[f] **, Hui Zhang**[b] **, Ivan Perić**[b]

[a] *Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France*

[b] *ASIC and Detector Laboratory, Karlsruhe Institute of Technology, Germany*

[c] *Physikalisches Institut, University Heidelberg, Germany*

[d] *Department of Physics, IIT Bombay, India*

[e] *IFAE Institute for High Energy Physics, Barcelona, Spain*

[f] *Department of nuclear physics, University of Geneva, Switzerland*

[g] *Department of Physics, University of Liverpool, UK*

E-mail: mridula.prathapan@kit.edu, ivan.peric@kit.edu

ATLASpix is a series of monolithic High Voltage CMOS (HVCMOS) sensor chips that are engineered to meet the requirements of outer layers of ATLAS ITk pixel tracker for HL-LHC upgrade. They are large collection electrode designs on high resistive wafers to ensure high detection efficiency and radiation tolerance. The readout electronics are placed on the chip periphery. ATLASpix1_M2 prototype is fabricated in a commercial 180 nm CMOS technology and has an active area of 1.6 cm $\times$ 0.33 cm. No clock signals are propagated inside the pixel matrix reducing the crosstalk and helping to achieve an estimated power consumption of 300 mW/cm^2. This work presents the design of ATLASpix_M2 with emphasis on its readout electronics, together with some experimental results.

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[*]Speaker.

1. Introduction

High Voltage CMOS (HVCMOS) sensor chips could be the building blocks of the proposed CMOS quad module which is a low cost alternative to hybrid modules for ATLAS Inner Tracker (ITk) upgrade. The HVCMOS designs are targeted to meet the specifications [1] of ATLAS ITk pixel barrel layer 4. The sensors are tested to be radiation tolerant up to at least 100 Mrad and 1×10^{15} n_{eq}/cm^2 [2]. The principle of operation of HVCMOS sensors is explained in [3]. The pixel electronics [4] include a charge sensitive amplifier and a discriminator that are placed inside the n-well which acts as the charge collection electrode. A high voltage is used to deplete the p-substrate underneath. The major blocks of ATLASpix chips are HVCMOS sensor array, hit buffers to store the hit information, Readout Control Unit (RCU) for scheduling the readout operation and several full custom blocks such as PLL, bias block, serializer etc. The signals caused by particle hits are digitized using discriminators and transferred to the digital periphery of the ASIC where the hit buffers are located. The hit buffer acts as a temporary storage for hit information until it is sent to the End of Column (EoC) buffer. There are two design variants based on the readout architecture, namely ATLASpix1_Simple and ATLASpix1_M2. ATLASpix1_Simple employs a traditional column drain readout without trigger whereas ATLASpix1_M2 adopts a novel triggered readout scheme [5]. The architecture of ATLASpix1_Simple and its experimental studies are described in [4]. Both ATLASpix1_Simple and ATLASpix1_M2 share the same pixel electronics and RCU.

2. Architecture and readout electronics of ATLASpix1_M2

ATLASpix_M2 employs a parallel hit transfer mechanism from the pixels to hit buffer, which is called "Parallel Pixel to Buffer (PPtB)"[5]. Out of 17920 pixels, each group of 16 pixels forms a super pixel which can be addressed using 8 address lines by projection addressing figure 1. This helps to save routing space by reducing the number of interconnect lines required to transfer the hit pattern from 16 to 8. The effect of RC delay of these routing lines that transmit the hit signals from the pixel driver to the hit buffer is investigated. Simulations done on a simplified RC-extracted netlist show a difference of 36 ns between the RC delays of interconnect lines corresponding to the top most pixel and the bottom most pixel in a column. In order to minimize this effect, the next generation ATLASpix chips are planned to be layouted in a way that the length of routing lines from pixel to hit buffer remain uniform across the matrix. This can be achieved with the help of an additional routing layer. The address encoding scheme shown in figure 1 poses a risk of having ghost hits sharing the same address pattern as real hits. Due to the small area of a super pixel (800 $\times$ 60 μm^2), the rate of multiple clusters is reduced by several orders of magnitude. Assuming a total hit rate of 108 MHz/cm^2, the probability of having a hit in the super pixel per bunch crossing is calculated as 1.3×10^{-3}. Ghost hits are caused either when a single particle produces a cluster on the group edges (figure 1) or when two particles hit the pixels of neighbouring groups in a super pixel. The former scenario leads to a real hit pattern which can be identified as a cluster and two ghost hits that appear as two separate particle hits. Since the probabilty of occurrence of two separate particle hits is much less than than the probability of a single clustered hit, we can neglect the ghost hits during reconstruction.
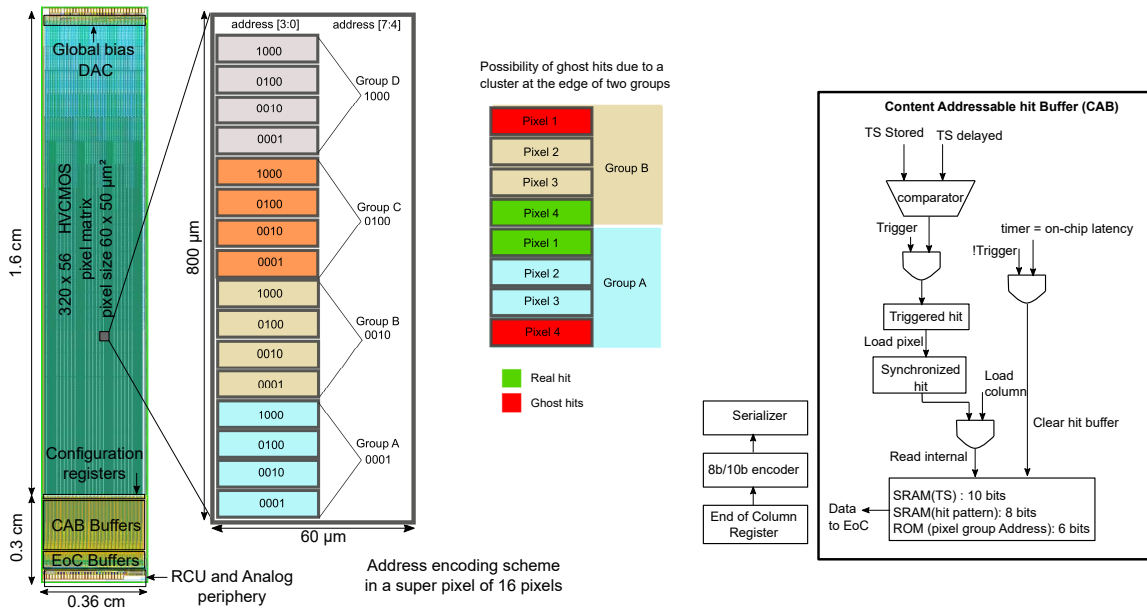
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Figure 1: ATLASpix1_M2 Top layout showing address encoding and readout logic

43 A super pixel is mapped to a Content Addressable hit Buffer (CAB) buffer block which can
44 store four hits. The hit buffer compares the stored Time Stamp (TS) (10-bit) with a delayed TS
45 propagated within the chip, hence it is content addressable. The group address (5-bit) of the super
46 pixel is programmed in address ROM. When there is a particle hit in one or more of the 16 pixels,
47 two or more address lines will be set to high. Therefore, a hit can be detected by calculating logical
48 OR function of the address lines (HitOR). When the HitOR signal goes high, the hit pattern (8-bit)
49 is recorded and transfered to CAB buffer. The time stamp of the corresponding HitOR signal is
50 recorded in the RAM. The time stamps are 10-bit gray coded signals with a period of 25 ns that
51 corresponds to the bunch crossing (BC) period of LHC. The hit information is held in the CAB
52 buffer until its retention time elapses. The retention time is programmable and is called on-chip
53 latency. The on-chip latency is determined by comparing the stored time stamp with an additional
54 time stamp signal that has the same period but different phase as the original time stamp signal.
55 Both time stamps are generated on chip. If level-1 trigger signal is received within the time period
56 before the on-chip latency expires, the stored hits are marked for readout. The hits that are not
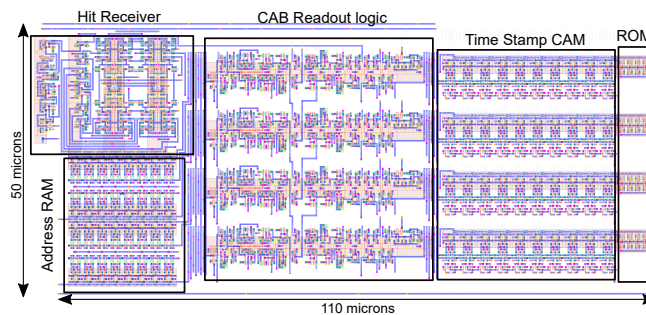57 marked for readout are deleted from the buffer.

Figure 2: Content Addressable Buffer (CAB) block full custom layout
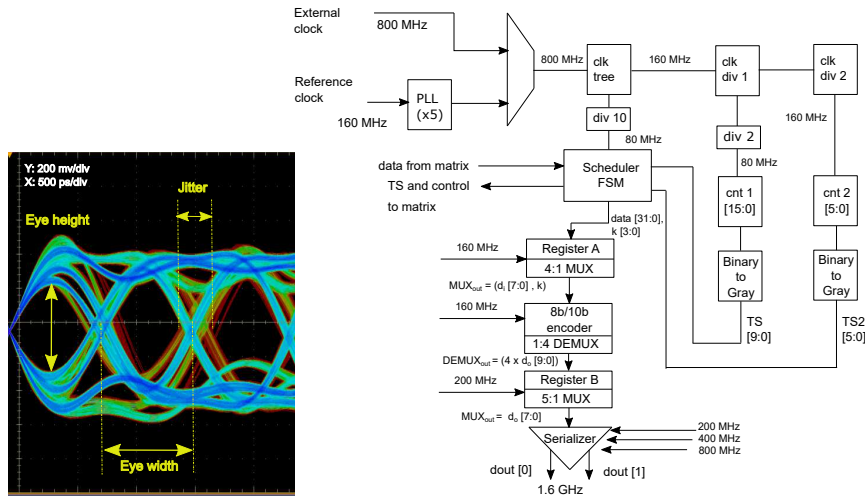
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Figure 3: ATLASpix1_M2 Readout Control Unit block and eye diagram at 1.28 Gbps

The readout control unit (figure 3) generates control signals to schedule the entire readout operation. It includes loading of the hit information from the hit buffer to the EoC buffer (load column) and reading the hit data from the EoC (read column). The hit data is then encoded and serialized. The RCU generates gray-coded time stamps and delayed time stamps (delay value equals on-chip latency) of 10-bits length. The 6-bit TS2 time stamp in figure 3 is unused in ATLASpix1_M2 chip and is used to store time-over-threshold in ATLASpix_Simple chip since both the chips have the same RCU design. The RCU works on multiple clock domains. The clocks of frequencies 160 MHz, 200 MHz and 400 MHz are generated from an input clock of 800 MHz using johnson counters and combinational logic. The encoder is a pipelined custom 8b/10b encoder with running disparity based on [6]. The serializer is based on a 3-stage MUX tree with input synchronization. The serializer in RCU outputs two bits. The final stage of serialization is achieved using a full custom serializer based on current mode logic.

3. Measurement results of ATLASpix1_M2

The data transfer characteristics has been studied with the help of an eye diagram. The oscilloscope probe was connected to the data line on the PCB which is about 10 cm long. On-chip PLL was used to generate the clock at 800 MHz. The serial data output works with Double Data Rate (DDR) of 1.28 Gbps with an eye height of 504 $\pm$ 1 mV, an eye width of 580 $\pm$ 1 ps and a jitter of 100 $\pm$ 0.2 ps as shown in figure 3. A threshold scan was done over the entire pixel matrix of size 320 $\times$ 56 at a readout speed of 800 Mbps. The trigger is generated a with a fixed delay after the injection, and it has a width of 400 ns (equivalent to 16 BC). The on-chip latency is adjusted so that all hits generated by injection are triggered. The injection voltage was then varied from 0 V to 0.6 V in steps of 0.025 V keeping the injection delay, the number of injections (10) and the on-chip latency (43 time stamps, where each time stamp corresponds to 1 BC) fixed. It is possible to adjust the threshold of every pixel using a 3-bit D/A converter (tune DAC). These tune bits are stored in the pixel memory. The threshold dispersion was reduced by a factor of four after tuning as shown

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in figure 4. The mean threshold is 1055 e⁻ with a standard deviation of 35 e⁻. The mean value of noise distribution over the entire pixel matrix after tuning is 78 e⁻.
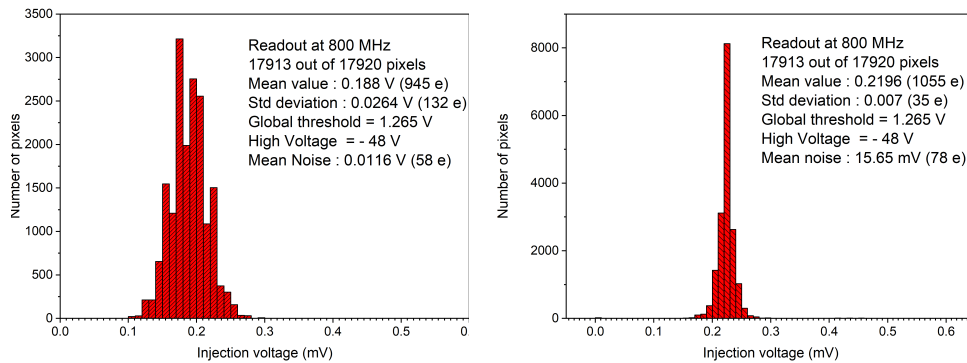

Figure 4: Threshold dispersion before tuning (left) and after tuning (right)

4. Conclusions and future work

ATLASpix1_M2 is the first large area and full height HVCMOS sensor prototype with triggered readout. The chip architecture includes several novel design concepts such as the Parallel Pixel to Buffer (PPtB) transfer, address compression of a super pixel, Content Addressable Buffer (CAB) readout, pipelined 8b/10b data encoding and serializer tree. The sensor is fully functional. The thresholds have been measured using the full readout chain. The threshold after tunning had a mean value of 1055 e⁻ with a standard deviation of 35 e⁻. The mean value of noise was about 78 e⁻. These values are small compared to the average signal of about 5000 e⁻. The serial data link works at the required data rate of 1.28 Gbps. Based on ATLASpix1 designs, a full size 2 cm×2 cm HVCMOS prototype will be developed. Test beam and irradiation studies are planned within the collaboration of six different institutions.

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