PROCEEDINGS OF SCIENCE

ABACUS : Two fast amplifiers for the readout of LGAD detectors.

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The design of a single particle counter for therapeutical proton beams based on Low Gain Avalanche Diodes and optimized for very fast signals is carried on in the framework of the INFN MoVe-IT research project. Fast signal shaping front-end electronics is mandatory in this application in order to deal with particle rates of the order of hundreds of MHz per channel. Two preamplifier architectures, one based on a fast Charge Sensitive Amplifier with self-reset capabilities and a second one based on a Trans-Impedance Amplifier have been developed in a commercial CMOS 0.11 μm technology and submitted to the foundry.

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1. Introduction

Hadrontherapy is the present forefront of cancer treatment with radiations. Ions (protons and carbon ions are the most used) are preferrable over photons since they release most of their energy in the last millimeters before coming to a stop. Therefore this technique is suited to treat tumors that are either deep or located close to critical organs.

The MoVe-IT (Modeling and Verification for Ion beam Treatment planning) project aims at the development of models for biologically optimized treatment planning systems and dedicated devices for plan verification.

In this framework a single particle counting detector and readout electronics for therapeutical proton beams is under development [1]. The device will have to cope with fluxes up to 10^9 p/(cm$^2\cdot$ s), while keeping the pileup probability below 1%. The detector is based on Low Gain Avalanche Diodes (LGADs) [2] implemented with thin sensors (50 μm) and gains of 10-20, thus optimized for very fast signals.

The current prototype covers a 30×30 mm^2 area; currently two different sets of strip geometries are under evaluation, with strip lenghts of 15 mm and 30 mm. The expected signal from this detector is between 4 and 150 fC for protons (with a gain of 15) and between 30 and 150 fC for carbon ions (with gain = 1). Figure 1 shows a typical LGAD structure and signal shape.

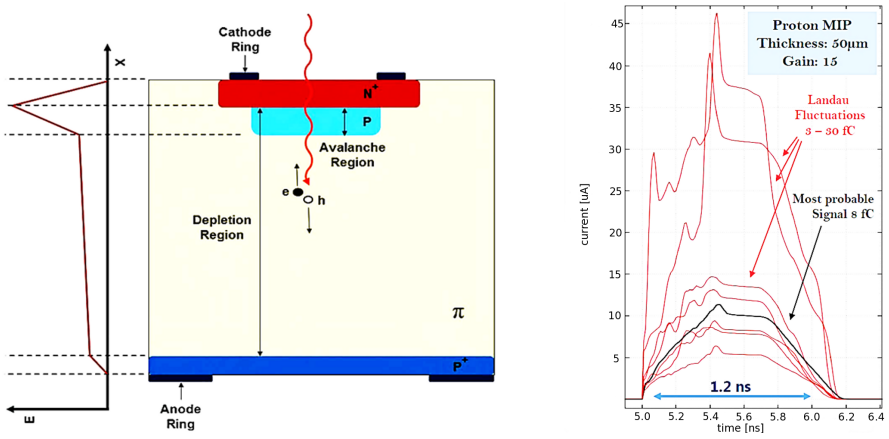

Figure 1: LGAD structure and signal shape.

Since the purpose of the system is to count the single particle, the front-end electronics has to provide not only fast rising times, as in timing measurement applications, but also a short signal duration in order to minimize the pile-up counting inefficiencies (instantaneous rates of 100 MHz or higher are expected for each readout channel). Moreover, in the energy range of therapeutical beams, the input charge dynamic range can be fairly large (between 3 and 150 fC) considering the large energy loss fluctuations in thin sensors.

Two different readout architectures have been developed in order to fulfill these demanding requirements. The first architecture is based on a Charge-Sensitive Preamplifier (CSA) with an automatic feedback capacitance reset to reduce the signal tail. The second one is based on a high bandwidth Trans-Impedance Amplifier (TIA). Both architectures have been prototyped on two 24-channels test ASICs in a commercial 0.11 μm CMOS technology. Section 2 and 3 of the paper

describes the two architectures while section 4 shows simulation results. Conclusions are drawn in section 5.

2. CSA-based architecture

The architecture, depicted in figure 2, is an evolution of a charge sensitive preamplifier developed for the readout of LGAD detectors [3]. In order to reduce the signal tail a reset signal on the 500 fF feedback capacitor has been introduced. The reset signal is controlled by the discriminator output.

The preamplifier is based on a direct cascode configuration with gain boost. It is biased with a fairly high current (about 10 mA) in order to obtain a gain-bandwidth product of 900 MHz with an open loop gain of 15 and an input capacitance of 5 pF. The simulated rms noise is about 0.323 fC.

The preamplifier is followed by a buffer and a multistage discriminator which generates the binary output signal. The discriminator output drives both the output driver and the feedback capacitor reset signal. The output driver is a Current Mode Logic (CML) differential stage with internal 50 Ω input termination in order to achieve high speed.

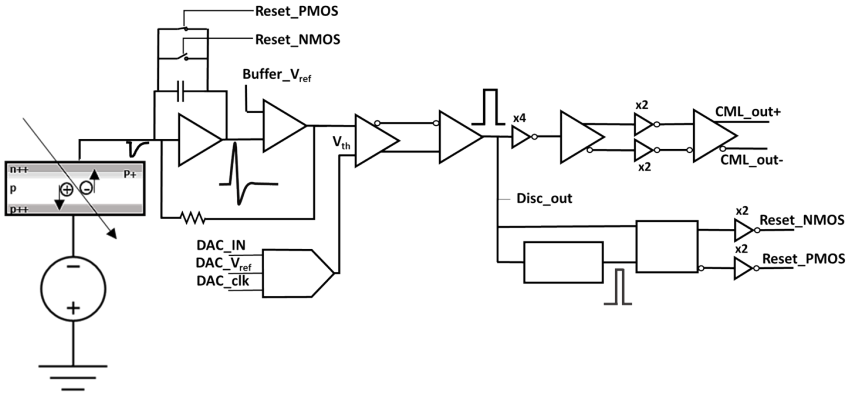

Figure 2: CSA-based architecture

A recovery circuit (in the bottom right of the scheme) sends further reset signals if the discriminator output remains high for a long time. This feature is used to increase the efficiency at high particle rates avoiding the CSA saturation due to pile-up. The discriminator threshold is controlled by a global control signal combined with a fine-tuning 6-bit per channel DAC.

3. TIA-based architecture

The second option is based on a high speed circuit architecture capable to follow as much as possible the shape of the input signal. The natural choice for such a circuit is the TIA scheme used for the readout of photodiodes for optical transmission. Several schemes have been proposed and implemented for this purpose [4]. Such an architecture can provide higher bandwidth and thus higher speed with respect to the CSA option. However, also the noise, integrated over a wide bandwidth, will be higher.

The main difference between a photodiode for optical communication and a LGAD is the capacitance, which is in the range of few hundreds of fF in the first case and of few pF in the second one. The higher capacitance has a significant implication in the design of the TIA, since its bandwidth is inversely proportional to the product of the input capacitance and the feedback resistor, thus resulting in a gain-bandwidth trade-off. The issue is made more severe by the fact that at high frequencies it is not easy to obtain a large open loop gain, which would be the most obvious solution to improve both parameters.

Two solutions have been implemented in order to address the problem. The first one is based on a two-stages fully differential core amplifier in order to increase the open loop gain and thus the close loop bandwidth. In the second solution a unity gain current buffer has been inserted between the input and the TIA to decouple the detector capacitance from the TIA input. The second solution features a reduced sensitivity to the detector capacitance and avoids a two stage amplifier, which is slower and requires more power; however, it adds an extra contribution to the noise.

A transimpedance gain of 10 kΩ has been selected for both architectures. The channel overall architecture is depicted in figure 3. The TIA stage (1) is followed by two voltage gain stages (2) with an overall gain of ≈16. After the amplification, a differential threshold is applied by a discriminator (3) followed by a further voltage gain stage, which drives the CML output stage (4). The differential threshold is generated by a single ended to differential converter (5) with the same common mode voltage of the gain stages.

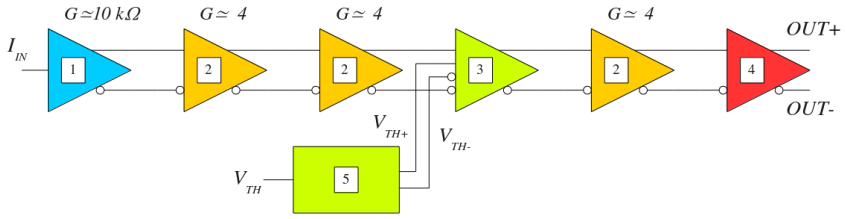

Figure 3: TIA-based architecture

4. Simulation results

The two architectures have been simulated using data obtained from the Weightfield2 and Geant simulators for the predicted environment. Figure 4 shows an example of the obtained results for protons with energy of 60 MeV and 250 MeV and average rate of 100 and 200 MHz.

The results obtained with the CSA scheme using the post-layout netlist obtained after the layout parasitic extraction show an efficiency close to 100% at 100 MHz, and about 85% at 200 MHz. It can be seen from figure 4 that some inefficiency is due to signal pile-up at the detector level and thus it cannot be resolved by the readout electronics.

TIA simulations shows a 74% efficiency at 100 MHz and 40% at 200 MHz for the same sets of input signals. Since for this scheme the signal duration is proportional to the input signal one, it is possible to partially correct for the input signal overlap using the signal width to detect pile-up. With such corrections, the efficiency increases to 96.5% and 64%, respectively. A better result can

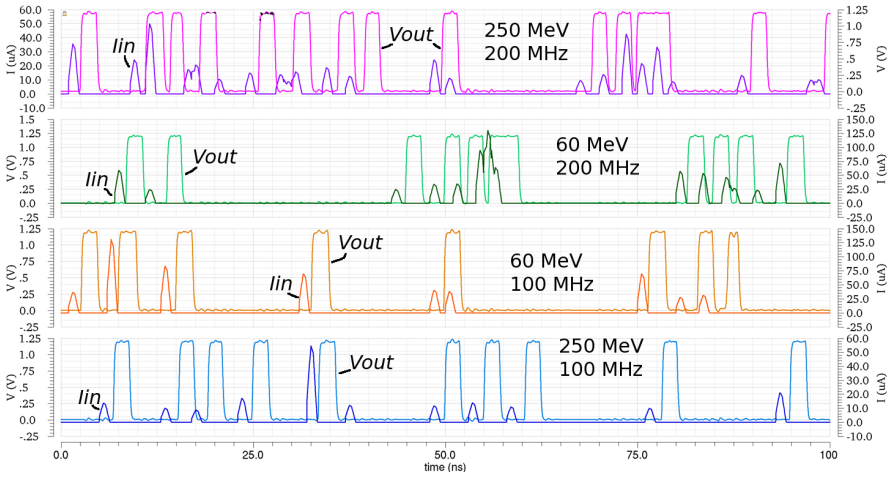

Figure 4: CSA channel simulations after layout parasitic extraction.

be obtained with MIPs, with an efficiency before correction of 80% and 66% at 100 MHz and 200 MHz, respectively and 92% and 87% after correction.

It should be noted that the development of the electronic readout is going in parallel with the detector optimization. Therefore the choice of the architecture will be made only after the proper detector size and gain will be selected.

5. Conclusions

Two 24-channels prototypes for the fast counting of particles crossing a LGAD silicon detector have been designed and produced in a commercial CMOS 0.11 μm technology. The two protoypes are based on a charge sensitive amplifier with self-reset capability and on a transimpedance amplifier configuration, respectively.

The two prototypes are intended to evaluate the best architecture to be used for a fast single particle counting system for dose delivery measurements in hadrontherapy. The prototypes have been received from foundry and are currently under test.

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