PROCEEDINGS OF SCIENCE

Flexible Printed Circuit design and testing for the High-Granularity Timing Detector for the Phase II upgrade of the ATLAS calorimeter system

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The High-Granularity Timing Detector (HGTD) will improve the performance of the ATLAS detector for the high luminosity upgrade of the LHC (HL-LHC) by providing precise timing information with a resolution of about 30 ps per track. The basic unit of the detector consists of a hybrid module of a 2×4 cm^2 Low Gain Avalanche Detector (LGAD) bump-bonded to two ASICs and wire-bonded to a Flexible Printed Circuit (FPC; FLEX cable). The latter transmits high-speed signals (1.28 Gb/s) for data readout while providing power and bias voltage to the module. Its design must fulfil the HGTD requirements both mechanically and electrically, combining different signal types. The design and the test plan of the initial prototype are presented.

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1. High-Granularity Timing Detector

The number of collisions per bunch crossing is increased in the HL-LHC leading to a new challenge for the upgrade of the ATLAS detector; a High-Granularity Timing Detector (HGTD) is proposed in this frame. The HGTD will improve pile-up mitigation, as well as b-tagging and lepton isolation performance by providing precise timing information associated to each track in the endcap region (σ_t = 30 ps per track with $2.4 < |\eta| < 4.0$)[1]. The basic detector unit, so-called module, consists of a 2×4 cm^2 Low Gain Avalanche Detector (LGAD) bump-bonded to two ASICs (2×2 cm^2 each). This element is glued on a Flexible Printed Circuit (FLEX cable) and wire bonded for the electrical signals (power supply, data transmission and slow control). The active area shown in Fig.1 is covered with modules placed on readout-rows, represented by the segmented regions. The most populated row consists of 19 modules (placed on the top and bottom sides of the cooling plate) that must be connected to the peripheral electronics boards.

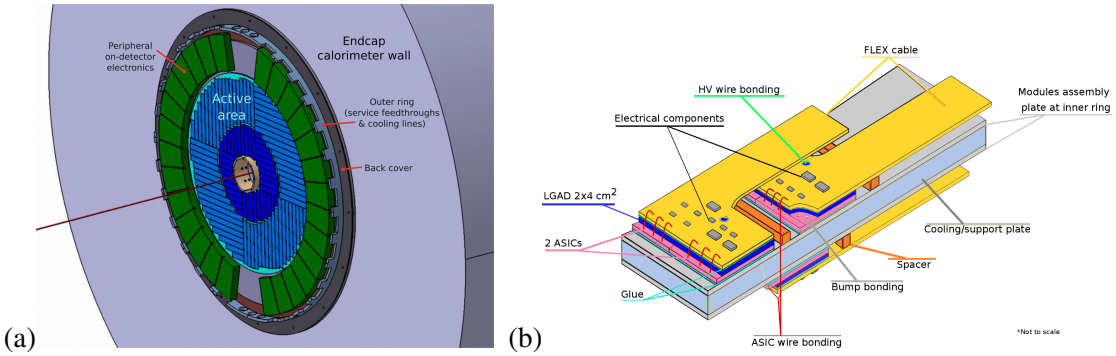

Figure 1: (a) Illustration of the HGTD, showing the peripheral on-detector electronics in green and the layout of the readout rows, containing modules mounted on the inner half-disk support plates at R < 320 mm (dark blue), and on staves at larger radii (light blue). The inner half-disk is a single structure to allow easy replacement at half lifetime of the HL-LHC [1]. (b) Schematic drawing of two adjacent modules on the top side and one on the bottom side of the cooling plate; the modules are mounted on thin support plates.

Table 1: Types of signals for two ASICs included in the FLEX cable design

Signal type	Signal name	No. of wires	Comments
HV	1 kV max.	1	HV reliability on insulation
POWER	1 $\times$Vdda, 1$\times$Vddd	2	Power planes
GROUND	Analog, Digital	1 plane	Dedicated layer
Slow control	Data, Ck (opt. + rst, error)	2 to 4	I^{2}C link
Input clocks	320 MHz, Fast command e-link (opt. 40 MHz (L1))	4 or 8	CLPS
Data out lines	Redout data (TOT, TOA, Lumi)	4 pairs	4 e-links differential pairs
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	1 or 3	Analog lines

2. FLEX cable requirements

Both the mechanical and the electrical constraints make a Flexible Printed Circuit the best

candidate to connect the signals from the module to the peripheral electronics, since the current PCB fabrication technology does not fulfil the manufacturing requirements previously mentioned. The geometrical constraints of the FLEX cable are defined by the distance between two layers, the distance between the modules and the peripheral electronics and the maximum number of modules per readout row. This fact leads to the design shown in Fig. 1 presenting three modules on top and bottom of a cooling plate. Considering the harshest constraints, the flex cable geometrical parameters are a maximum length of 750 mm, width < 19 mm and thickness < 350 μm. Considering the electrical requirements, one HV line is required in the design in order to supply voltage to bias the LGADs (1 kV maximum). Since two ASICs are bonded per FLEX, only few signals are merged and the full set (i.e. for clock or data transmission) of signals in Table 1 must be routed.

3. Prototype design

As part of the initial study phase, a prototype has been designed with the aim to understand the technology requirements (materials, manufacturing capability, electrical and mechanical robustness) and address the potential problems by representing a significant subset of the signals (signal integrity, power distribution, HV insulation, interference and crosstalk). The direct interaction with the company allowed to overcome the process limitations leading to a satisfiying compromise to produce 8 prototypes of 750 mm and 8 medium length, 430 mm pieces as depicted in Fig. 2.

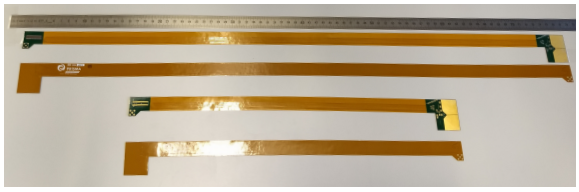

Figure 2: Top and bottom view of two different length FLEX cables: long (750 mm) and medium (430 mm).

The stackup of the cable consists of a 4 copper layers design with layers numbered 1 to 4 from top to bottom. On the top layer the impedance control is achieved with a microstrip configuration. Layers 2 and 4 are full planes dedicated to powering and grounding. Then, the differential pairs as well as the HV line are placed in layer 3 in a stripline configuration. In order to improve the impedance match 100 $\pm$ 10 Ω for the differential pairs and 50 $\pm$ 5 Ω for the singles lines, the manufacturer proposed hatched planes in both powering and grounding planes. This configuration affects the voltage drop and power integrity of the FLEX cable. The impact of this decision was carefully simulated and evaluated before the manufacturing.

3.1 Power Integrity simulations

Post-layout simulations were performed with Cadence "Sigrity" and "PowerSI" [2] (signal integrity and power distribution over long lines). Signal integrity and power integrity are mutually influenced. On the one hand, this choice increases the impedance of the differential lines without further reducing the width and the spacing of the tracks. On the other hand, the etching increases the DC resitance of the power lines. The figure of merit between the resistance of the hatched and

Table 2: Power Integrity simulation results comparing the voltage drop for a FLEX cable with hatched and non-hatched geometry for power and ground planes.

Plane	Ratio
Power analog	3.51
Power digital	4.57
Ground analog	3.60
Ground digital	4.50

non-hatched geometry for power and ground planes is defined by

$$\text{Ratio} = \frac{R_{\text{hatched}}}{R_{\text{non-hatched}}}$$

The results of the simulation are listed in Table 2. Tolerating the 4 times higher resitance has a benefit on the matching of the impedance that increases from 66 Ω to 90 Ω and the Standing Wave Ratio from 5:1 to 1.2:1. It should be simplier to compensate a DC voltage drop than an impedance mismatch.

4. Testing plan

The performance of the first prototype is currently under evaluation at the PRISMA Detector Laboratory in Mainz. To emulate the signals we have programmed an FPGA on the Kintex KC705 evaluation board [3] and connected the FLEX cable via an adapter board to build an automatic test setup for all the types of cables that are under test.

The FPGA injects test patterns at 1.28 Gb/s and checks the response with the Integrated Bit Error Rate Test (IBERT). The SMA connectors placed on the adapter board route the signals to the oscilloscope for classical eye-diagram analysis. A wire bonding between two differential pairs at the end of the FLEX cable makes a loopback path for the signals. Our test configuration and the I/O drivers are compatible with the VC707 [4] FPGA used by the LpGBT [5] system. In this way we assure the same conditions as the on-field operation.

The insulation of the FLEX materials is checked up to 1 kV with the Megger MIT420 tester [6]. Additionally the IBERT will be performed with and without HV in order to check the influence of the HV while transmitting the high speed signals. The Time Domain Reflectrometry (TDR) test is performed in order to check the impedance homogeneity of the tracks, which is crucial for high-speed data transmission. The Tektronix DSA8200 oscilloscope [7] together with the TDR modules 80E08 [8] were used to measure the impedance. A preliminary result of the impedance as a function of the length for one of the diffential pairs of the FLEX cable is shown in Fig. 3. The dashed vertical lines indicate the region of the differential lines on the FLEX cable. The impedance values shown in the region previous to the FLEX cable correspond to cables, connectors and the adapter board used to connect the TDR equipment to the FLEX cable.

All tests are performed both at room temperature and at the foreseen operation temperature of -30^{o}C required to decrease the leakage current when running the sensors, to emulate the conditions in the HGTD.

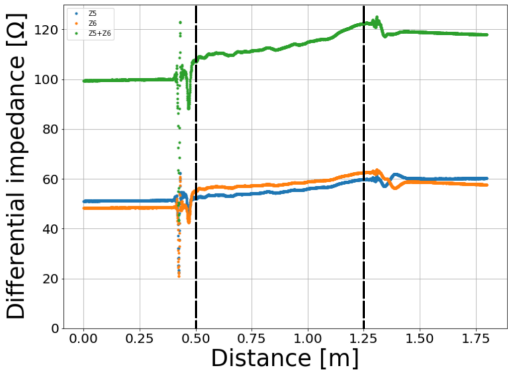

Figure 3: Preliminary result of the differential impedance for a differential pair line in the FLEX cable (green). The vertical dashed lines indicate the region of the FLEX cable. The orange and the blue lines correspond to the impedance mesurement for each line of the differential pair by the module Tektronix 80E08, used to calculated the differential line impedance (green).

5. Conclusions

The first prototype of a FLEX cable for the ALTAS HGTD was designed and manufactured considering both the electrical and geometrical requirements. Simulations were performed in order to study and improve the power integrity of the design. The FLEX cable is intensively tested in terms of power integrity and signal integrity to prove its capability to fulfil the requirements of the HGTD.

References

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