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An integrated SRAM radiation monitor in 180 nm CMOS technology

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In this work an experimental radiation sensor is presented which is based on an SRAM (Static Random Access Memory). The radiation flux is measured with the memory by counting the number of Single-Event Upsets (SEUs) within one readout cycle. This monolithic sensor allows a cheap alternative to existing sensors. The core supply voltage of the memory can be adjusted to increase the SEU sensitivity. The sensor was verified experimentally with heavy ions, protons and two-photon laser tests.

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1. Introduction

Radiation monitoring is required in any nuclear facility like nuclear power plants, high-energy physics experiments but also for space and ground applications. Typically this involves expensive sensors and a combination of different technologies to perform the monitoring. Static Random Access Memories (SRAMs) have proven to be useful to monitor ionizing radiation through the measurement of SEUs in the devices [1]. By counting the amount of upsets, an estimation can be made about the particle flux. The measurements may not be as accurate as other dose or dose-rate measurements but this approach becomes very cost efficient. Over the past decades, the soft error rate in commercial SRAM devices has been reduced significantly through error coding, which was required to counteract the intrinsic single-event sensitivity of devices in scaled technologies. By developing a custom SRAM ASIC, the increased sensitivity of the scaled devices can be employed to obtain a sensitive memory based radiation sensor.

The RadMon radiation monitoring system at the LHC complex currently employs SRAM memories to detect radiation [2]. These commercial SRAMs are based on 0.4 μm CMOS technology and has become obsolete. More recent versions are based on a 90 nm CMOS memory which has been characterized extensively [3]-[5]. The advantage of using commercial components is their reduced cost and instantaneous availability. However, the sensitivity and performance of the devices solely depend on the manufacturer and usually, few design details are available as an input to the system development.

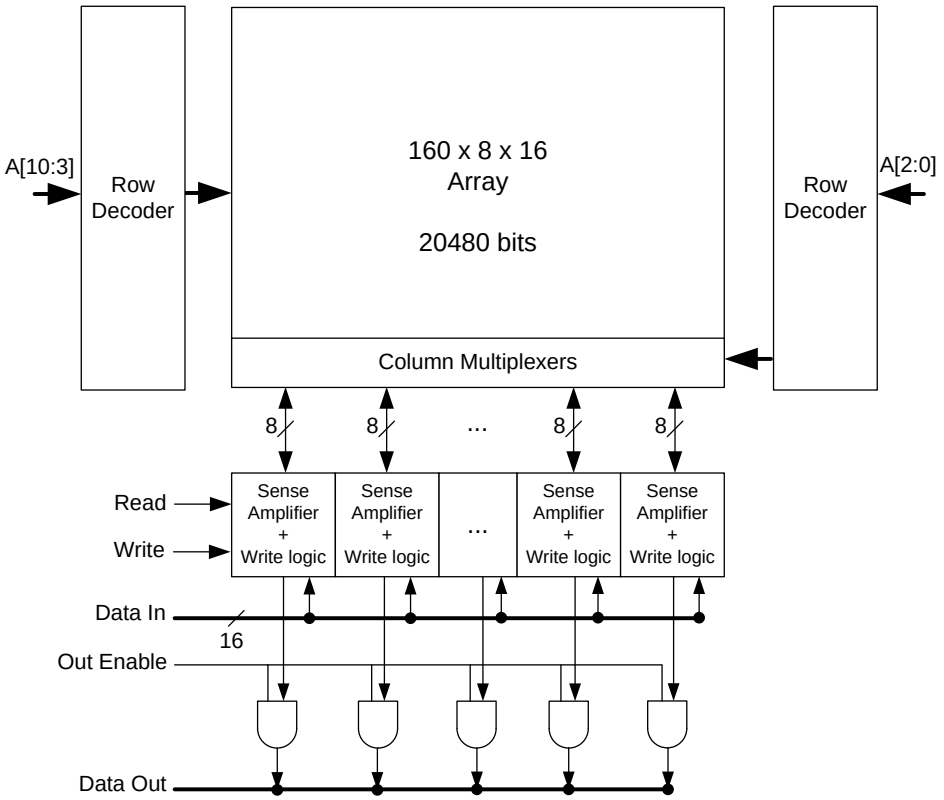
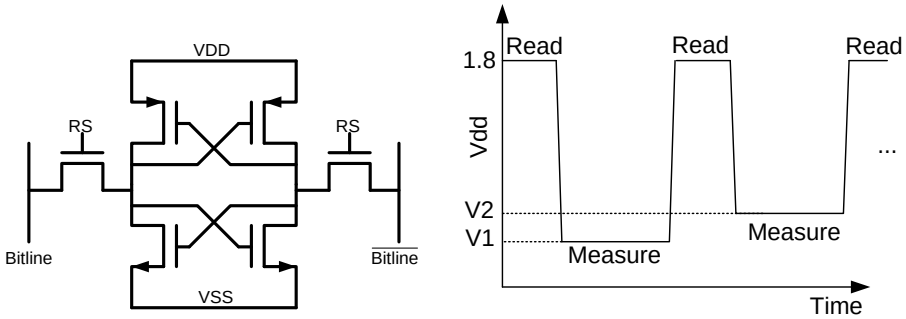


Figure 1: SRAM architecture.

2. SRAM architecture

The custom SRAM device architecture is shown in Figure 1. The SRAM array is organized as a 2D matrix of 160 rows and 128 (8x16) columns. This yields a total of 20480 cells within a 700 x 700 μm^2 area. Logically, the SRAM is interfaced with 16 bit data words such that the memory can be seen as a 160 x 8 array. This means that each read or write operation involves 16 bits simultaneously. The logical to physical mapping of the array is extremely important for the back-end analysis of multi-bit upsets.

The digital logic of the SRAM consists of 3 main parts, firstly the binary address is decoded through the row and column decoder. Which selects the appropriate row and column. Secondly, the read and write logic interfaces with the SRAM cells. A sense amplifier is used for readout which amplifies the word line signal since these (differential) voltages are not full-swing logic signals. Thirdly a shift register is used to communicate with the memory serially. With this approach, the communication speed is reduced compared to a parallel data/address interface. However, since the targeted readout rate is very slow (10's seconds), this is not required which saves area of the package and routing/interface complexity of the test system. Finally, the serial interface was designed such that many chips can be daisy chained. This has been done to increase the statistical data collection during radiation tests by using 4 chips simultaneously. All digital logic has been protected with Triple Modular Redundancy (TMR) to prevent errors in the memory.



(a) (b)

Figure 2: a) Schematic of 6T SRAM cell. b) Power readout cycle.

The schematic of a single SRAM cell is shown in Figure 2a. This is conventional 6-transistor (6T) SRAM cell which a cross coupled inverter as storage element and two access transistors to a shared bitline. The access devices are controlled by the row decoder while all columns share the same bitline. Thus, 160 devices are connected to a bitline which has a single pull-up device on the top. The access devices are sized to prevent destructive read operation on the cells.

It has been well known that each of the SRAM cells has specific static noise margins. These noise margins drastically decrease when the supply voltage of the memory reduces. Therefore, this ASIC has separate supply voltages for the SRAM core devices and the digital interface logic. In this way, the SRAM core voltage can be reduced without reseting or altering the operation of the internal digital modules. The reduction of the static noise margin proportionally leads to an

increased sensitivity to single-event upsets (SEUs) which is beneficially for this SRAM radiation monitor.

However, careful interfacing is required when dealing with reduced noise margins. If the memory array is read when operating at ultra-low supply voltages (e.g. O.3 x Vdd), the reads may be destructive. Therefore, the readout cycle, shown in Figure 2b was used. When interfacing to the SRAM, the supply voltage of the SRAM cells is ramped to its nominal Vdd. Then the cells are read or written. In the next phase, the voltage of the SRAM cells is reduced. In this phase, which is dominant over time, the memory is exposed for several seconds at a reduced supply voltage and increased sensitivity to ionizing particles. Then, finally, the supply voltage is increased to read/write the array. The measured flux/fluence is directly proportional to the number of upsets measured in the SRAM.

3. Measurements

Various radiation experiments were done with this SRAM memory: heavy-ions, protons, high-energy hadrons and finally two-photon laser scanning tests. Overall, these measurements confirmed that the supply voltage has a significant impact on the cross section of the SRAM cells. Heavy ion tests were performed at the RADEF facility in Finland using cyclotron accelerated ions with an energy of 9.3 Mev/nucleon and LETs ranging from 1.8 - 60 Mev.cm^2/mg. The cross section of a single cell is shown in Figure 3. This shows the cross section for various supply voltages ranging from 0.4V up to 1.8V. From this measurement, it is clear that the cross section changes with different supply voltages. In the back-end calculation, a separation was done between single-event upsets and multi-bit upsets (MBU). This was done by analyzing the bitmaps that were periodically measured. The measured cross section for SEUs and MBUs are shown in Figure 4 where the

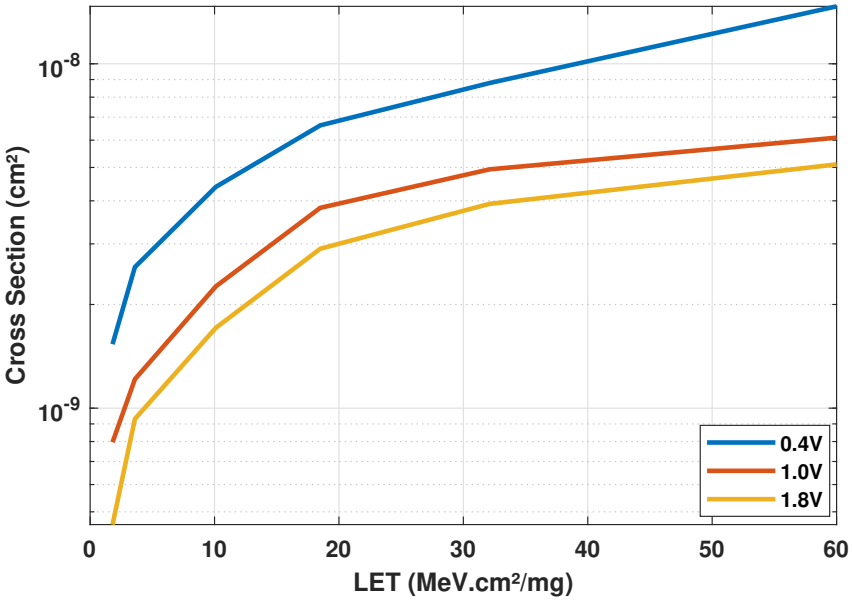


Figure 3: SRAM cell cross section for heavy-ions.

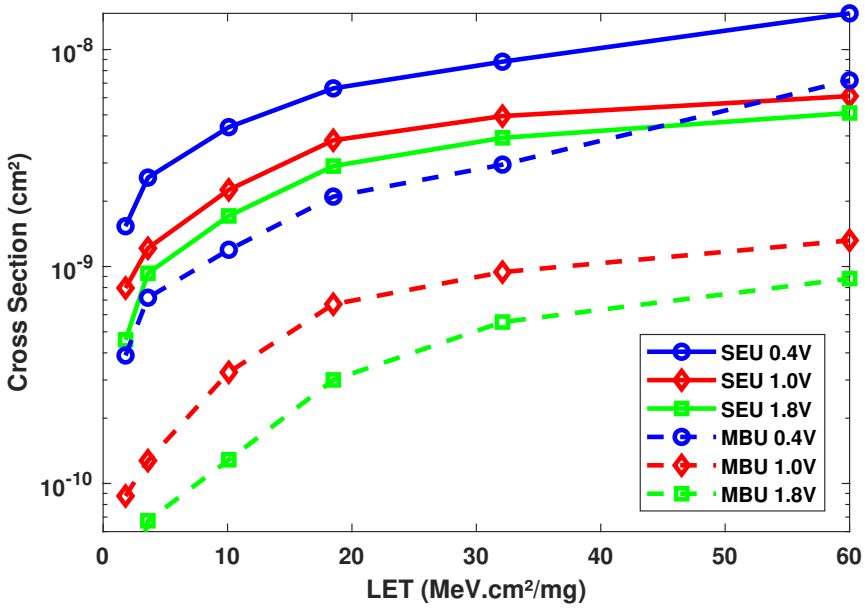


Figure 4: SRAM cell cross section for heavy-ions for SEU and MBU.

solid curves represent the SEU cross sections for varying supply voltages and the dashed curves represent the MBU cross sections. From this data, two observations can be made. Firstly, similarly to the SEU cross section, the MBU cross section increases when the supply voltage is reduced. This is due to the increasing sensitivity of surrounding cells which at their turn, more easily trigger multiple upsets. Secondly, the ratio between SEU and MBU cross section for low supply is much smaller compared to the ratio for large supply voltages.

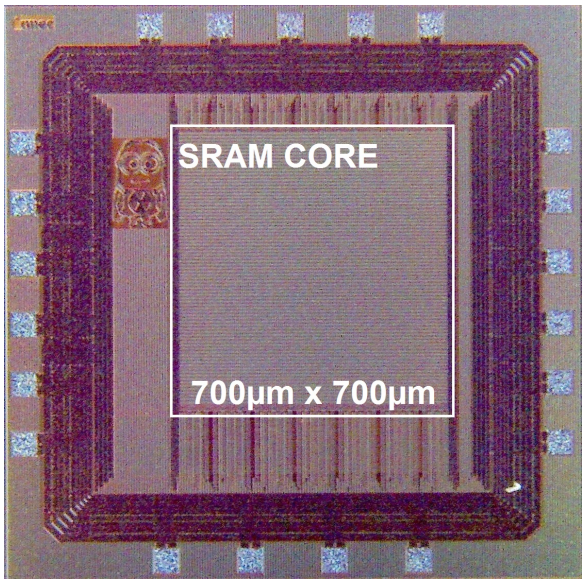


Figure 5: SRAM die photograph.

The SRAM memory was designed and processed in a 180 nm CMOS technology and the die has a size of 1500 x 1500 μm area with a 700 x 700 μm sensitive core area. A die photograph is shown in Figure 5.

4. Conclusion

This paper presents an experimental verification of a custom SRAM memory which has a flexible sensitivity controlled by adjusting the supply voltage of the SRAM cells. The adjustment of the supply voltage leads to a change of the sensitivity of the array. A different sensitivity dynamic range has been observed for SEUs and MBUs. Therefore, a combination of SEU and MBU measurements can improve the accuracy and range of the device. The chip has been designed an processed in a 180 nm CMOS technology.

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