

## GBT oriented firmware for Data Processing Boards for CBM

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The Data Processing Boards are the important component of the development version of the CBM readout system. Even though in the final version they will be replaced with the new Common Readout Interface PCIe boards, they are still used for development and testing of new firmware features and for operation during the beam tests. The paper describes the current state of the DPB firmware development. The special emphasis is put on the functionalities related to support for various configurations of the GBTX-connected front-end electronics.

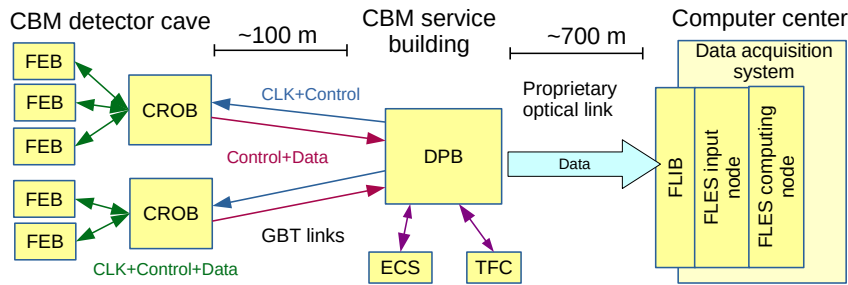
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## 1. Introduction

The Compressed Baryonic Matter (CBM) experiment is currently prepared at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt. Its purpose is the exploration of the QCD phase diagram in the region of high baryon densities during high-energy nucleus-nucleus collisions [1]. CBM will utilize various particle detectors: Micro Vertex Detector, Ring Imaging Cherenkov Detector, Transition Radiation Detector, Time of Flight Detector, Projectile Spectator Detector, Silicon Tracking System (STS), Muon Chamber (MUCH). In the first version of the CBM readout chain the Data Processing Boards (DPB) implemented on AFCK [2] hardware platform were important components responsible for communication between the Front End Electronics boards (FEB), the Timing and Fast Control (TFC) system, the Experiment Control System (ECS) and the first stage of the data acquisition system - First Level Event Selector (FLES) (see Figure 1).

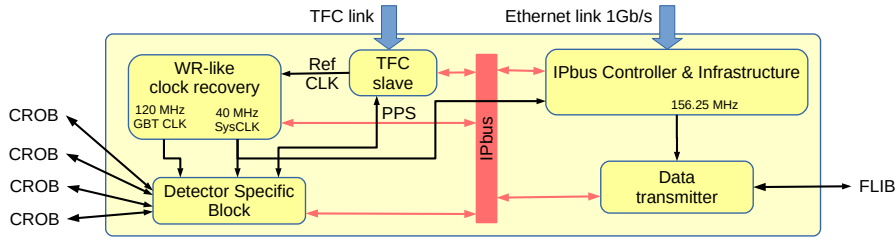


**Figure 1:** The first version of the STS readout chain in the CBM experiment (based on [3]).

In the final version of the CBM readout chain, the DPB boards will be replaced with the Common Readout Interface boards [3, 4], implemented as PCIe cards and located in the FLES Input Node computers moved to the CBM Service Building. That solution will allow utilization of standard network connections to transmit data to the FLES computing nodes in the Computer Center. However, DPBs will be used in the MiniCBM readout chain [5], and are still used as a prototyping and development platform for CBM readout. Therefore, the DPB firmware has to support various configurations of the Front End Boards (FEBs) connected by Common Readout Boards (CROBs), which in turn requires the high level, parametrized HDL implementation.

## 2. General organization of the DPB firmware

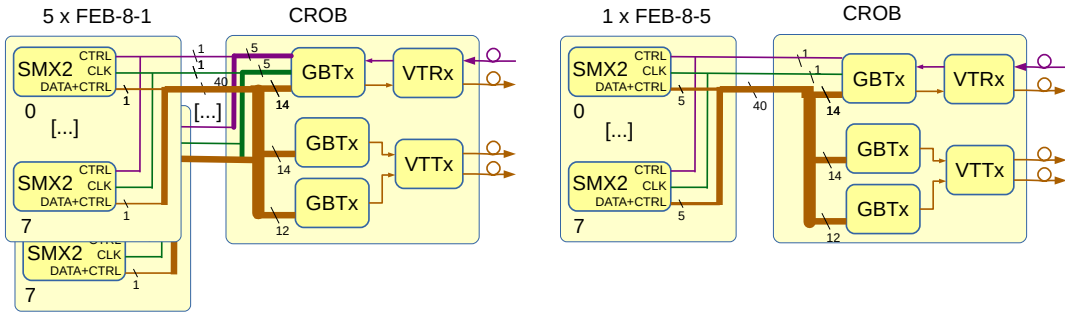
The main components of DPB firmware are shown in Figure 2. The IPbus controller provides the possibility to access registers in the firmware and control other IP blocks. Other infrastructure blocks contain independent clock generators, SPI, and I2C controllers. The TFC slave block receives the experiment reference clock and synchronization pulses (PPS). The received clock is converted in the White Rabbit-like clock recovery block into synchronous low-jitter clocks for DPB internal logic and GBT transceivers. The main DPB datapath component is the Detector Specific Block with FEB controller, data concentrator and preprocessor. The aggregated data from that block are further sent by the data transmitter block (based on the FLIM module [6]) via an optical link to the data acquisition system.



**Figure 2:** The general block diagram of the DPB firmware. PPS stands for “Pulse per second” synchronization signal

30 **3. The flexible architecture of the Detector Specific Block**

31 The Detector Specific Block provides GBTx-based [7] communication with the detector-  
 32 specific FEE using the slightly modified GBT-FPGA [8] core. At the FEE side, the GTBx ASIC  
 33 provides SPI-like e-Links. Their number depends on the data rate. In the CBM readout chain,  
 34 in most cases the GBTx chip will be used with 160 Mbps downlink and 320 Mbps uplink rate,  
 35 providing up to 14 e-Links. Each GBTx with the bidirectional link (master) may control two additional  
 36 GBTx chips connected only to uplinks (slaves). Therefore the most complex variant of  
 37 Common Readout Board (CROB) uses three GBTx chips and supports up to 42 e-Links (however  
 38 up to 40 will be used) [9]. Detectors using the STS-MUCH-XYTER2 (SMX2) readout ASIC [10]  
 39 may use between 1 and 5 uplinks, depending on the expected volume of data. Therefore, the DPB  
 40 firmware must be able to handle different connection scenarios. The two boundary cases are shown  
 in Figure 3.



**Figure 3:** Two boundary cases of FEE connections. The number of SMX2 ASICs connected to a single CROB may vary between 8 and 40 (based on [9]).

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42 **3.1 Flexible routing of data frames for FEE with the SMX2 ASIC**

43 Communication with SMX2 FEE ASICs uses the dedicated protocol [11]. Control commands  
 44 to SMX2 chips are sent by "SMX2 command transmitters". The uplink data stream sent by ASICs  
 45 contains confirmations of those commands, responses to them, timestamps, and the hit data. The  
 46 first two of them must be delivered to the appropriate transmitter, while others are sent to the

47 sorter system, and then to the FLIM module. Because the uplink frames are received by inde-  
 48 dependent "SMX2 receivers", it requires a frame routing system dependent on the connected FEB  
 49 boards. A fully flexible solution requires a programmable switch matrix that routes 24-bit words  
 50 between 40 inputs and 240 outputs. However, such IP core would require a huge amount of FPGA  
 51 resources. Currently, the firmware allows for runtime selection from one of predefined response  
 52 routing schemes. Another option is to use parametrized VHDL code to compile different, opti-  
 mized versions of firmware for various used configurations of FEBs.

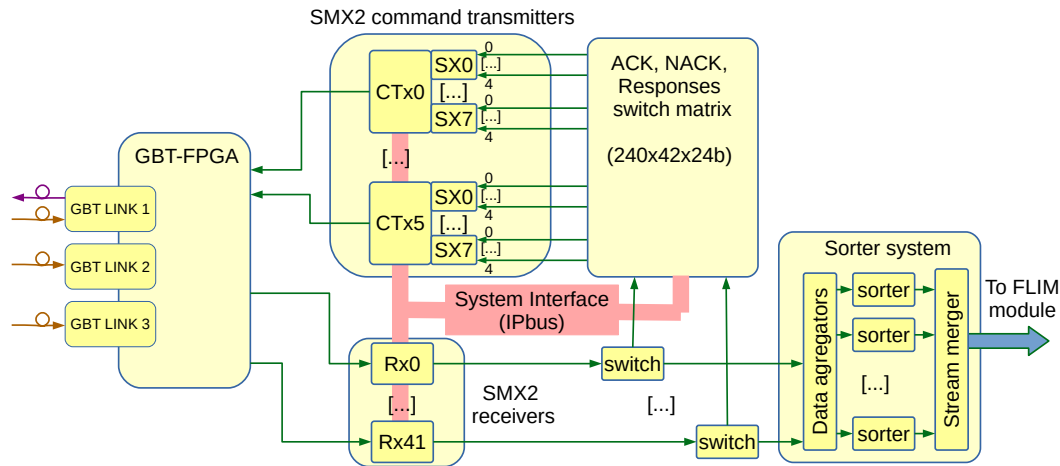


Figure 4: The general block diagram of the DPB firmware.

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### 54 3.2 Organization of register access in flexible firmware

55 In prototyping usage, and in case of generation of specialized firmware for specific FEB  
 56 configurations it is necessary to vary the number of different blocks (e.g., numbers of supported  
 57 CROBs, SMX2 chips connected to a single downlink, uplinks used by a single SMX2). That may  
 58 be achieved by parametrized VHDL code. However, it imposes the variability of the number of  
 59 registers and requires modification of the address space. A dedicated Python module was created  
 60 that allows describing a multilevel hierarchical structure of registers and blocks and automating the  
 61 generation of address map. The output is the VHDL package, the Python module, and the IPbus  
 62 address map. The solution may be easily adapted for other than IPbus communication channels,  
 63 like PCIe or AXI.

### 64 3.3 Aggregation and sorting of hit data

65 Data aggregation block is responsible for packing the data into so-called MicroSlices (MCs)  
 66 containing samples acquired by multiple FEB's in a configurable period of time. Each FEB times-  
 67 tamps the acquired samples and sends them via up to 5 serial links. The SMX2 operating principle  
 68 allows hits to be sent out of order. Therefore, the DPB firmware aggregates the hits from multiple  
 69 links into pipelines with rate up to 80 Mhits/s and passes them via a Heap Sorter module. After  
 70 that, each pipeline is strictly sorted by the acquisition time. Sorted pipelines are merged by a ded-

71 icated merger. The merger works at 160 MHz clock frequency, processing two samples in each  
72 clock cycle and producing the sorted stream with rate up to 320 Mhits/s for the 10 Gb/s FLES link.

#### 73 4. Conclusions

74 The GBT-oriented firmware for DPB boards is a complex and highly reconfigurable digital sys-  
75 tem. To achieve the required level of flexibility, it was necessary to implement it in a parametrized  
76 high-level VHDL code. For even greater flexibility (e.g., for automatic generation of registers with  
77 associated IPbus address tables), it was necessary to create new solutions based on an automatic  
78 generation of the VHDL, XML and Python code from the common description of the system.  
79 The system may be a good example of the flexible and parametrized control and data processing  
80 firmware. The firmware is currently used in the development of readout chain for MiniCBM and  
81 CBM.

#### 82 5. Acknowledgment

83 Work was supported by GSI.

#### 84 References

- 85 [1] “The CBM experiment.” <https://fair-center.eu/for-users/experiments/cbm.html>.
- 86 [2] W. Zabolotny, G. Kasprowicz et al., *Versatile prototyping platform for Data Processing Boards for*  
87 *CBM experiment*, *Journal of Instrumentation* **11** (Feb., 2016) C02031.
- 88 [3] W. M. Zabolotny, G. H. Kasprowicz et al., *Selection of hardware platform for CBM Common Readout*  
89 *Interface*, *Proc. SPIE* **10445** (Aug., 2017) 1044549.
- 90 [4] W. M. Zabolotny, A. P. Byszuk et al., *CRI board for CBM experiment: preliminary studies*, *Proc.*  
91 *SPIE* **10808** (Oct., 2018) 108083X.
- 92 [5] “mCBM@SIS18.” [https://fair-center.eu/fileadmin/fair/experiments/CBM/documents/mcbm-](https://fair-center.eu/fileadmin/fair/experiments/CBM/documents/mcbm-proposal2GPAC-WebVersion0619-SVN7729.pdf)  
93 [proposal2GPAC-WebVersion0619-SVN7729.pdf](https://fair-center.eu/fileadmin/fair/experiments/CBM/documents/mcbm-proposal2GPAC-WebVersion0619-SVN7729.pdf).
- 94 [6] D. Hutter, J. d. Cuveland and V. Lindenstruth, *CBM First-level Event Selector Input Interface*  
95 *Demonstrator*, *Journal of Physics: Conference Series* **898** (Oct., 2017) 032047.
- 96 [7] “GBTX manual.” <https://espace.cern.ch/GBTProject/GBTX/Manuals/gbtXManual.pdf>.
- 97 [8] M. B. Marin, S. Baron et al., *The GBT-FPGA core: features and challenges*, *Journal of*  
98 *Instrumentation* **10** (Mar., 2015) C03021.
- 99 [9] J. Lehnert, A. Byszuk et al., *GBT based readout in the CBM experiment*, *Journal of Instrumentation*  
100 **12** (Feb., 2017) C02061.
- 101 [10] K. Kasinski, R. Szczygiel and W. Zabolotny, *Back-end and interface implementation of the*  
102 *STS-XYTER2 prototype ASIC for the CBM experiment*, *Journal of Instrumentation* **11** (Nov., 2016)  
103 C11018.
- 104 [11] K. Kasinski, R. Szczygiel, W. Zabolotny et al., *A protocol for hit and control synchronous transfer for*  
105 *the front-end electronics at the CBM experiment*, *NIM-A* **835** (Nov., 2016) 66–73.