TWEPP 2018 Topical Workshop on Electronics for Particle Physics

Tuesday, 18 September 2018

Posters: Posters session - 1 ASIC - **FBS 0.01/0.02 (Feestzaal) (17:20 - 18:50)**

  -Conveners: Ken Wyllie

[id] title	presenter	board
[18] An integrated SRAM radiation monitor in 180 nm CMOS technology	PRINZIE, Jeffrey	
[183] A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC	NODARI, Benedetta	
[179] Design and characterization of a high speed transmitter circuit for the ATLAS/CMS HL-LHC pixel readout chip	WANG, Tianyang	
[178] A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase II Upgrades	SCARFI', Simone	
[114] The Quality Assurance of two ASICs for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade	XIAO, Le	
[96] A high integration and low power ASIC with TOT front-end and waveform sampling for MRPC applications	REN, Jiayi	
[160] A Capacitor DAC for Charge Redistribution Analog to Digital Converter with Successive Approximation	Mr VANCURA, Pavel	
[140] Prototype Front-end ASIC for Silicon-strip Detectors of J-PARC Muon g-2/EDM Experiment	Mr TSUTSUMI, Yuki	
[147] A 130 nm CMOS PLL for Phase-II ATLAS-MDT TDC	RESTA, Federica	
[146] A 28 nm Fast Tracker Front-end for sMDT Detectors at Future Hadron Colliders	MANGIAGALLI, Luca	
[121] Application Of Multiple Use SiPM Integrated Circuit (eMUSIC) For Readout Based Time-Of-Flight Detectors	SANMUKH, Anand	
[68] An UVM-based verification environment for the lpGBT 10 Gbps transceiver ASIC	CASTRO FONSECA, Jose Pedro	
[150] A Topmetal-based and High-Performance Resistance Measurement Circuit for the Thin-Film Sensitive Gas Detection	Dr AN, Mangmang	
[115] An Ultra-Fast 10Gb/s 64b66b Data Serialiser Back-end in 65nm CMOS Technology	Mr GARDINER, Thomas	
[169] ASoC: A High Performance Waveform Sampling and Feature Extraction System-on-Chip for Data Acquisition	MOSTAFANEZHAD, Isar	
[57] MuPix9 - a HV-MAPS prototype with serial powering	WEBER, Alena Larissa	
[27] Design of HVCMOS pixel sensor ASIC with on-chip readout electronics for ATLAS ITk Upgrade	PRATHAPAN, Mridula	
[47] A Sigma-Delta ADC for Pixel Charge Readout Targeting Neutrinoless Double-Beta Decay Search in High-Pressure TPC	Mr HUANG, Xing	
[34] A rad-hard full information pixel imager chip for the HEPS-TF project	Dr WEI, Wei	
[10] Development and performance of the new front-end ASIC for the ATLAS MDT chambers at the HL-LHC	RICHTER, Robert	

[9] Design of a monolithic HR-CMOS sensor chip for the CLIC silicon tracker	KREMASTIOTIS, Iraklis	
[8] ABACUS : Two fast amplifiers for the readout of LGAD detectors	MAZZA, Giovanni	
[163] A 10 GSa/s Waveform Sampling ASIC with Multi-Event Buffering Capability	PORTER, John	
[110] A High Dynamic Range ASIC for Time of Flight PET with monolithic crystals	Dr GÓMEZ FERNÁNDEZ, Sergio	
[87] Study of Time of Arrival Measurement with Constant Fraction Discrimination Using Switched Capacitor Sampling or Bucket-Brigade Analog Time Delay Line	Dr DEPTUCH, Grzegorz	
[67] Design and status of custom-designed ASICs for the Phase-I upgrade of the ATLAS muon spectrometer	MATAKIAS, Dimitrios	
[72] The Quality-Assurance Test of the ATLAS New Small Wheel Read-Out Controller ASIC	POPA, Stefan	
[113] The Readout and Data Transmission of a Monolithic Active Pixel Sensor prototype for the CEPC Vertex Detector	XIAO, Le	
[95] A Low-Noise Charge-Sensitive Amplifier for Gain-less Charge Readout in High-pressure TPC	Dr GAO, Chaosong	
[39] Algorithms for Threshold Dispersion Minimization of the CHIPIX65 Asynchronous Front-End	SONZOGNI, Mauro	

Posters: Posters session - 1 Optoelectronics and Links - FBS 0.01/0.02 (Feeszaal) (17:20 - 18:50)

 -**Conveners: Ken Wyllie**

[id] title	presenter	board
[181] MULTI-GIGABIT PHOTONIC TRANSCEIVERS FOR HARSH ENVIRONMENT APPLICATIONS	THOMSON, Ross	
[73] Precision Clock Distribution studies for timing in phase II upgrade of the CMS experiment	BAUSSON, Pierre-Anne	
[162] Thermal characterisation of the Versatile Link PLUS Transceiver	SOOS, Csaba	
[176] New LpGBT-FPGA IP: Simulation model and first implementation	MENDEZ, Julian Maxime	
[32] In-situ Radiation Damage Studies of VCSELs and p-i-n diodes in the ATLAS SemiConductor Tracker	POWNALL, Gavin	
[164] Concept, design and verification of components for an integrated on-detector silicon photonic multi-channel transmitter unit	ZHANG, Yunlong	

Posters: Posters session - 1 Programmable Logic, Design Tools and Methods - FBS 0.01/0.02 (Feeszaal) (17:20 - 18:50)

 -**Conveners: Ken Wyllie**

[id] title	presenter	board
[80] Remote control unit of the LHC injector complex BLM system	CALVO GIRALDO, Eva	
[143] An automated pipeline for continuous integration of FPGA firmware and software for the LHCb Run3 upgrade	DURANTE, Paolo	
[55] Ethernet-based slow control system for parallel configuration of FPGA-based front-end boards	Dr ZABOŁOTNY, Wojciech	
[43] GBT oriented firmware for Data Processing Boards for CBM	Dr ZABOŁOTNY, Wojciech	

[98] FPGA Based Time Measurement for the MRPC Detector	ZHANG, Jie	
[128] FPGA Implementation of an Artificial Neural Network for Subatomic Physics Experiment Particles Recognition	ZHAO, Ruiguang	
[134] Machine learning: hit time finding with a neural network	THALMEIER, Richard	
[172] A possible implementation of a detector specific extension of the FELIX firmware for the ITk Pixel subdetector	DULSEN, Carsten	

Thursday, 20 September 2018

Posters: Posters session - 2 Other - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

-**Conveners: Ken Wyllie**

[id] title	presenter	board
[100] GSPS: a 1 GS/s sampling digitiser designed with interleaved architecture for the LaBr3 detectors of the FAMU experiments.	TRAVAGLINI, Riccardo	
[106] A bipolar shaping amplifier for low background alpha/beta counters with silicon detectors.	Mr THYS, Sam	
[125] Optimizing Time Resolution for Large Area Silicon Photomultipliers	Dr GÓMEZ FERNÁNDEZ, Sergio	

Posters: Posters session - 2 Power, Grounding and Shielding - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

-**Conveners: Ken Wyllie**

[id] title	presenter	board
[174] Hybrid GaN and CMOS integrated module radiation hard DC-DC converter	MIKKOLA, Esko	
[22] High-Voltage Silicon JFET for HV Multiplexing for the ATLAS MicroStrip Staves	Dr GIACOMINI, Gabriele	

Posters: Posters session - 2 Production, Testing and Reliability - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

-**Conveners: Ken Wyllie**

[id] title	presenter	board
[48] Front-end hybrids for the strip-strip modules of the CMS Outer Tracker Upgrade	GADEK, Tomasz	
[37] MrRobot: an automated ASIC testing rig	Mr CASAJUS RAMO, Adrian	
[35] Production and Quality Assurance of Mu2e Silicon PhotoMultipliers	MORESCALCHI, Luca	
[124] Quality control and reliability testing of the front end electronics production for the upgrade of the LHCb RICH detectors	NERI, Ilaria	
[148] Front-end Electronics of the Forward Strip Detector for the ATLAS HL-LHC Upgrade	GARCIA ARGOS, Carlos	
[142] First Double-Sided End-Cap Strip Module for the ATLAS High-Luminosity Upgrade	WIIK-FUCHS, Liv	

Posters: Posters session - 2 Radiation Tolerant Components and Systems - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

-**Conveners: Ken Wyllie**

[id] title	presenter	board
[133] Characterization of Soft Error Rate against Memory Elements Spacing and Clock Skew in Logic with Triple Modular Redundancy in a 65nm Process	Dr MIRYALA, Sandeep	
[89] The Upgraded Microstrip Silicon Sensor Characterisation Facility of the University of Sheffield	KOURLITIS, Evangelos	
[97] Delay Locked Loop for use in a time-to-digital converter with quick recovery and low hysteresis	Mr VAN BOCKEL, Bjorn	

[103] Radiation tests and production test strategy for the ALICE TOF readout upgrade board	Dr FALCHIERI, Davide	
[11] ATLAS Tile Calorimeter Link Daughter Board	Mr VALDES SANTURIO, Eduardo	
[21] Investigation of Single Event Latch-up effects in the ALICE SAMPA ASIC	MAHMOOD, Sohail Musa	
[111] Radiation tolerant conditioning electronics for vacuum measurements	Mr CHATZIGEORGIOU, Nikolaos	

Posters: Posters session - 2 Systems, Planning, Installation, Commissioning and Running Experience - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

  -Conveners: Ken Wyllie

[id] title	presenter	board
[132] The WaveCatcher systems: a family of powerful and low cost digitizers.	Mr BRETON, Dominique	
[127] ATLAS Phase-II-Upgrade Pixel Demonstrator Read-out	BUSCHMANN, Eric	
[119] Novel Si-Sensor technology for high resolution and high repetition-rate experiments at accelerator facilities	PATIL, Meghana Mahaveer	
[116] ATLAS Phase-II-Upgrade Pixel Data Transmission Development	GROSSE-KNETTER, Joern	
[177] New 63U ATCA rack: thermal performances and integration challenge	KALINOWSKI, Michal Tomasz	
[4] The CMS phase 2 ECAL front end electronics upgrade	BAUSSON, Pierre-Anne	
[144] Design of the Back end card for the JUNO experiment	YANG, yifan	
[156] The PaDiWa-AMPS2 TDC and QDC front-end electronics for the HADES Electromagnetic Calorimeter	Mr ROST, Adrian	
[64] The Embedded Local Monitor Board upgrade proposals	NICPON, Kamil Szymon	
[117] CMS ECAL Upgrade Front End card: design and prototype test results	SINGOVSKI, Alexander	
[102] Design and Test of the Analog to Digital Converter Unit for the JUNO Readout Electronics	HU, Jun	
[151] Design and performance of CMS Muon Triple-GEM Detector Control System	DE LENTDECKER, Gilles	
[153] CMS Drift Tubes Readout Phase 1 Upgrade	NAVARRO TOBAR, Alvaro	
[26] Electronics Developments for Phase-2 Upgrade of CMS Drift Tubes	TRIOSSI, Andrea	
[71] Level-1 Data Driver Card - A high bandwidth radiation tolerant aggregator board for detectors	GKOUNTOUMIS, Panagiotis	
[84] FPC design and testing for the High-Granularity Timing Detector for the Phase II upgrade of the ATLAS calorimeter system	ROBLES MANZANO, Maria	

Posters: Posters session - 2 Trigger - FBS 0.01/0.02 (Feestzaal) (17:00 - 18:30)

  -Conveners: Ken Wyllie

[id] title	presenter	board
[93] Towards a heterogeneous High Level Trigger farm for CMS	Dr BOCCI, Andrea	
[62] Input Mezzanine Board for the Fast Tracker(FTK) at ATLAS	MITANI, Takashi	
[180] Development and testing of a Trigger Processor Card based on a Kintex Ultrascale FPGA	MALLIOS, Stavros	

[70] Study of Retina Algorithm on FPGA for Fast Tracking	DENG, Wendi	
[19] New development in the CMS ECAL Level-1 trigger system to meet the challenges of LHC Run 2	THIANT, Floris	
[145] Ultraflex: An ATCA Prototype Board for the CMS Phase 2 Tracker Upgrade	ARDILA, Luis	
[15] A Lightweight First-Level Muon Track Trigger for Future Hadron Collider Experiments	CIERI, Davide	
[24] The CMS Level-1 muon triggers for the LHC Run II	HEIKKILAE, Jaana	
[88] A novel 4D fast track finding system using precise space and time information of the hit	GANDINI, Paolo	