TWEPP 2018
FPGAs & Timing Working Group
Summary

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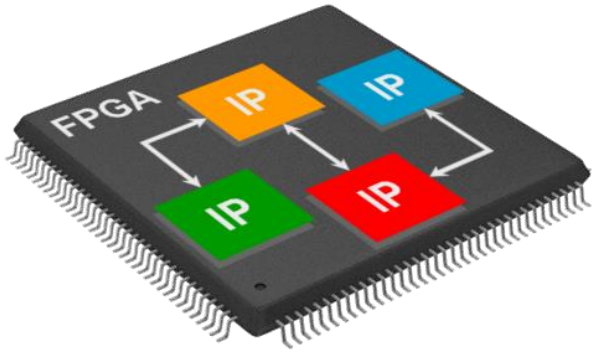
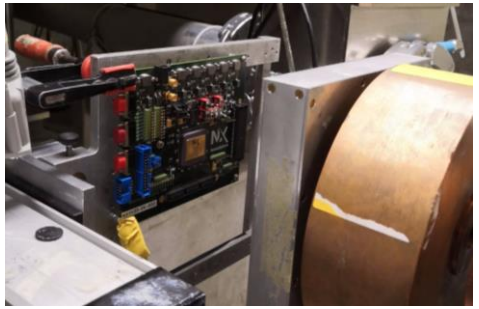


Summary:

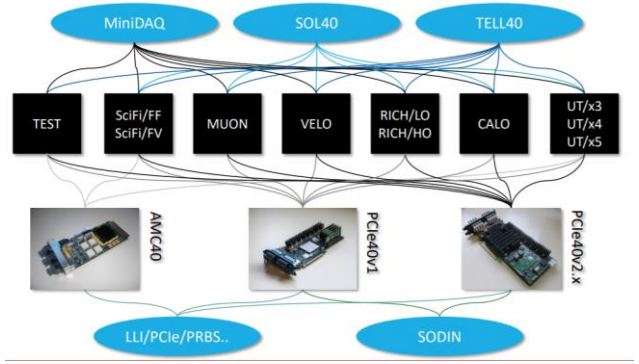
- This year we have decided to mix FPGA and Timing for the first time
- ~50 participants
- Most of the participants were interested in both the topics
- 5 Presentations divided in
  - 3x FPGA
  - 2x Timing

FPGA

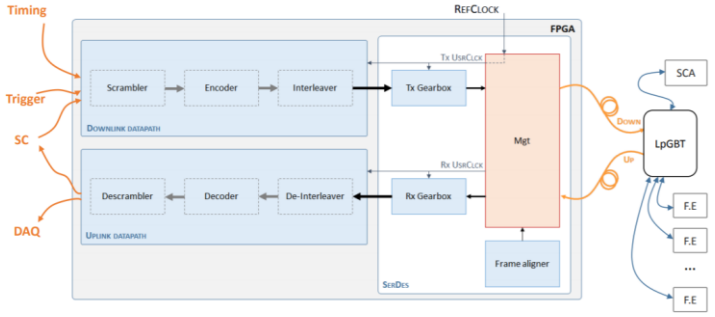
- NanoExplore rad-hard FPGA radiation tests for CERN applications – *Salvatore Danzeca*
  - *First irradiation test results on the NanoExplore NG-MEDIUM radhard FPGA for CERN application using 200 MeV proton beam*



- Case-study of continuous integration of FPGA firmware and software - *Paolo Durante*
  - *A pragmatic way of maintaining, compiling and testing firmware and software for multiple experiments based on gitlab*

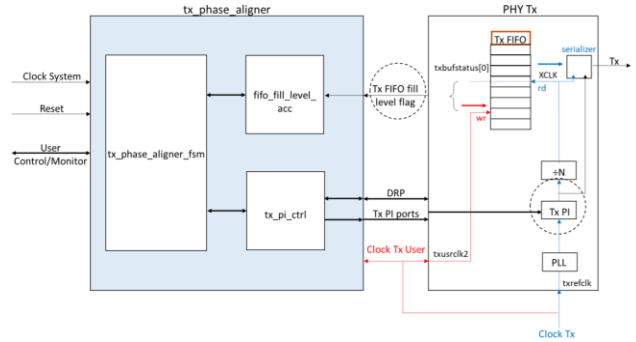


- Introduction to the lpGBT-FPGA - *Julian Maxime Mendez*
  - Status and implementation of the LpGBT-FPGA, the FPGA counterpart of the LpGBT ASIC

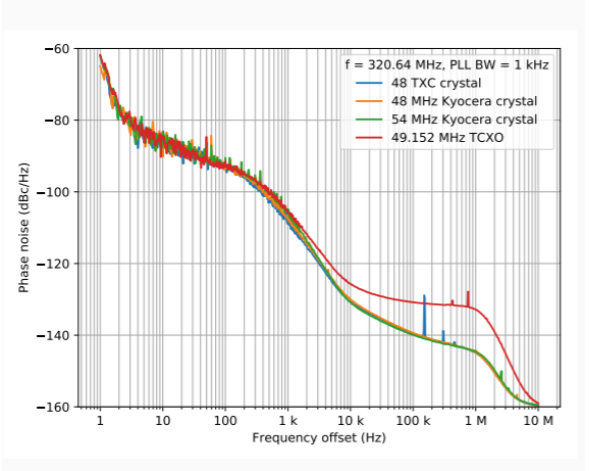


Timing

- Implementing the High Precision Timing IP for Xilinx Ultrascale FPGA transceivers - Eduardo Mendes
  - Fixed-phase after a link start-up? Possible with the HPTD IP core architecture



- Phase Noise Studies on the Si5345 PLL - Jeroen Hegeman
  - Validate choice of jitter attenuator (Si5345) evaluating the phase noise under different conditions (temperature, Changing output frequency, Changing PLL bandwidth, crystal or temperature compensated crystal oscillator)



Thank you!