Power Working group Summary

Legacy

- The power working group was started some years ago with primary goal to evluate and compare the DCDC converter vs. serial power schemes for the tracking detectors for LHC phase 2.
- Results in, essentially, DCDC power for the outer trackers and a mix of serial power and DCDC converters for the inner trackers

Serial Power

- Demonstration of serial power essentially successful
- PWG recommends
  - Build rather long “chains” early and make available to non-experts to “break” the system
    - May me difficult due to shortage of hardware. To be solved.
  - ATLAS and CMS risk assessment similar but ATLAS attempts to mitigate the “open loop” failure mode with FET switches controlled external to the loop.

DCDC converters

- Main weakness or worry is the potential for additional noise injection
  - Demo has shown that the potential issue can be mitigated with careful layout

- Resent FEAST DCDC converter failures
  - 5% of the CMS phase 1 pixel detector, negligible impact on physics
  - Due to radiation induced leakage current into a node with no load when the converter is disabled leading to voltage build-up follows and two 3.3V transistors break down.
  - Risk zone ~700 kRad up to ~4 Mrad explaining why the issue was not discovered during radiation qualification
  - Understood and solved by adding a 3k bleed resistor on the node accessible on a package pin. Solution applicable to all versions of the ASIC.

New DCDC converter development

- Poster by Esko Mikkola
- 18V to 1.5V 7A
- External GaN FETs (COTS)
- Second version taped out
- Rad tol tests to be done but controller designed to be radiation tolerant to high levels (>100Mrad)
- High switching frequency of around 10 MHz => small inductor
- PWG suggests to add a switching phase control feature in order to allow operation of several DCDC converters in parallel
  - May be possible on future versions