

Stave0B - RCE readout test with COB

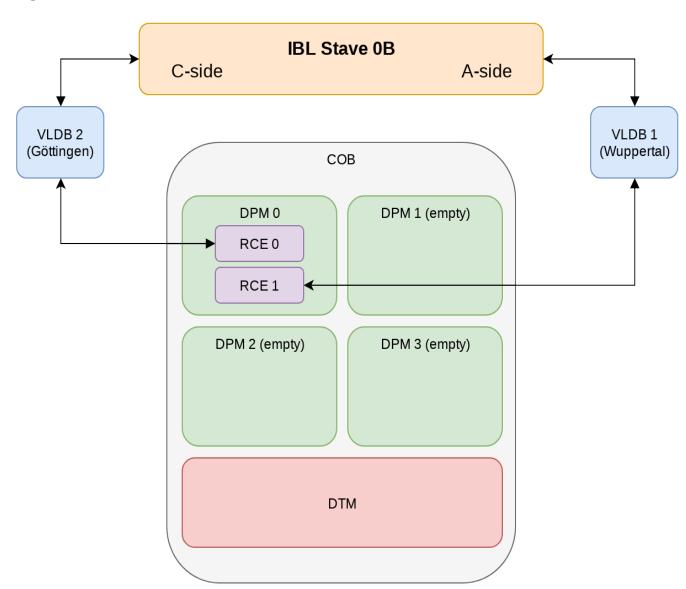


Introduction

- 2 weeks before Christmas Martin sent me a new DTM with on-board jitter cleaner.
- FW was prepared and tested: See DtmJitterCleaner branch in gitlab.
- Still issues with clock generation (timing?!) resulting in constant resets of the RMB PLL...
- Martin provided a firmware with no RMB PLL problem, which is working fine.



Connectivity





Test results so far

- Found 14 front-ends with good analog scan
- Inconsistencies
 with previous tests
 using the Kintex
 Ultrascale readout.
- Using pixel320.txt for the VLDB config
- Phase alignment in VLDB to be tested (maybe we can get more chips working)

front-end	RCE	Inlink	Outlink	Serial Number	Digital scan	Analog scan	Threshold
M1A1-1	1	0	0	n	-	-	
M1A1-2	1	0	1	n	-	-	
M1A2-1	1	2	2	у	у	у	у
M1A2-2	1	2	3	у	у	у	у
M2A3-1	1	4	4	n	-	-	-
M2A3-2	1	4	5	у	у	у	
M2A4-1	1	6	6	у	у	у	
M2A4-2	1	6	7	n	-	-	
M3A5-1	1	8	8	n	-	-	
M3A5-2	1	8	9	у	у	у	
M3A6-1	1	10	10	у	n	-	
M3A6-2	1	10	11	n	-	-	
M4A7-1	1	12	12	n	-	-	-*
M4A7-2	1	12	13	n	-	-	-*
M4A8-1	1	14	14	у	у	у	-*
M4A8-2	1	14	15	n	-	-	-*
M1C1-1	0	14	15	у	у	у	
M1C1-2	0	14	14	у	у	у	
M1C2-1	0	12	13	у	у	у	
M1C2-2	0	12	12	n	-	-	
M2C3-1	0	10	11	у	у	у	
M2C3-2	0	10	10	n	-	-	
M2C4-1	0	8	9	у	у	у	
M2C4-2	0	8	8	n	-	-	
M3C5-1	0	6	7	у	n	n	
M3C5-2	0	6	6	n	-	-	
M3C6-1	0	4	5	У	у	у	
M3C6-2	0	4	4	n	-	-	
M4C7-1	0	2	3	у	у	у	-*
M4C7-2	0	2	2	У	у	у	-*
M4C8-1	0	0	1	n	-	-	-*
M4C8-2	0	0	0	у	n	-	-*
		working	9	17			
		failed		15		3 1	
untested			0	1:	5 17	8	

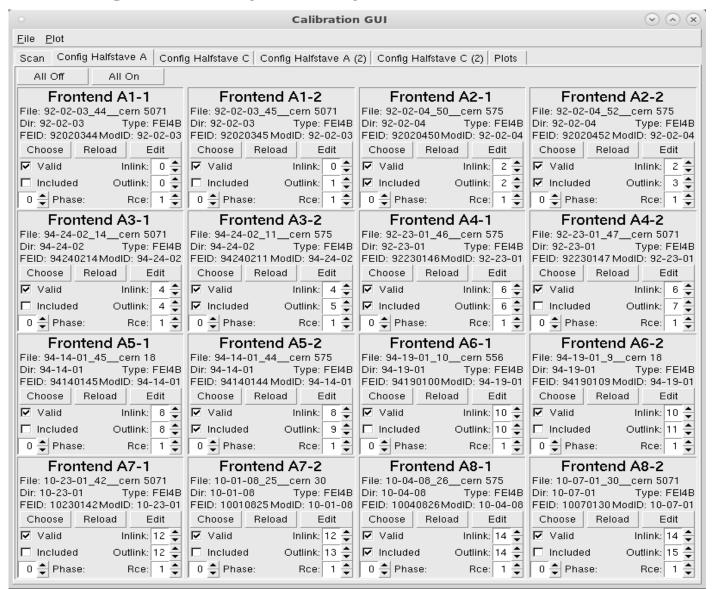


Summary

- Successful verification of the new DTM firmware
- RCE readout in Wuppertal has been set-up and is working fine
- Results of IBL stave measurements show some inconsitencies between different readout systems
 - I suspect the phase alignment settings in the VLDB have quite an effect...
 - Will do an manual tuning of the phases (I did already with the Kintex Ultrascale readout with some success)



calibGui configuration (A-side)





calibGui configuration (C-side)

