VMM and the SRS - update

Michael Lupberger (CERN)

What happened since December 2017

New student from Central China Normal University for 6 months

→ Yan, will work on DDR3 memory on the FECv_6 (FPGA coding)

BrightnESS test beam in December

→ → first neutron test beam with VMM3 hybrids (four) and better software (see presentation on last miniweek, data analysis still ongoing)

I2C test of new ADC for hybrid

→ Firmware implementation of new ADC for full functionality

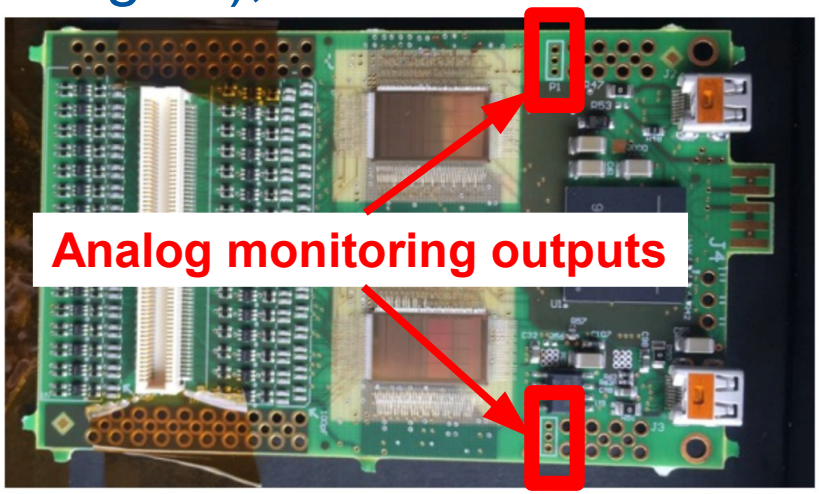
VMM3 hybrid noise test

→ currently ongoing

New ADC

Necessary to read monitoring outputs

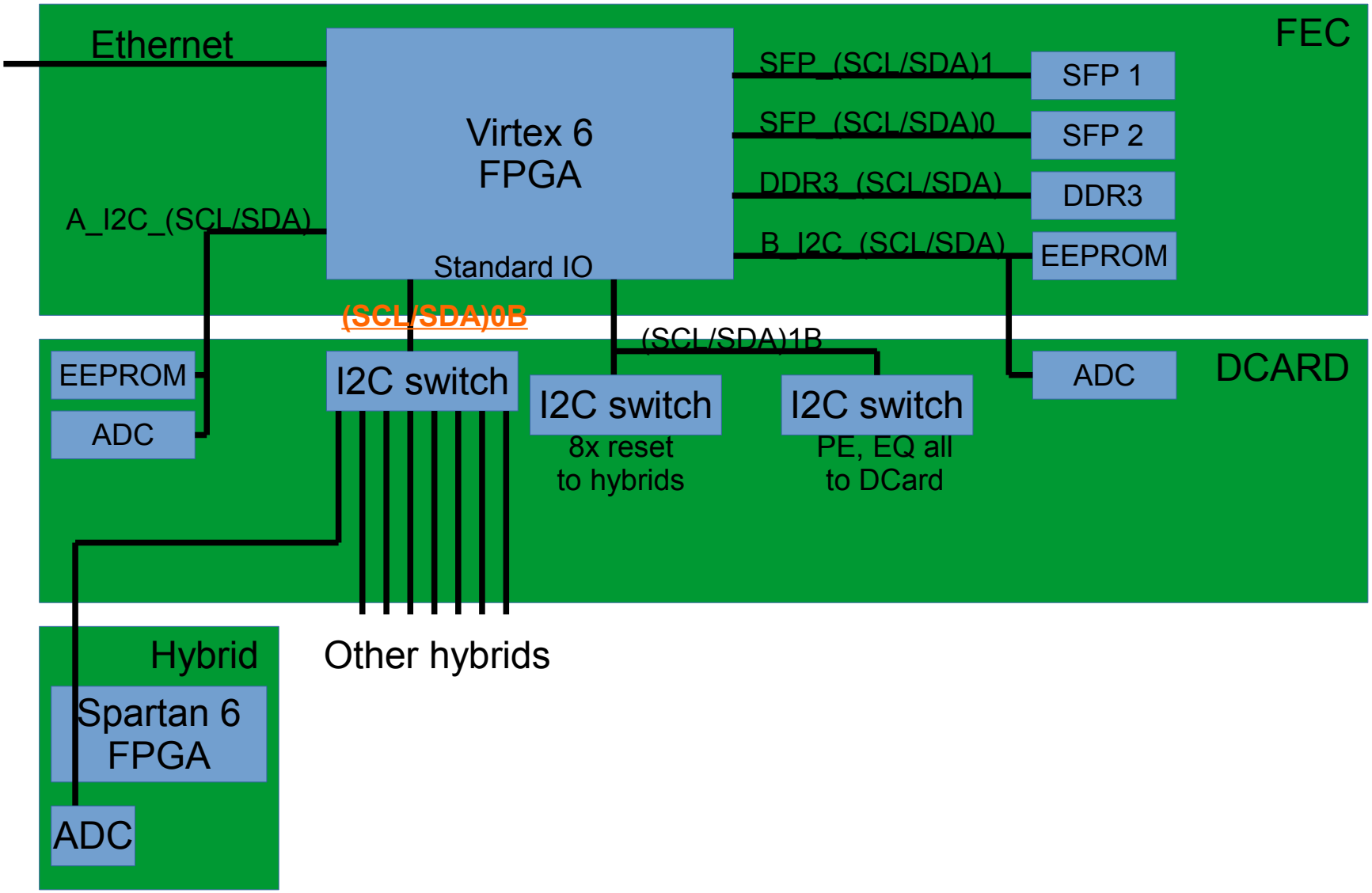
- M0: Can be set to output global threshold DAC, pulser DAC, temperature sensor level, band-gap reference
  and for every channel: baseline (and signal), threshold level
- tdo: baseline and ramp
- pdo: baseline and pulse amplitude



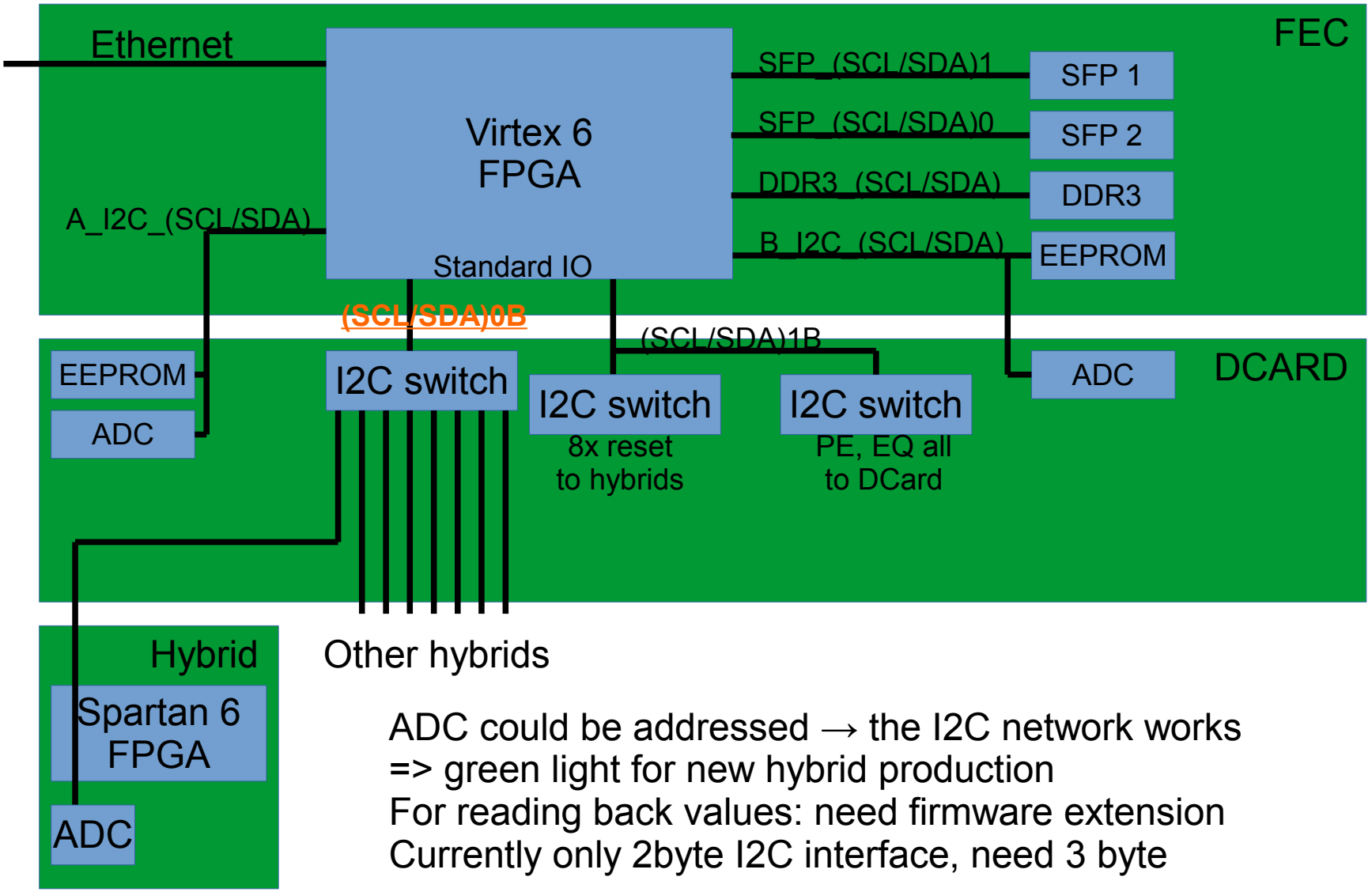
For fast signals (ramp, pulse), ADC is to slow

We need it for calibration of baselines and thresholds

I2C network

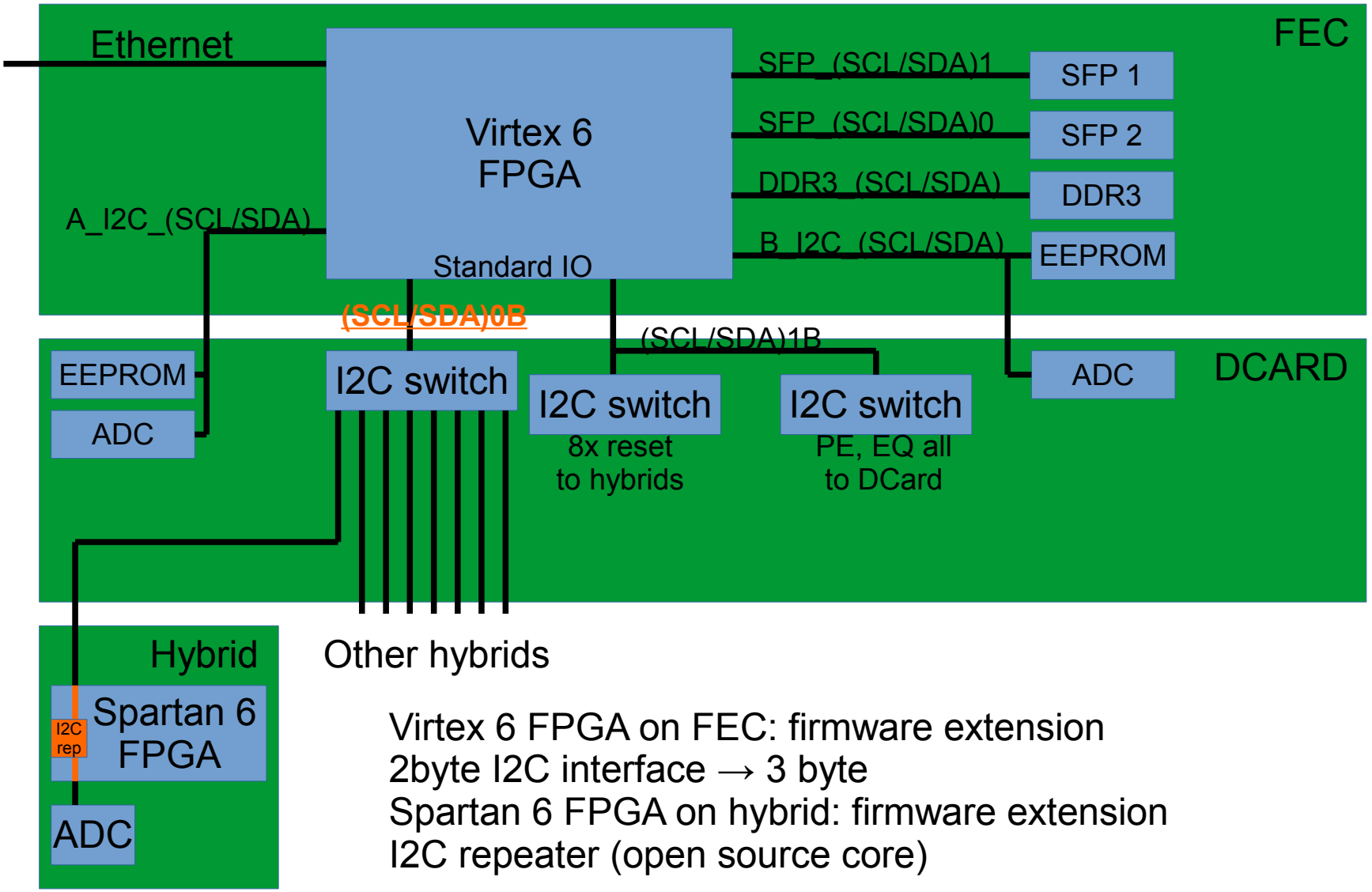

FEC
Ethernet
Virtex 6
FPGA
SFP_(SCL/SDA)1
SFP 1
SFP_(SCL/SDA)0
SFP 2
DDR3_(SCL/SDA)
DDR3
B_I2C_(SCL/SDA)
EEPROM
A_I2C_(SCL/SDA)
Standard IO
(SCL/SDA)0B
(SCL/SDA)1B
ADC
DCARD
EEPROM
ADC
I2C switch
I2C switch
8x reset
to hybrids
I2C switch
PE, EQ all
to DCard
Hybrid
Other hybrids
Spartan 6
FPGA
ADC

I2C network



ADC could be addressed → the I2C network works
=> green light for new hybrid production
For reading back values: need firmware extension
Currently only 2byte I2C interface, need 3 byte

I2C network



Virtex 6 FPGA on FEC: firmware extension
2byte I2C interface → 3 byte
Spartan 6 FPGA on hybrid: firmware extension
I2C repeater (open source core)

VMM3 noise test

Principle of measurement

Compare baseline rms (mV) with test pulse U_test (mV)

VMM internal test pulse has know charge (ΔU on C)

ΔU: measure TestPulse DAC at M0 output for x=0, and x=200

U_test: measure amplitude of test pulse at M0

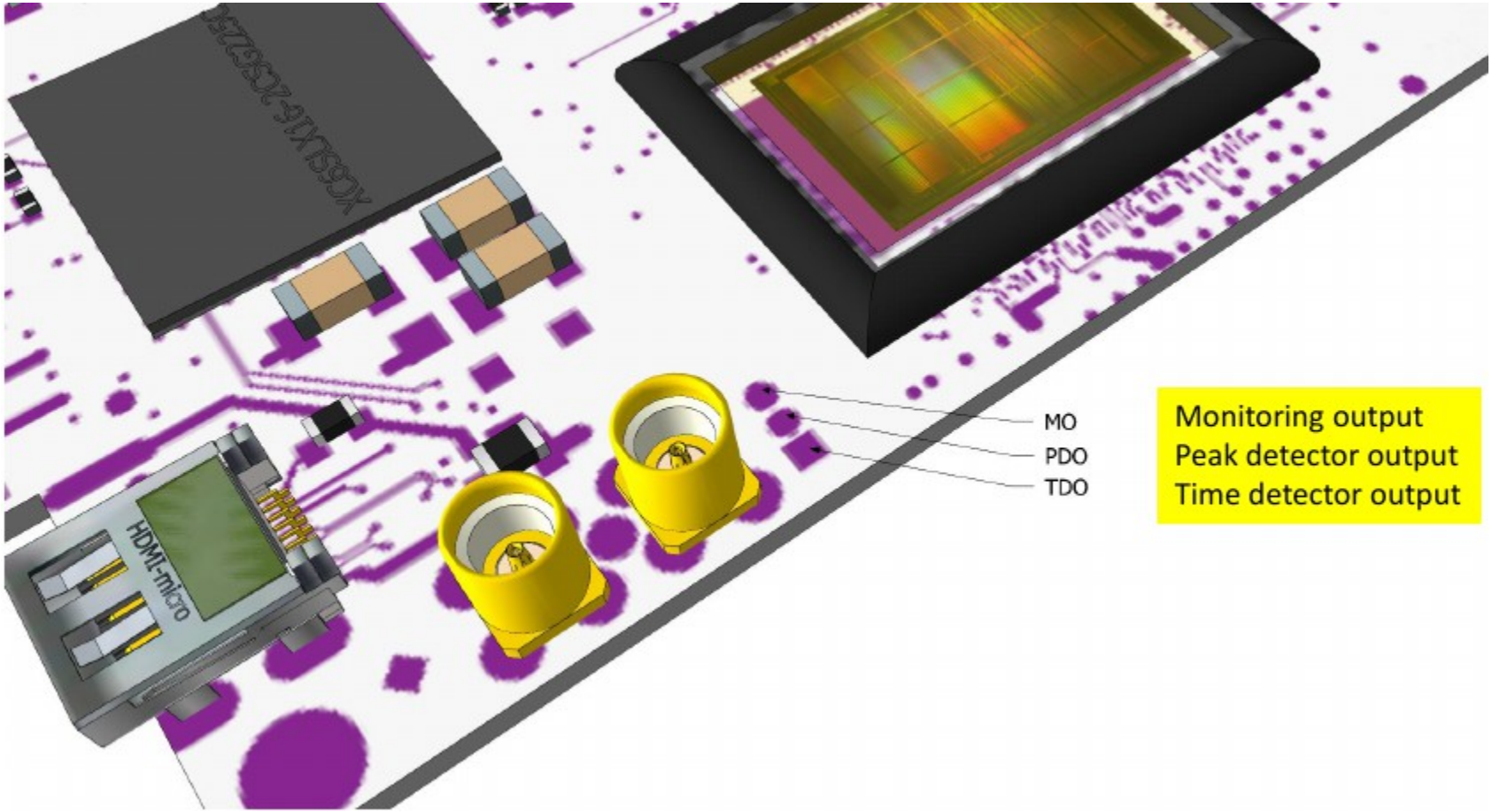
Baseline rms: measure without test pulse at M0

$$ENC = \frac{U_{rms}}{e-} \Big/ \frac{U_{peak}}{\Delta Q_s} = \frac{U_{test}\ Cs}{e-} * \frac{U_{rms}}{U_{peak}}$$

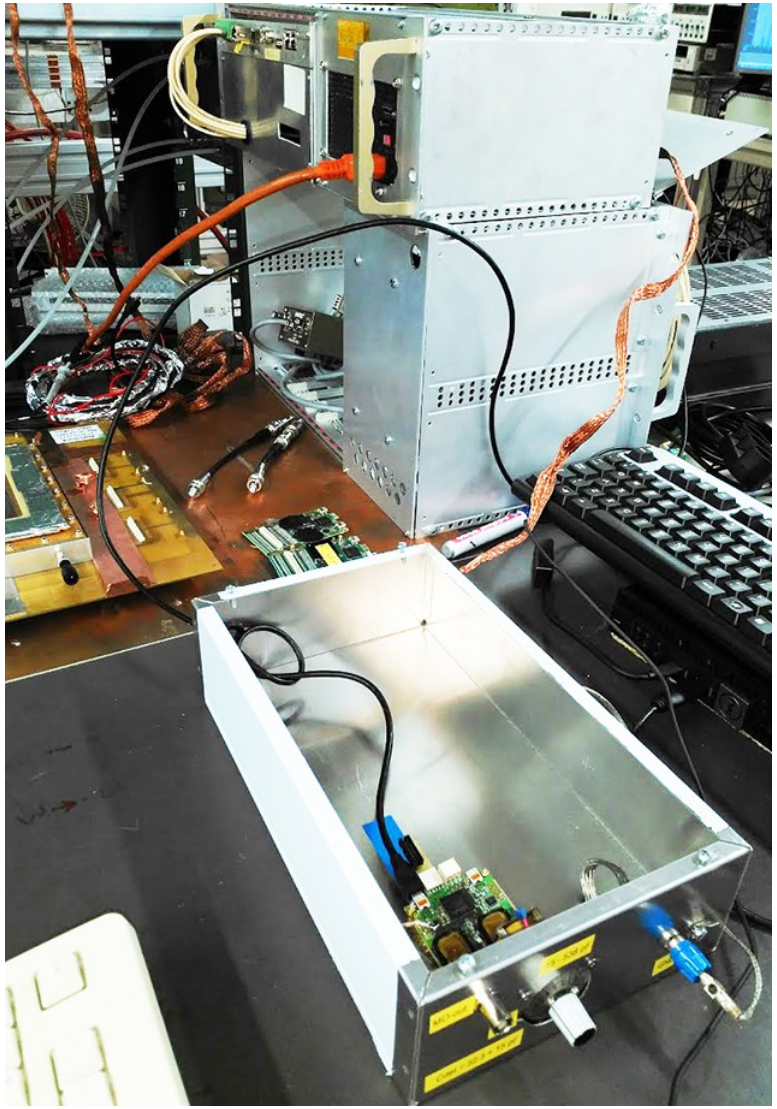
Cs = 300 fF

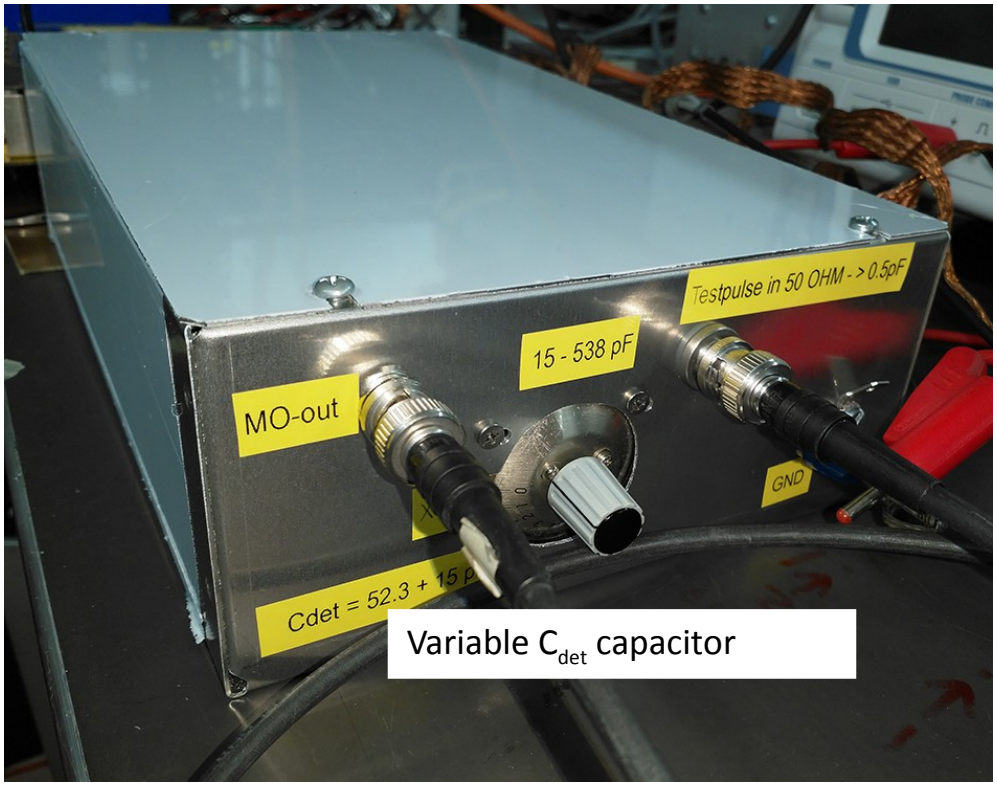
$$ENC[e-] = 1864.5 \frac{U_{rms}[mV]\ U_{test}[mV]}{U_{peak}[mV]}$$

VMM3 noise test



VMM3 noise test





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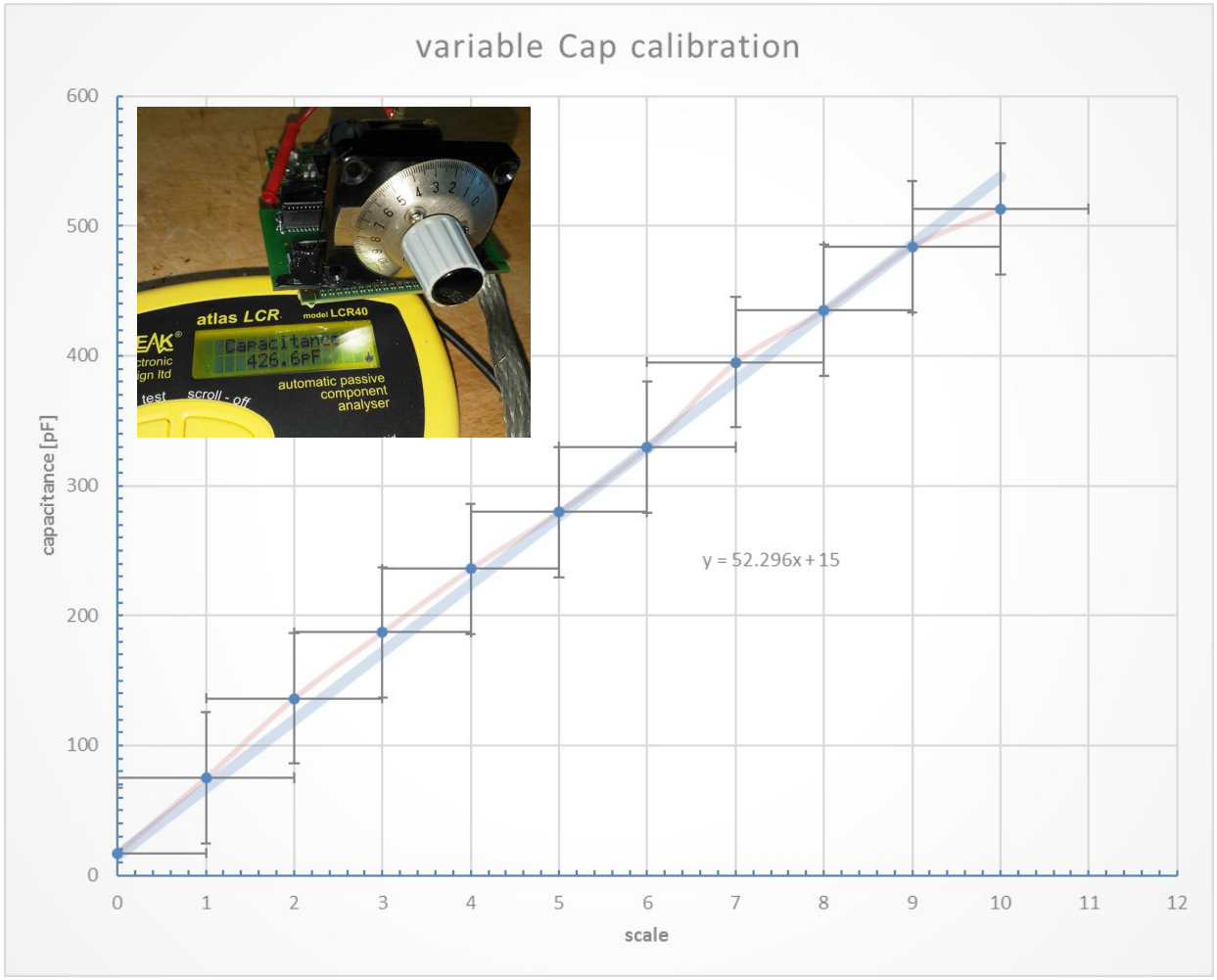

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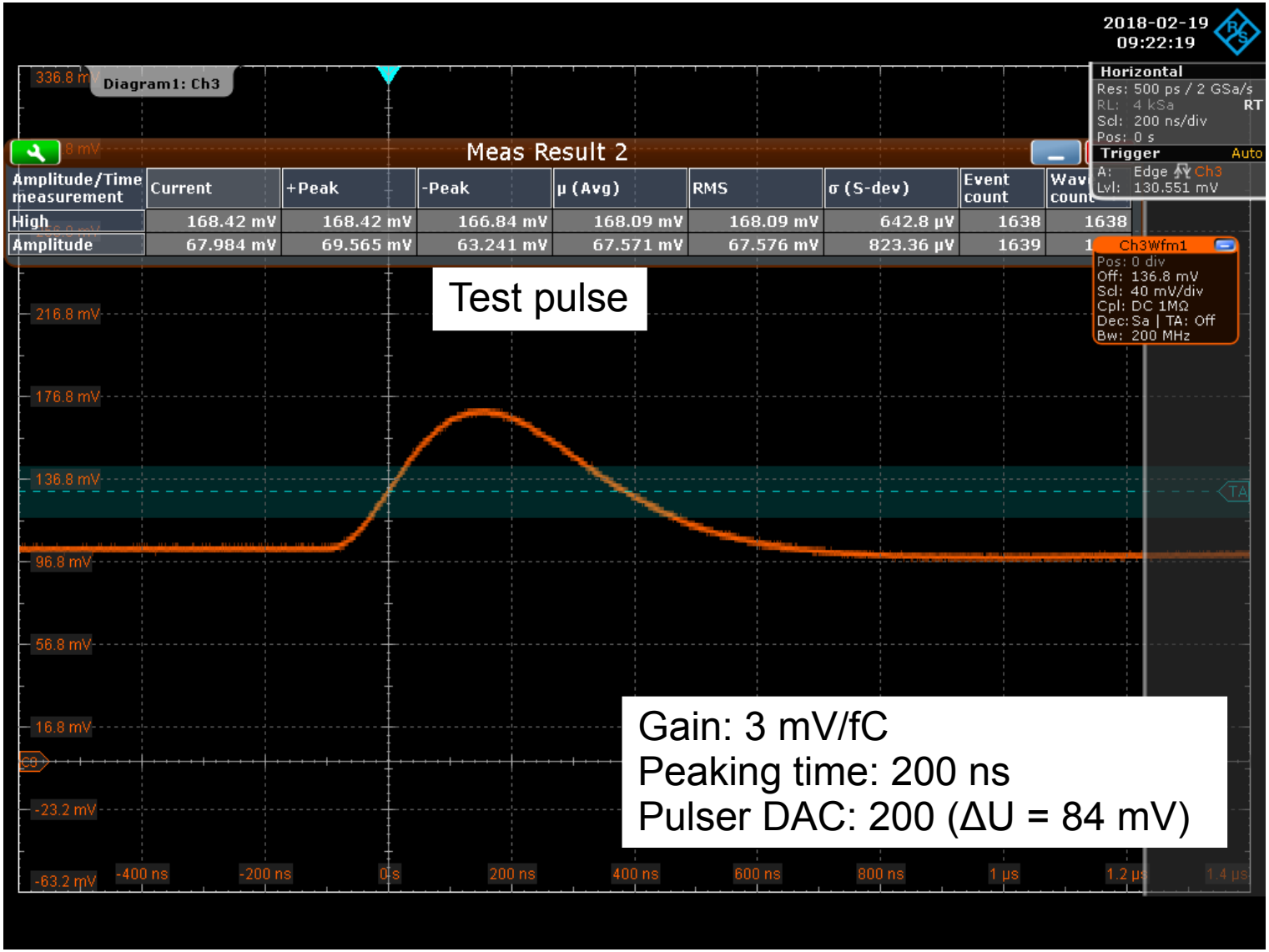
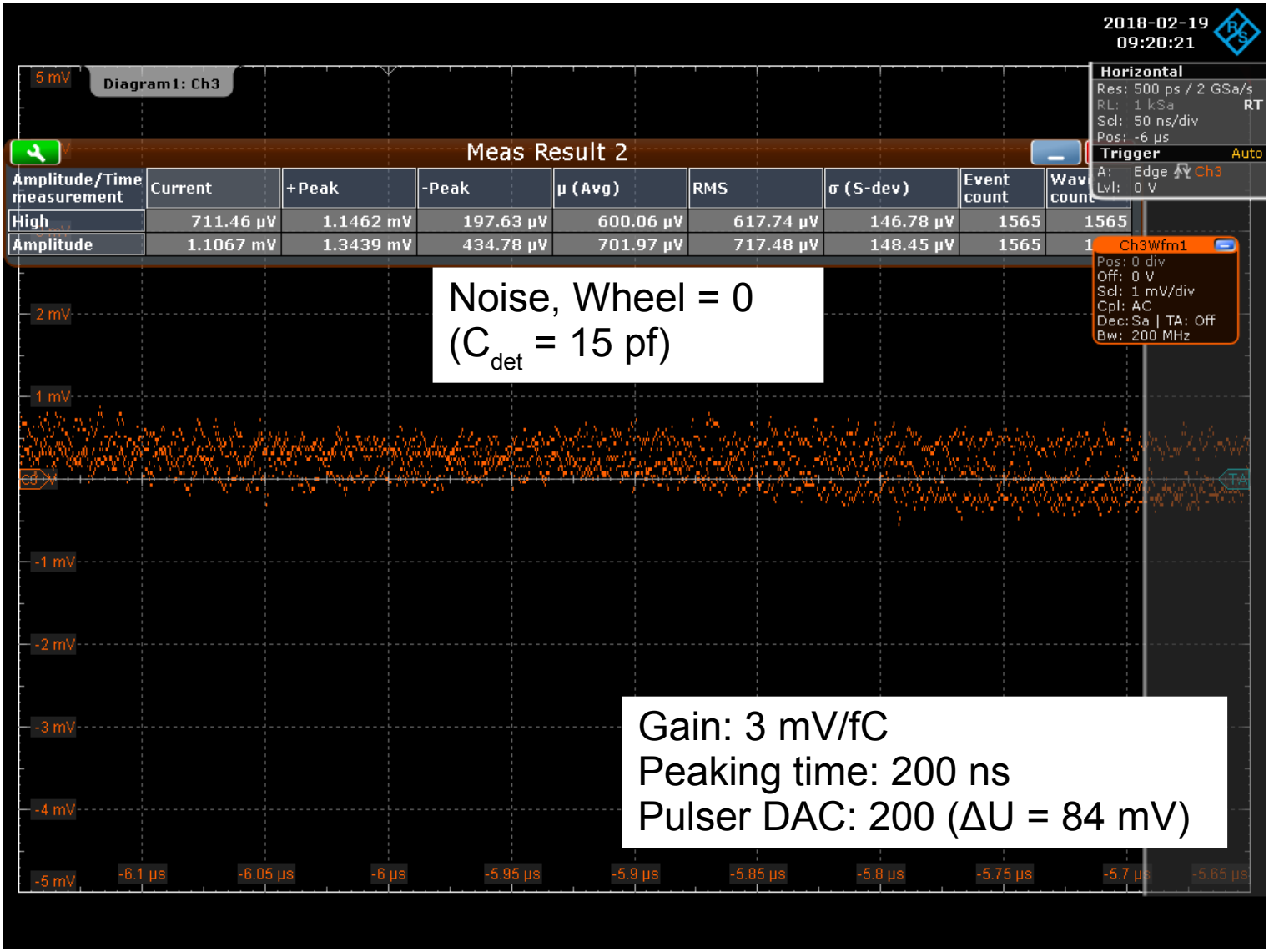


VMM3 noise test



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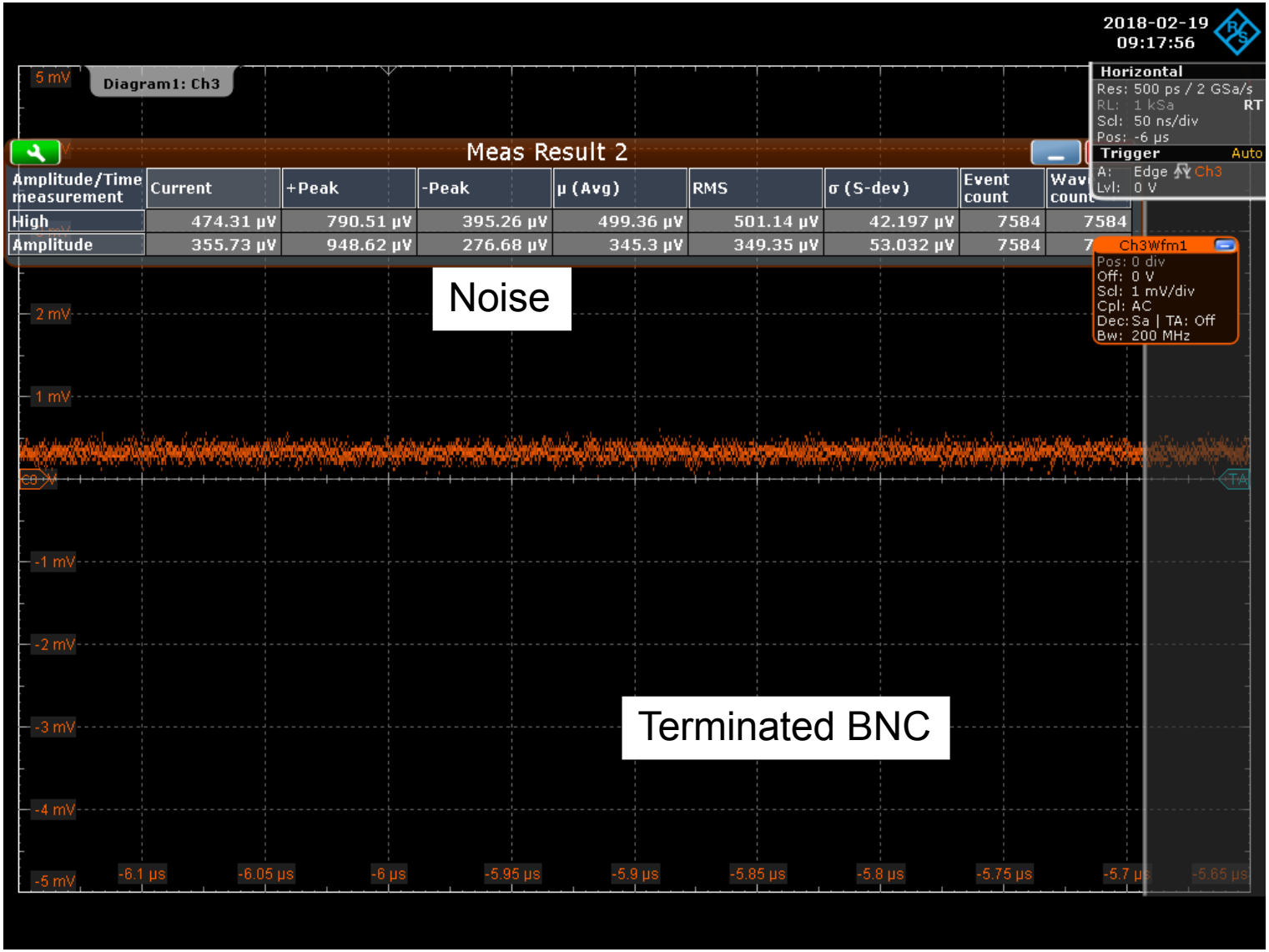


VMM3 noise test

Systematic effects:

Oscilloscope noise → quadratic subtraction

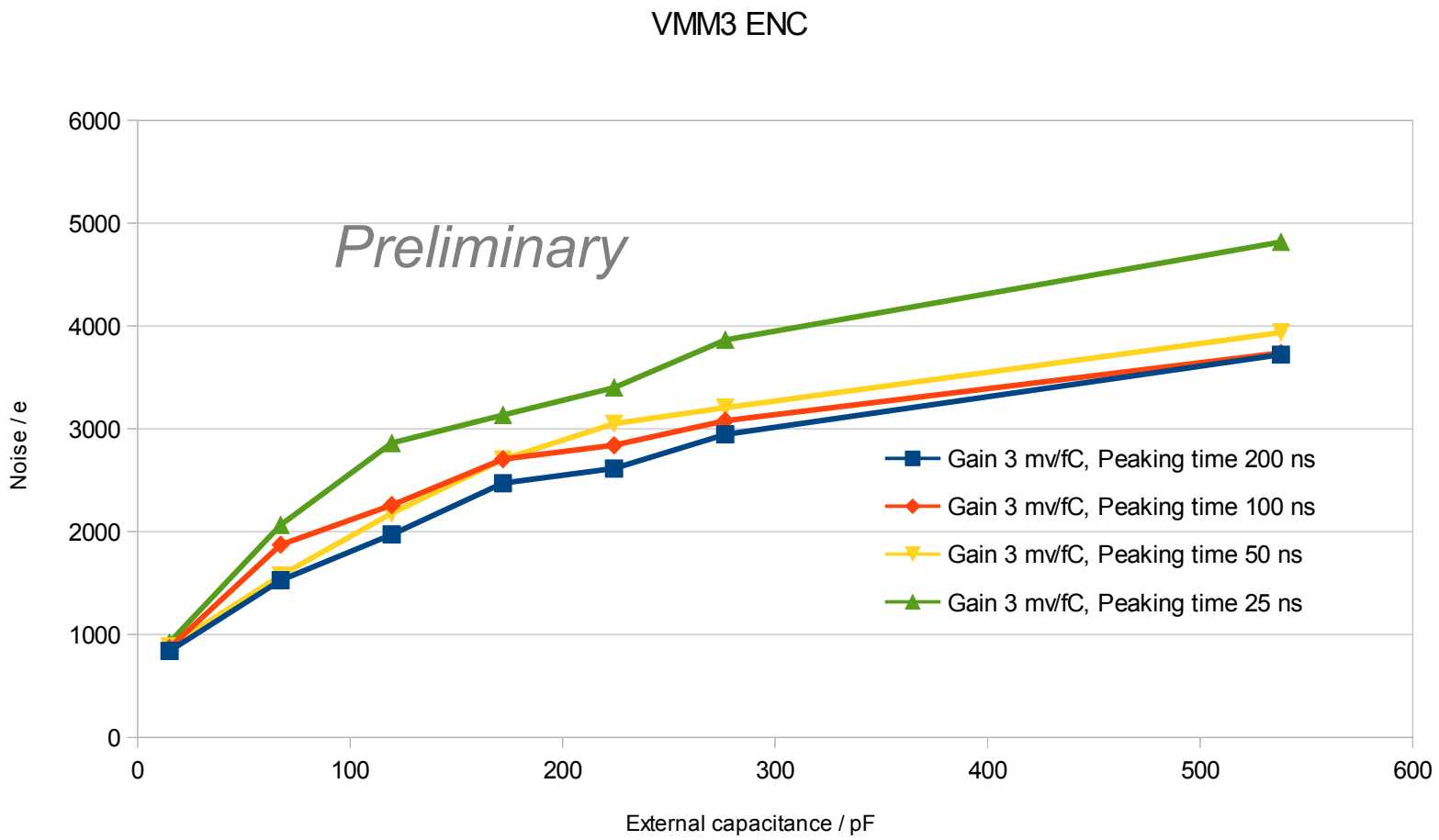
External noise → shielding box, grounding, go out of lab

Still: External noise can not be excluded completely

⇒ VMM noise could be smaller then measured

Internal noise → disable test pulser, readout while measuring

VMM3 noise test – Preliminary results



Statistical error: ≈ 300 e

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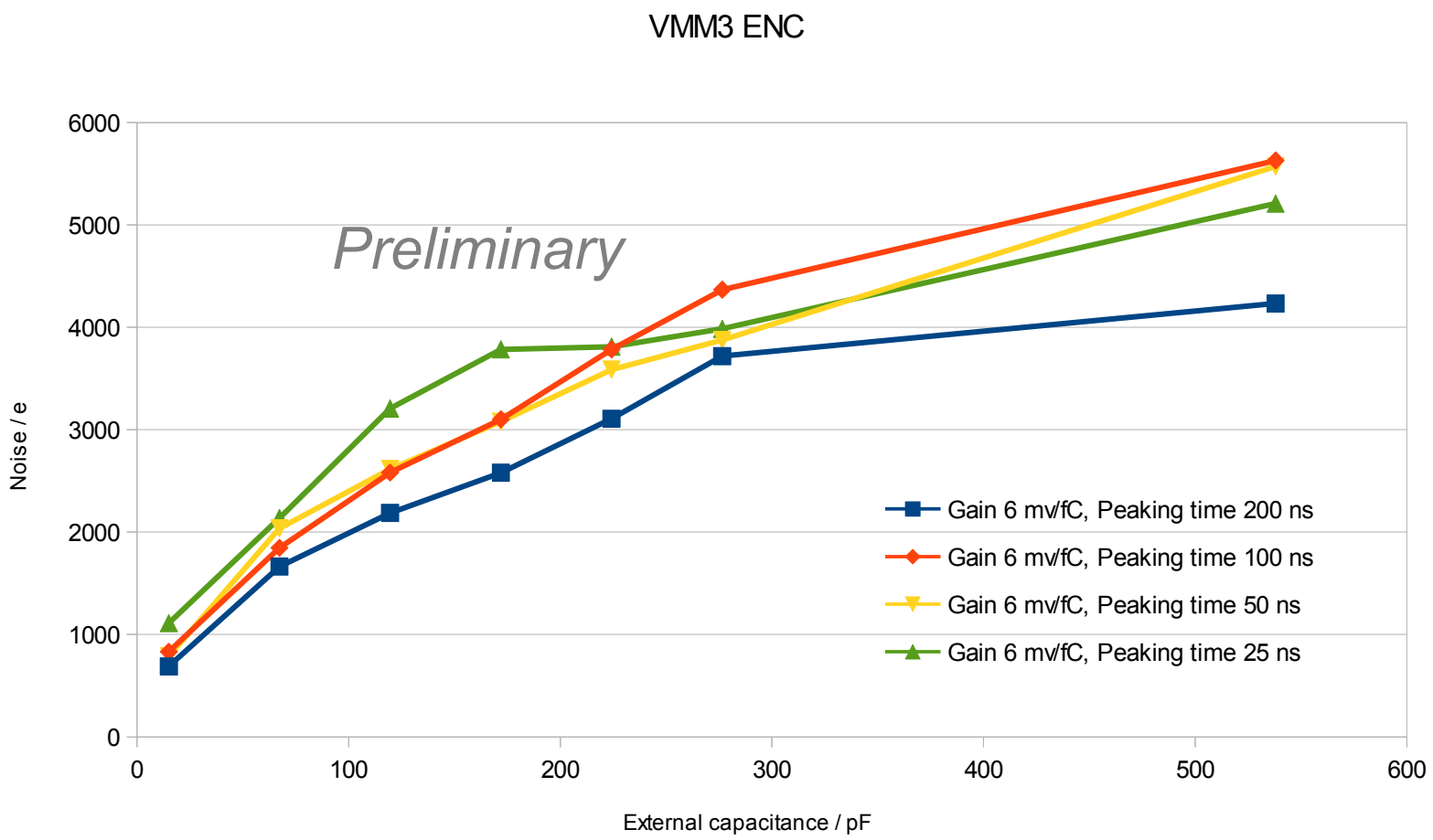

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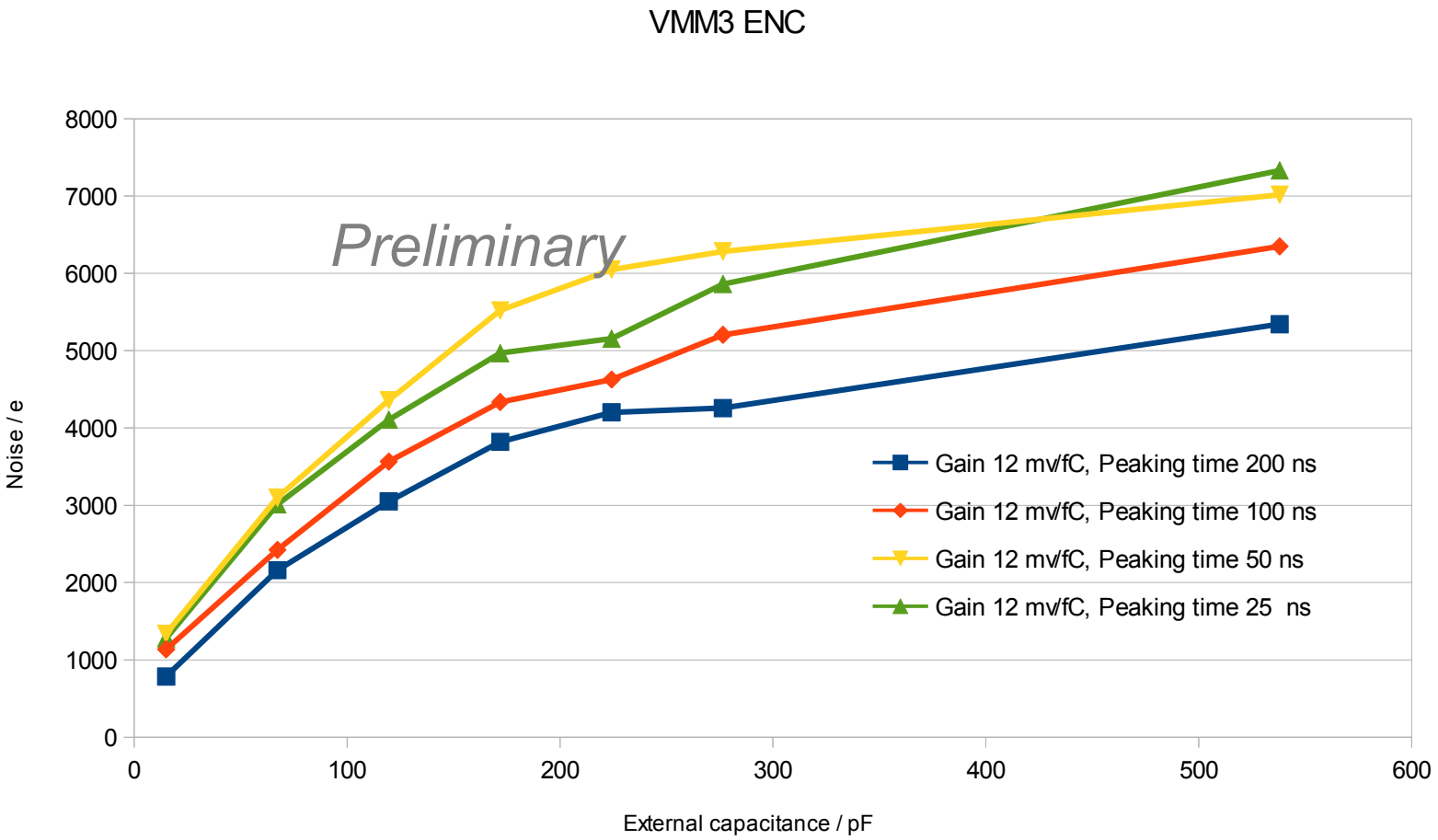

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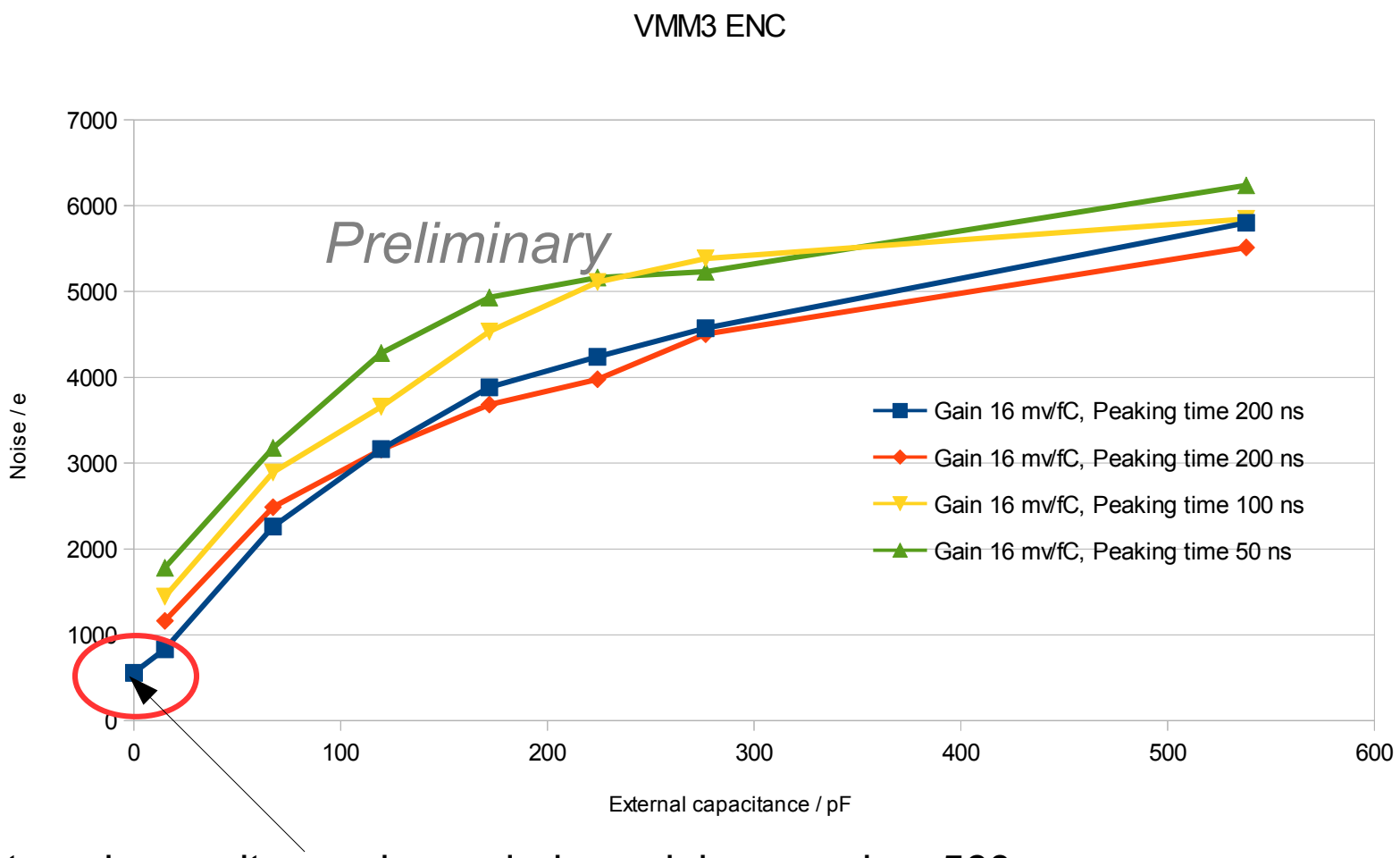

External capacitance decoupled → minimum noise: 560 e

Statistical error: ≈ 300 e

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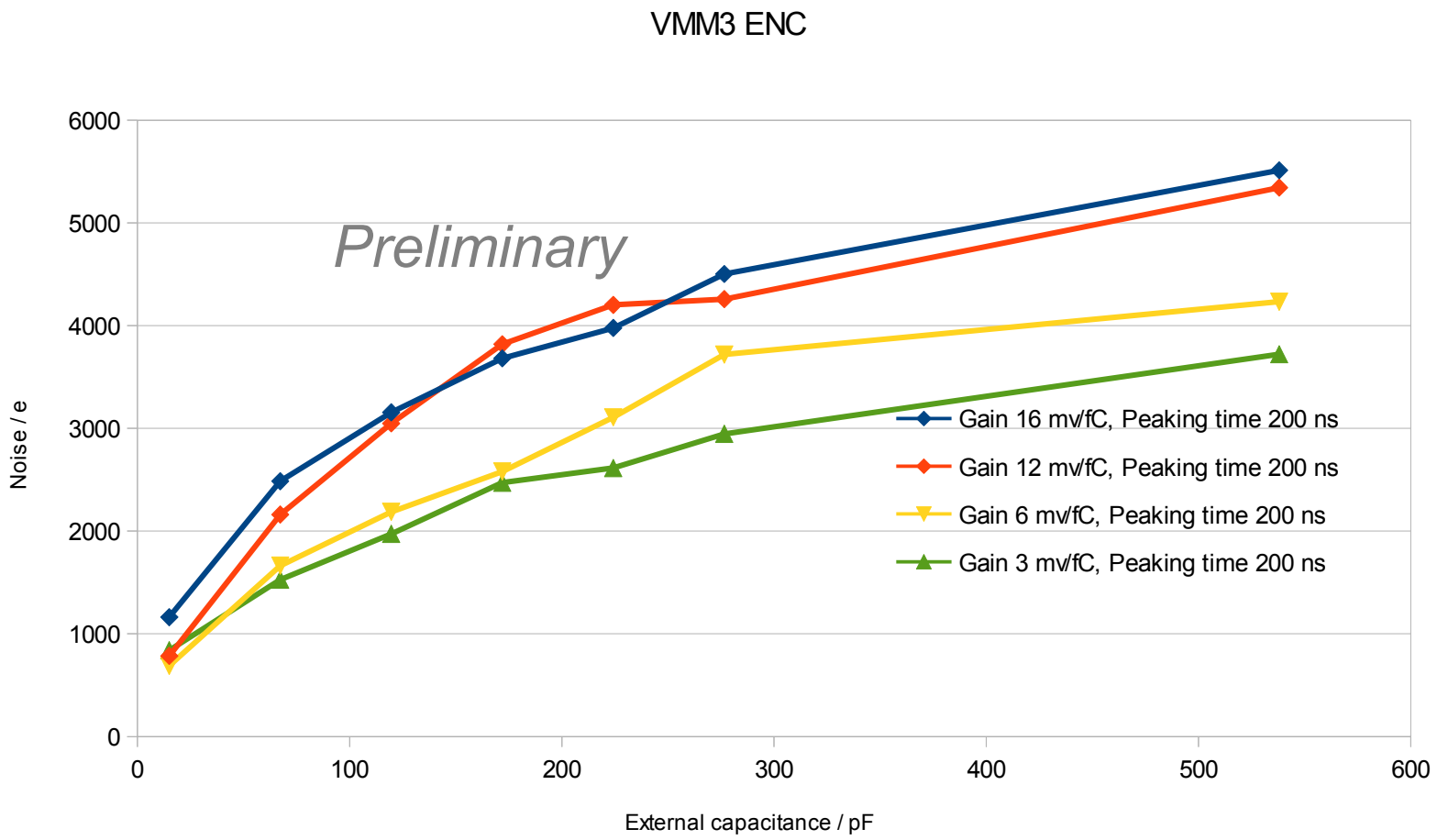

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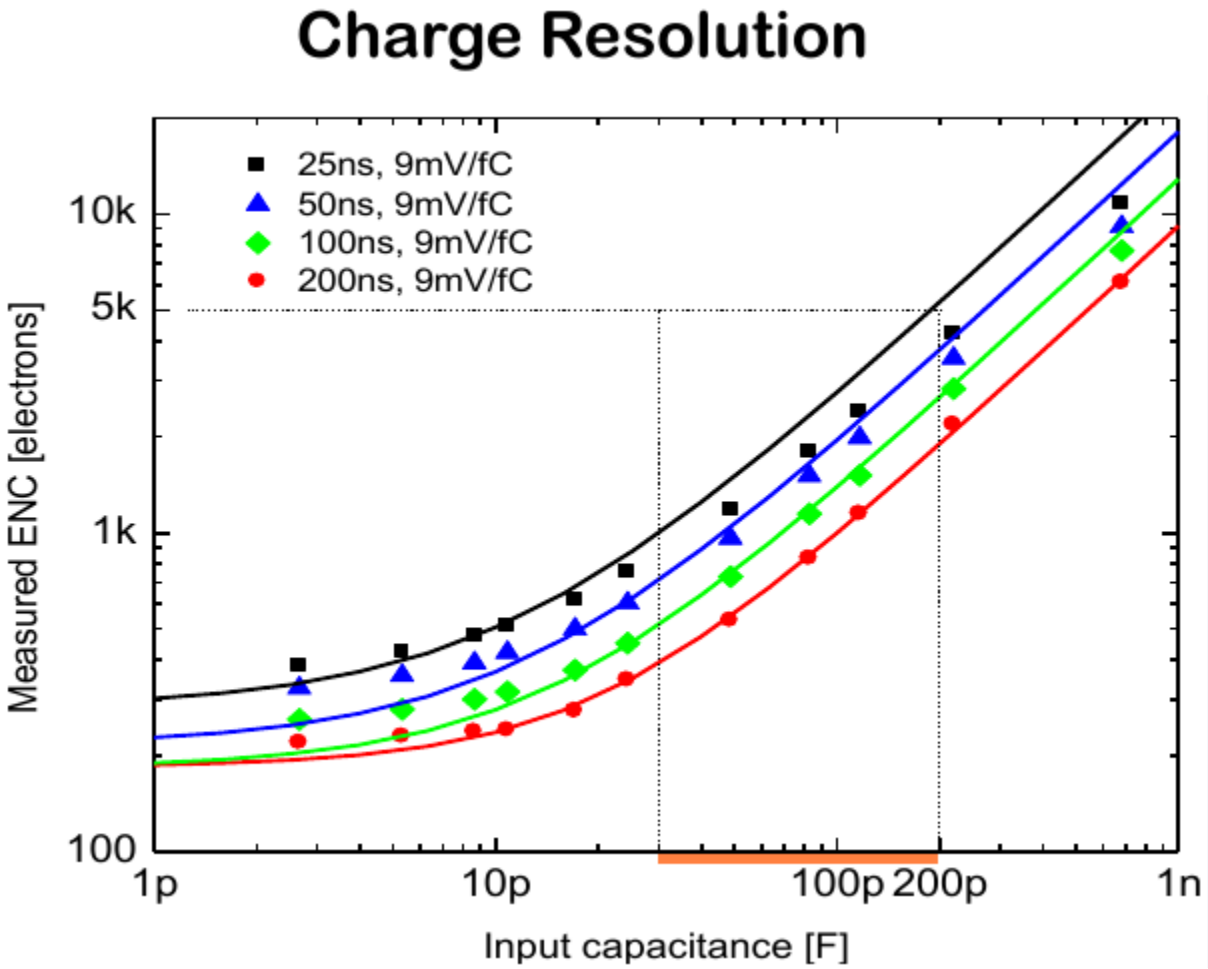

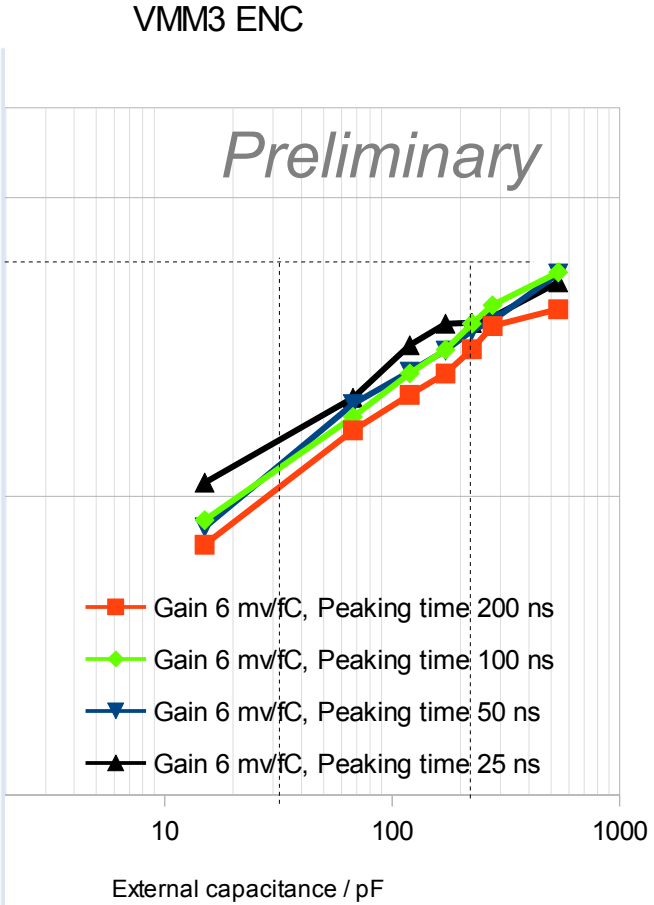

From George Iakovidis, poster at MPGD2017

Statistical error: ≈ 300 e

How you can support the SRS+VMM development

Send a student! (master/PhD, should stay at least for two months)

Good experience so far:

- Freddy Fuentes (Universidad Antonio Nariño, Bogotá) → **will come again for 1.5 months** ==
- Lara Bartels (University of Göttingen, CERN summer student)
- Manuel Guth (University of Freiburg, CERN summer student)
- Lucian Scharenberg (University of Bonn)
- Yan Huang (Central China Normal University)

Win-win-win situation:

You: Student brings back experience with operating the SRS + VMM setup

We+You: Student advances the project

Student: Stay at CERN

How you can support the SRS+VMM development

Send a student! (master/PhD, should stay at least for two months)

Proposed projects:

1. Advance slow control: implement automated calibration → **CERN summer student?**

→ preferably stay of 6 months, should know C++, Qt, also work in the lab for testing

2. Implement useful triggered readout in firmware → **currently ongoing by myself**

→ at least 2 months with knowledge of FPGA programming (> 3 month only basic knowledge)

3. Improve readout speed from VMM to Spartan-6 FPGA → **will be done by Freddy**

→ at least 2 months with knowledge of FPGA programming (> 3 month only basic knowledge)

4. Understanding the VMM readout and documentation for users

→ no prior knowledge required

5. VMM hybrid characterisation for user references

→ some experience with working in the lab, using instruments

Outlook for the next months

SRS + VMM project is advancing very well - but still so much to do

- VMM3a test samples will arrive end of this month
- Hybrid PCBs are currently produces
- DVM Card final review ongoing
- VMM3a wafer production will start soon (3-5 wafers for us)
- SRS + VMM test system for first groups to be delivered
- Three SRS test beams
- Two neutron test beams for completing BrightnESS