Trackella
Tracking on a hybrid architecture: Parallella

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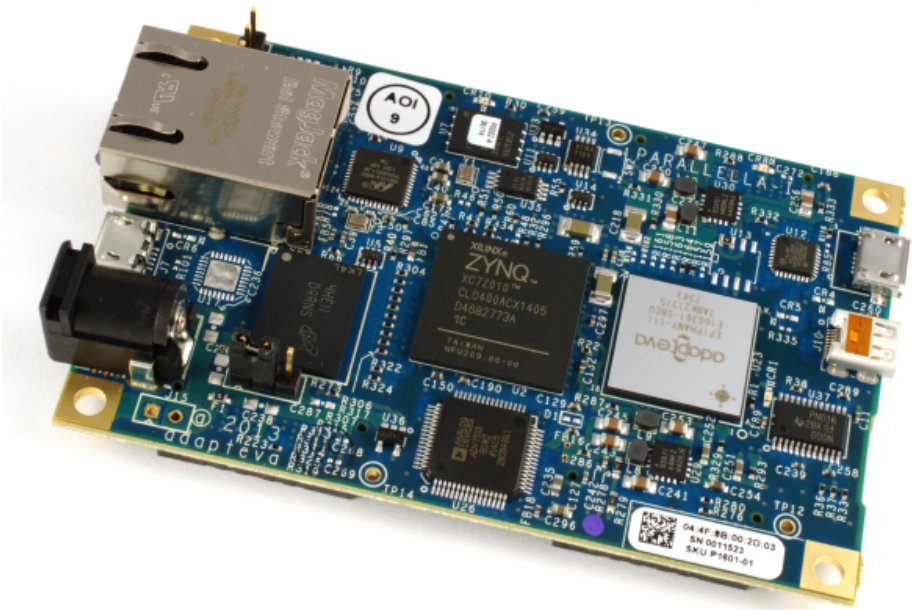
The Parallella board[1]



- Dual core ARM Cortex A9+NEON @667MHz
- 16-core Epiphany RISC SOC @600MHz (C/C++/OpenCL)
- Zynq 7020 SOC (FPGA + ARM A9) FPGA 50% available
- 1GB SDRAM
- Runs Linux

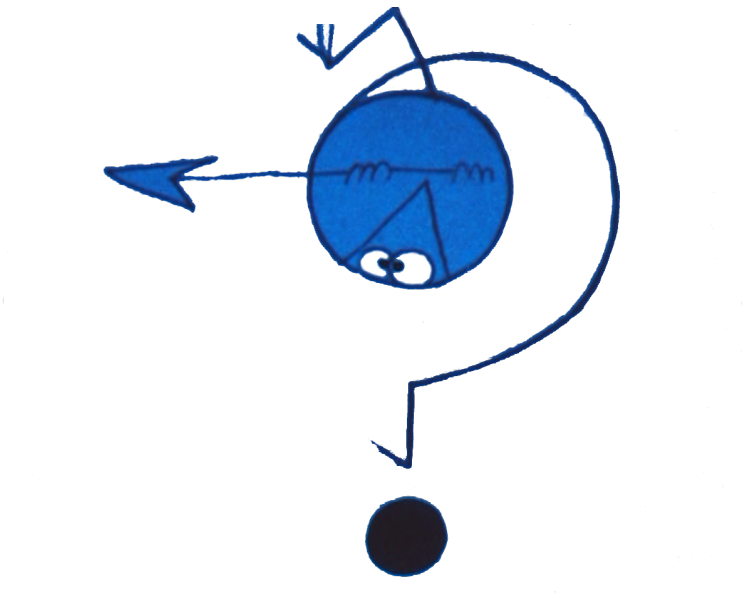
[1] from https://www.parallella.org/

What we target...

- CPU implementation of doublet maker
- FPGA implementation of doublet maker
- Epiphany coprocessor software implementation
- Compare implementations

What we have already...

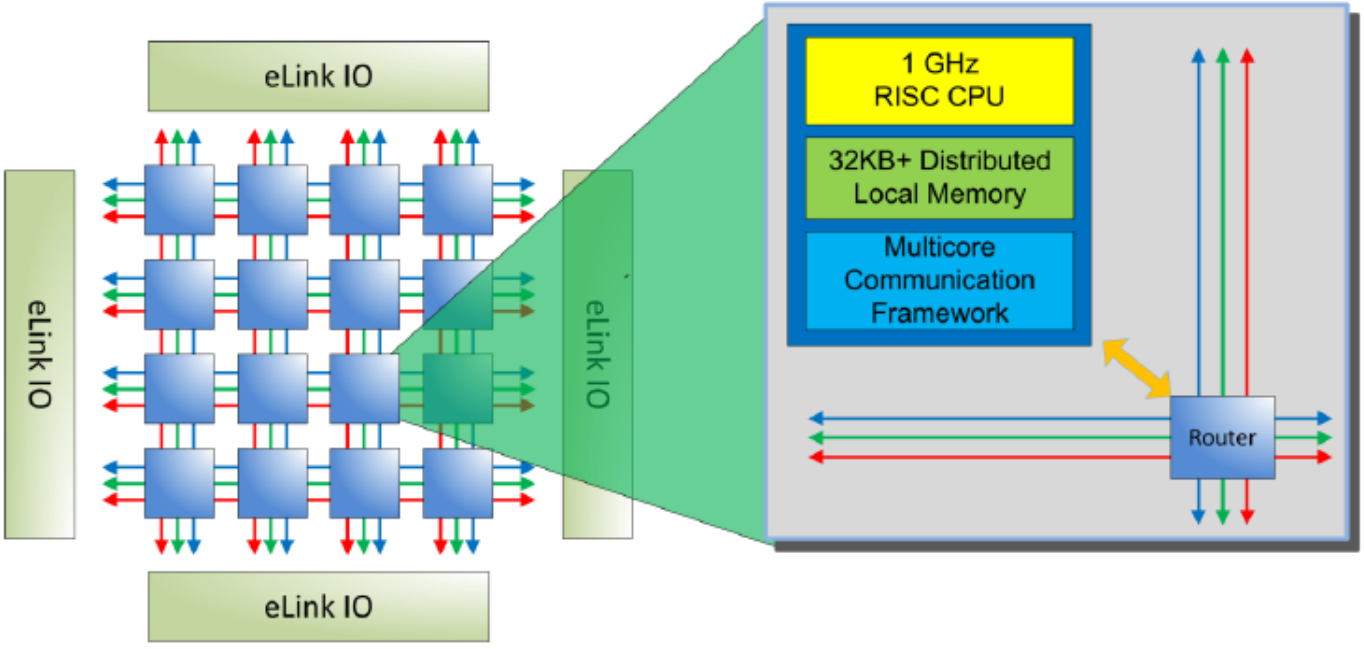
- Software implementation of doublet maker (C++) using real data events of 2017 as input
- Beginning of FPGA implementation ($\sim$20% done)



Parallella, additional features

- Credit card sized computer
- Power consumption: 5W
- 16-core Epiphany RISC SOC (32kB SRAM/core)
- Zynq 7020 SOC (FPGA + ARM A9)
  53k LUT6, 106k FF, 140 BRAM36, 220 DSP48
- Gigabit Ethernet
- 1GB SDRAM
- Micro-SD storage
- Up to 48 GPIO pins
- HDMI, USB (optional)
- Open source design files
- Runs Linux

Epiphany coprocessor 1/2[2]



[2] http://www.adapteva.com/docs/e16g301_datasheet.pdf

Epiphany coprocessor 2/2

- 16 high performance RISC CPU cores
- C/C++ and OpenCL programmable
- 32-bit IEEE floating point support
- 512KB on-chip distributed shared memory
- 32 independent DMA channels
- Up to 1GHz operating frequency
- 32 GFLOPS peak performance
- 512 GB/s local memory bandwidth
- 64 GB/s Network-On-Chip bisection bandwidth
- 8 GB/s off-chip bandwidth
- 1.5ns network per-hop latency
- $<$2 Watt maximum chip power consumption

Abstract

Parallella is a “credit-card sized” computer built on a low-power, high performance Zynq based hybrid architecture consisting of a dual-core ARM CPU with a NEON vectorization engine, a 16-cores Epiphany coprocessor and an FPGA. In this project CMS tracking algorithms will be implemented on the Parallella. The possible implementations of each part of track building in suitable parts of the platform are presented in the sketch. Because of limited time, we will not be able to explore every combination. We will use existing reconstructed real-data events and focus on implementing the seed finding engine on FPGA and investigate the trajectory finder and implementations of it on the on-board CPU and possibly on the Epiphany coprocessor. The “trackella” team consists of 5 people from IIHE/ULB-VUB from Brussels with very diverse areas of expertise, covering FPGA design and SoC implementation, programming, tracking algorithms, as well as various physics analyses.

Abstract (possible architecture)