FPGA Acceleration of Kalman Filter

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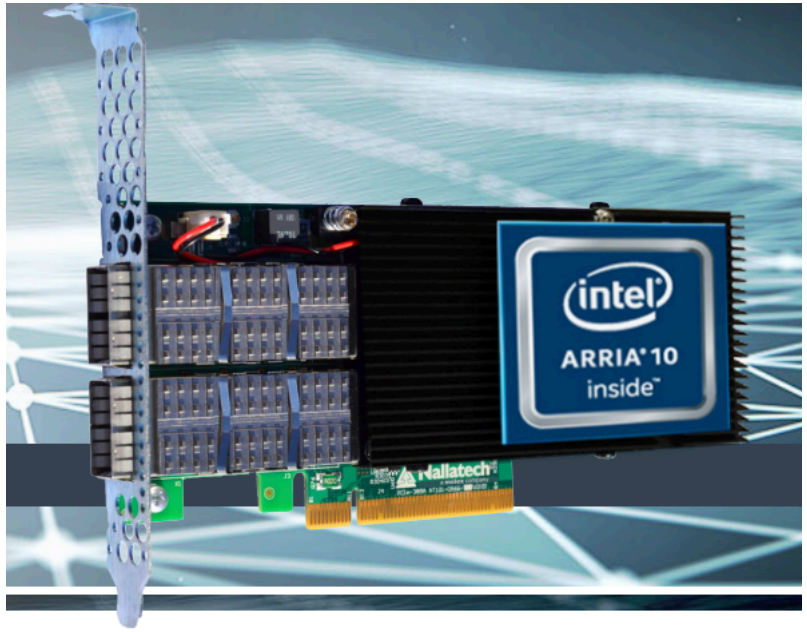
Goals

- Interfacing an implementation of a CMS HLT algorithm into CMSWW
- Kick-off to future work on FPGA-based acceleration for CMS HLT algorithm

Hardware



- Start working with FPGAs on Intel Arria 10

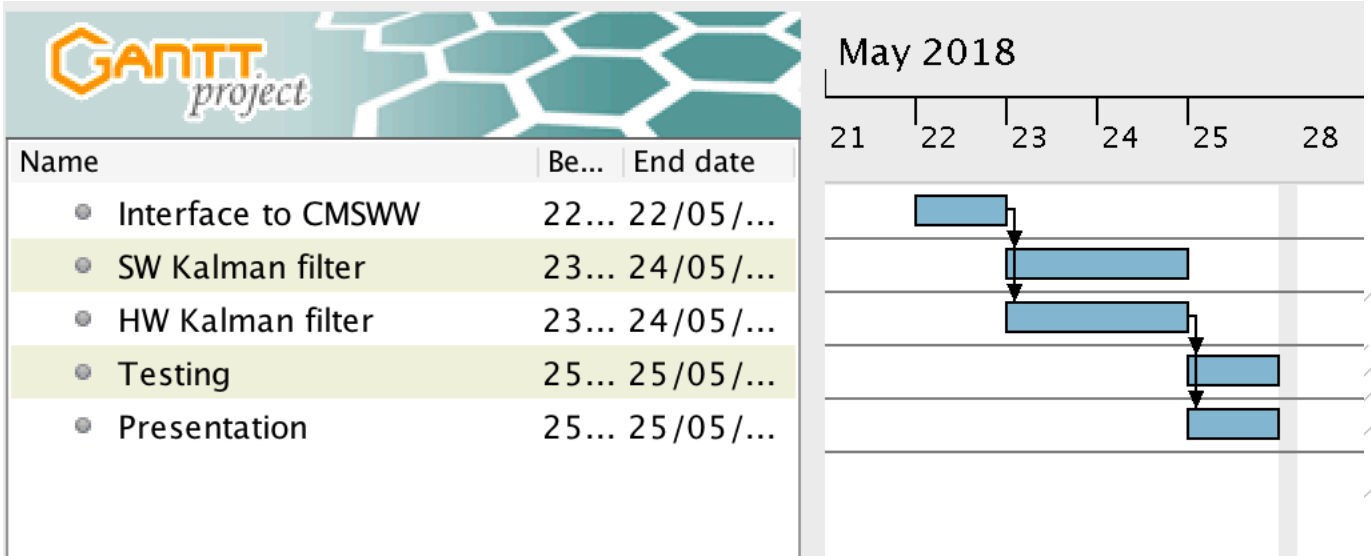
385A – with Arria 10 / 1150 FPGA

Highlights

- **Featuring Arria 10 FPGA Up to 1.5 TFLOPS of processing power**
- **Two high bandwidth banks of DDR3 SDRAM memory**
- **8-lane PCIe Gen 3.0 card**
- **Two 10 & 40GbE Network Ports**

Tasks

- Interfacing to CMSWW
- SW Part
- HW Part (OpenCL + VHDL)



Possible Algorithms

- Kalman Filter
- Real-Time Matrix Cross Product Engine
- …