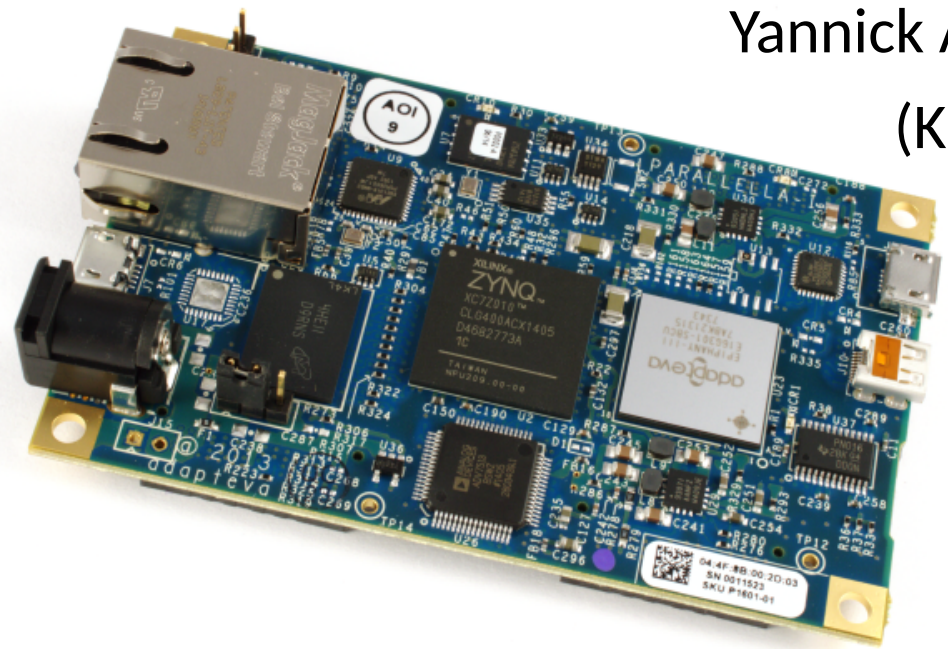
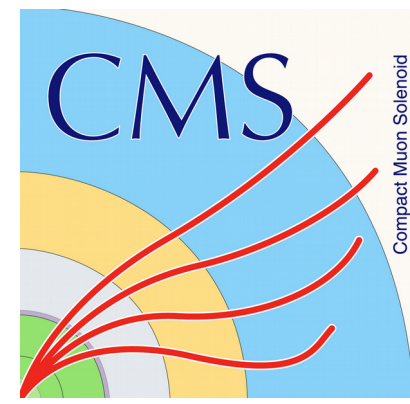


Trackella status

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Done...

- On hardware side:
 - Sorting hits in φ
 - Implemented in vhdl
 - Seems to work on simulation
 - Problem with synthesis: memory “simplified” by synthesis tool
- On CPU side:
 - Sending data to one core of the coprocessor
 - Reading a “done” flag from shared memory

To do...

- Measure speed of hit memory loading
 - in simulation
- Implement hardware sorting
 - Done in sim; trying to understand the problem with synthesis
 - Repeat the same in z
- Run the finding algorithm on one core on the coprocessor
- Then distribute it among cores