# Trackella conclusions & plans

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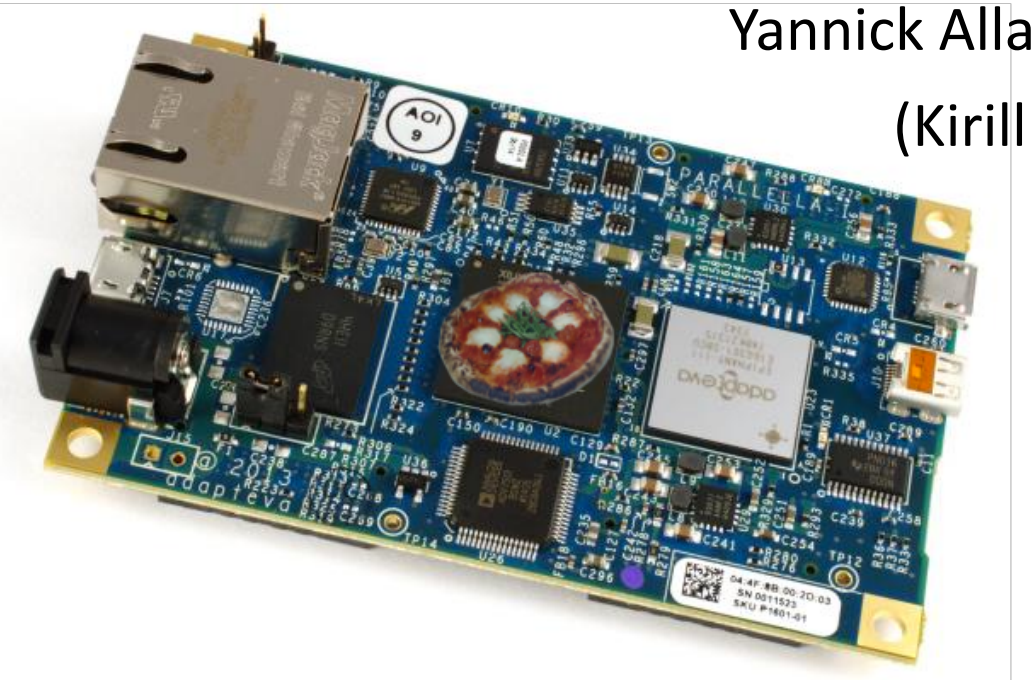

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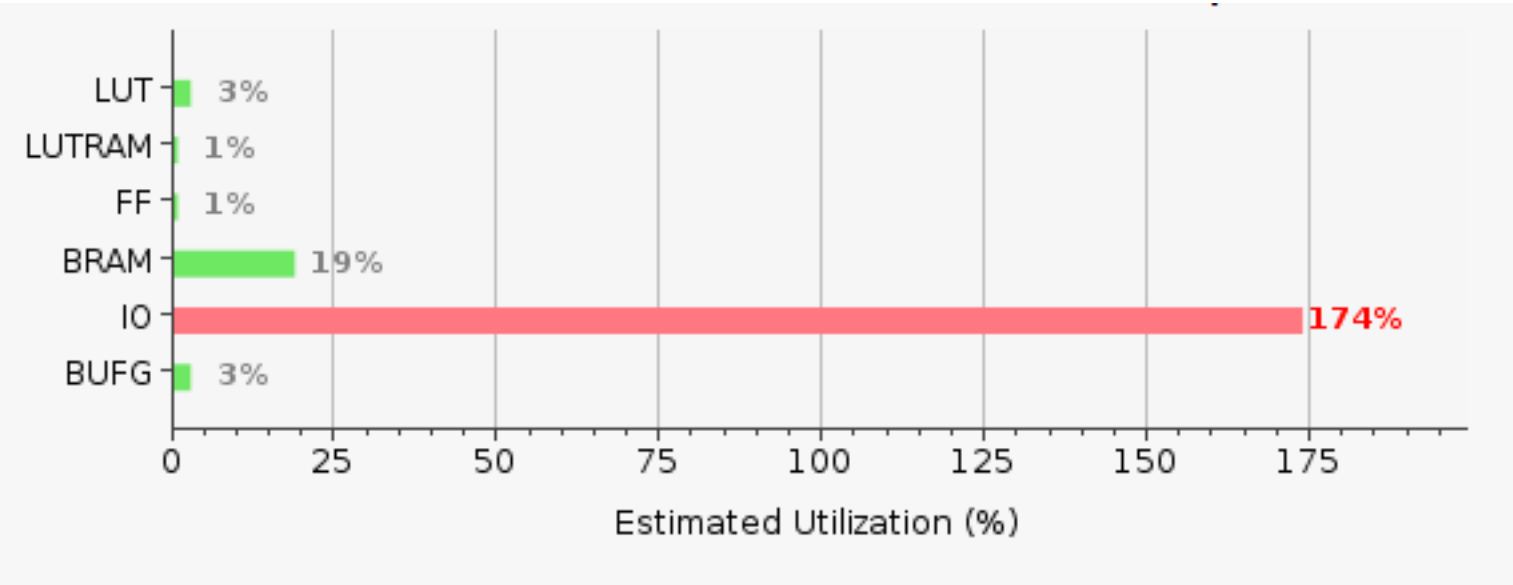
# Done during this hackathon…

- On HW side:
  - Doublet finding with simplified cuts!
    - Average doublet verification: ~3 clk (30M checks / s)
- Ran on same event on SW and HW
  - Simple dz and dϕ cuts on both sides
  - Nhits in this event: L1= 1225 L2=1022
  - 761 doublets on SW – 652 on HW
  - Matched them one by one
    - 113 extra on SW, 4 on HW

# Done during this hackathon…

- On HW side:
  - The size of the design…
  - Given:
    - 4k hits for layer1 and layer2 => 64kB memory
    - 8k doublet memory => 32kB
    - ϕ: 64 bins of 128hits => 16kB

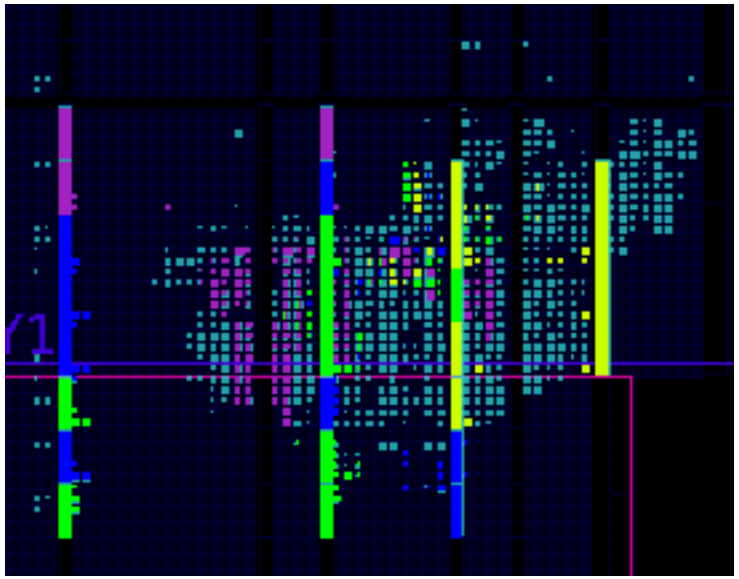


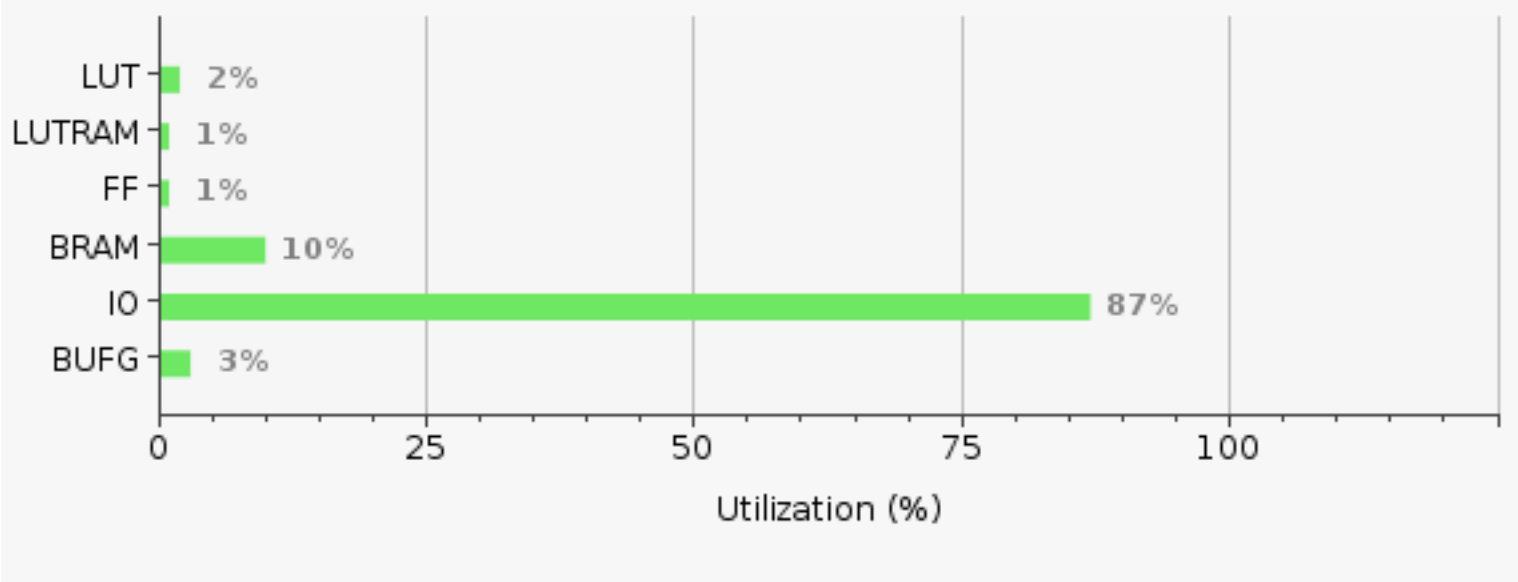

Total LUTs: 1840
Total FFs: 1506
total BRAMs: 27
Synthesis time: 2:09 min

IO is not fitting because AXI slave not linked to AXI ZYNQ master

# Done during this hackathon…

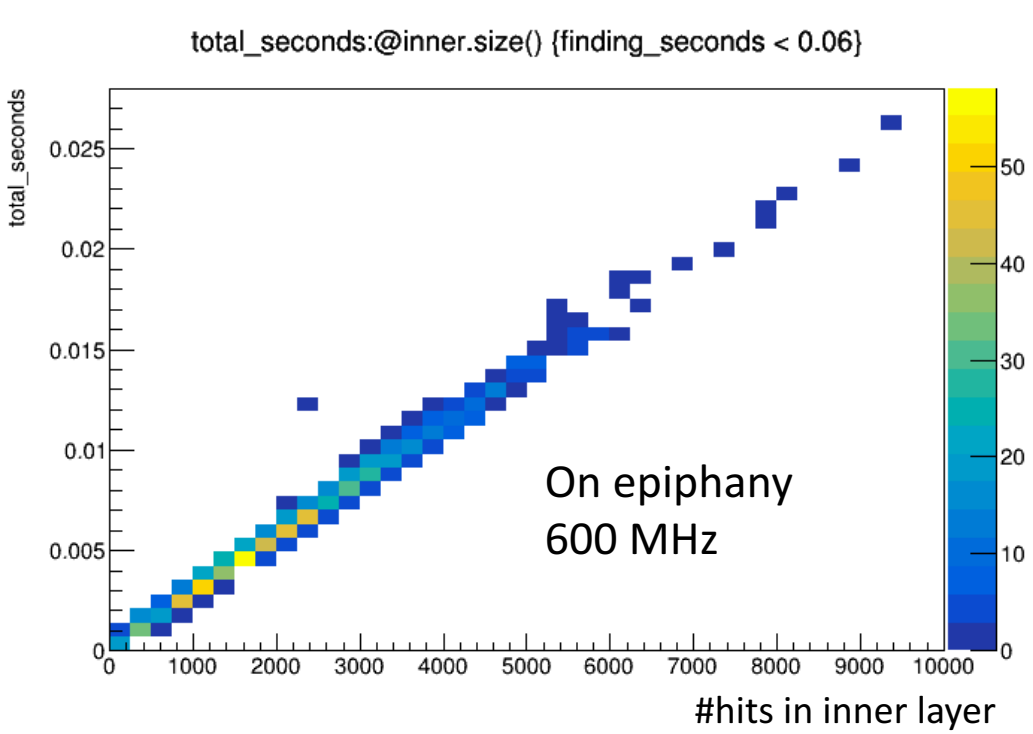
On ZYNQ xc7z030fbg676-1
~50 % more logic
Double IO

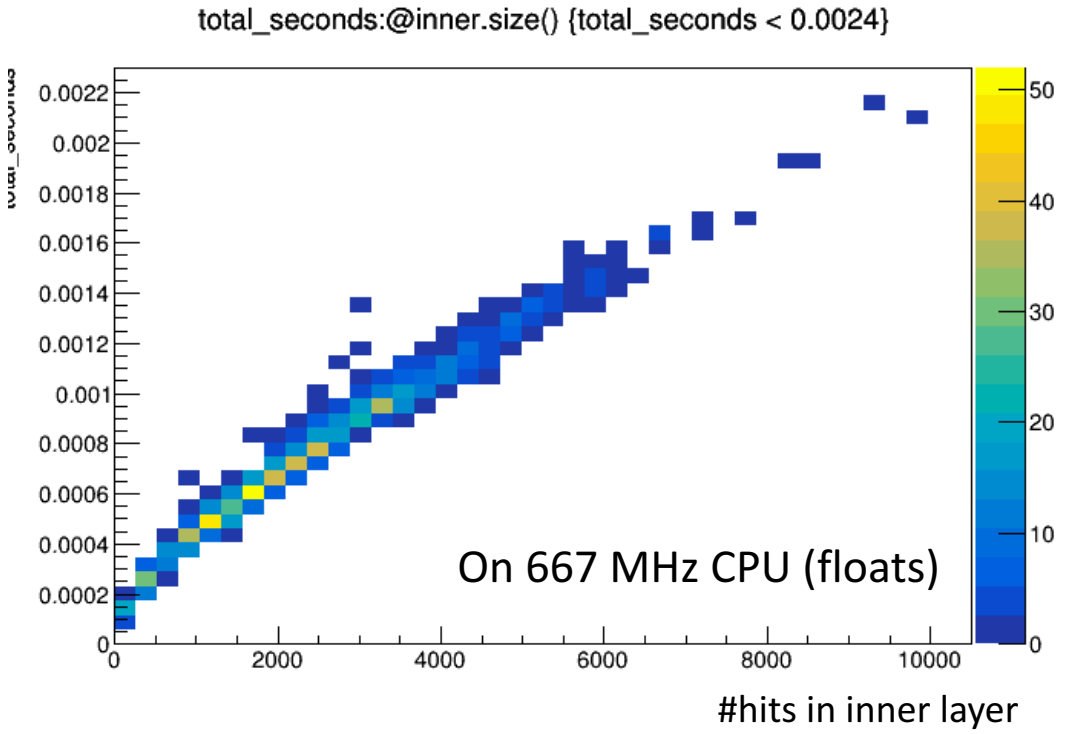




# Done during this hackathon…

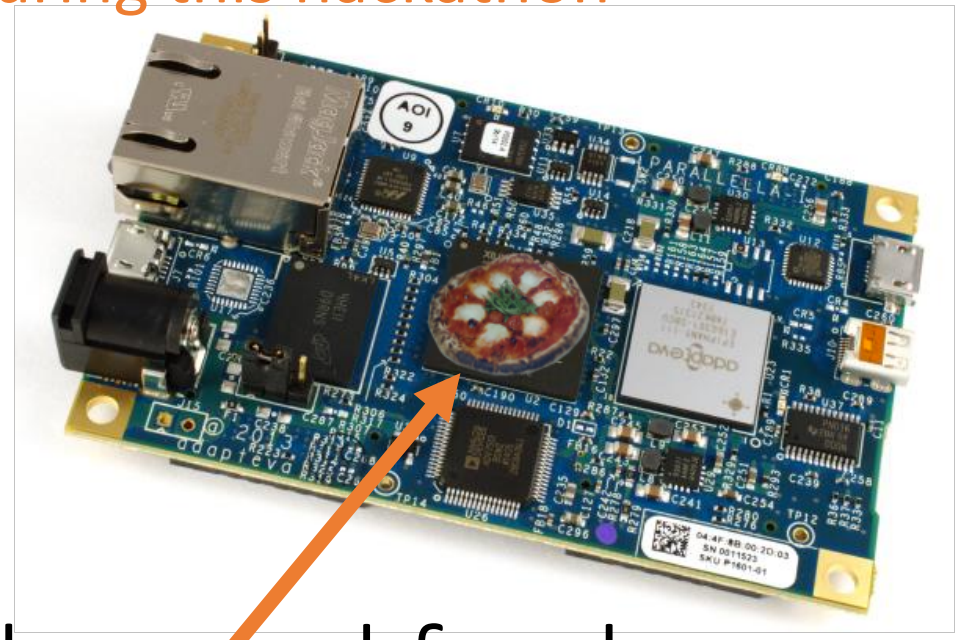
- On SW side:
  - Three implementations of doublet finding:
    - Same algorithm (also for FPGA) running on
      - CPU (floating point and fixed point)
      - and partially on epiphany



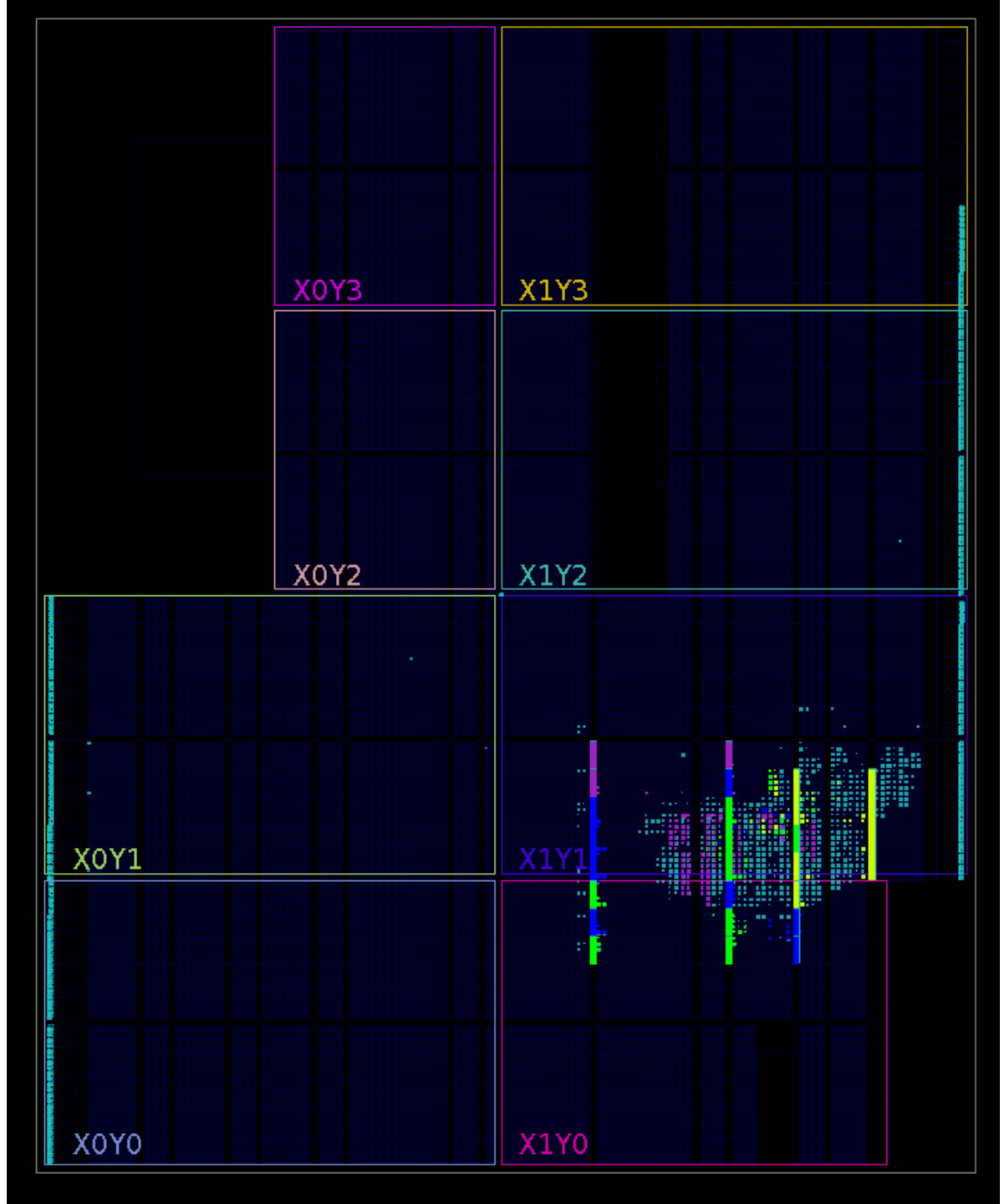
# Conclusions & future ideas

- Managed to achieve benchmarks aimed during this hackathon
- Future thoughts:
  - Test in HW, not only cycle-accurate SIM
  - triplet, quadruplet …
  - Implement KF
  - Can always discuss new ideas ☺



Thanks for the organization, the good food and the best social dinner ever

# Backup


X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0