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The Front-End board of the upgraded LHCb Calorimeter

Joao De Abreu Barbosa Coelho, Yasmine Amhis, Christophe Beigbeder, Olivier Duarte, Yiming Li, Vitalii Lisovskii, Frédéric Machefert, Monique Taurigna, Vincent Truong-Canh

Laboratoire de l'Accélérateur Linéaire, Orsay, France

Abstract

This note describes the ECAL/HCAL Front-End board. The signal treatment for pedestal subtraction and gain correction is explained. The scheme used to produce the trigger information, and to send the data throught the optical links is also detailed. The results of some of the tests are given and show the present performances of the board.

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1 Overview

1.1 Connections with the detector

The calorimeter electronics [1, 3] is based on 246 front-end boards (FEB), 2×96 and 2×27 for the ECAL and HCAL respectively [7]. The factor 2 illustrates the symmetry between the A and C sides of the detector. This number includes FEB needed for the measurement of the pin-diode signals (4 pin-diode FEB for each sub-detector). Both ECAL and HCAL use identical FEB. Each board handles 32 channels, and is connected to 32 photomultiplier (PMT) outputs. In the outer region of the ECAL, a module (whose section is of approximately 12×12 cm^2) contains a single channel, while in the rest of the detector a module embeds several channels. The region of the calorimeter which is covered by a FEB is a rectangle of 4×8 cells.

Each FEB provides:

- the data to the computer farm in the form of 32 transverse energy (E_{T}) measurements,
- the Low Level Trigger (LLT) information which is based on the ADC data of the board and on data received from other boards, either plugged in the same or other crates.

The digital electronics is based on a 12 bit Analog to Digital Converter. Hence, the E_{T} is coded in the data readout with 12 bits for each of the 32 channels of a board.

The LLT is based on 4 values evaluated on each board:

1. the maximum transverse energy measured from the clusters built from 2×2 cells,
2. the address of the cluster giving the largest transverse energy as measured in the previous calculation,
3. the total energy from the contributions of the 32 channels handled by the FEB,
4. the number of cells on the region covered by the FEB for which the measured transverse energy is larger than a threshold[1].

As a FEB treats 32 channels, the ADC data requested bandwidth is $12 \times 32 = 384$ bits (12 bits per channel and 32 channels) at 40 MHz. The LLT bandwidth is 32 bits at 40 MHz (see section 3).

Several solutions exist to send the data, but the most efficient and the scheme the most adapted to the 8 channel blocks of the FEB consists in using 4 fibres per board (one fibre per block of 8 channels), in the widebus mode of the GBT and so that each fibre transports 112 bits.

[1]The threshold is loaded in the FEB by slow control during configuration.

1.2 Crates

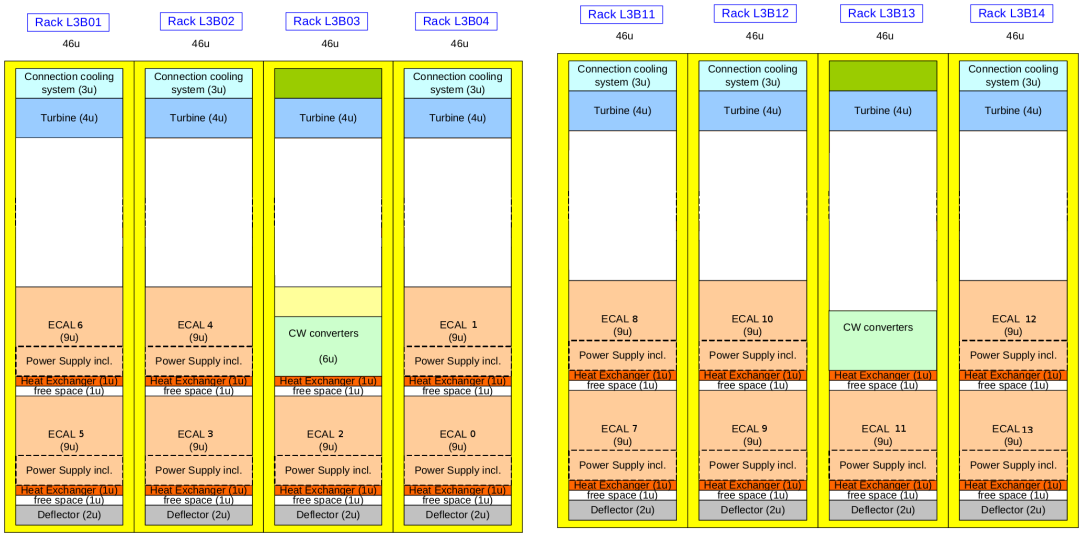

Figure 1: The ECAL crates as they should be organized on the gantry (ECAL calorimeter).

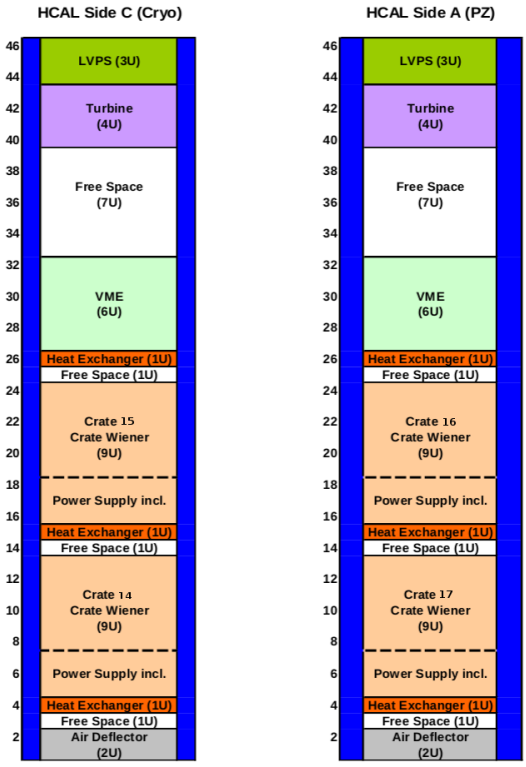

Figure 2: The HCAL crates located above the HCAL on the gantry (HCAL platform).

The location of the front-end electronics is unchanged for the upgrade. The 18 necessary 9U crates will be gathered in racks located on the calorimeter gantries, 14 on the ECAL platform and 4 on the HCAL one. The clock, fast and slow control for the front-end electronics will be ensured by 18 control boards (called 3CU, see 3CU internal note) plugged in the central slot of the crates. The 3CU boards are powered directly by the backplane of the crate as for the FEB and are connected to the counting room with bi-directional optical links.

The overall organisation of the ECAL and HCAL front-end electronics (mainly the crates) on the gantry is identical to the present situation [10]. The SPD/PS equipments will be removed during the long shutdown. Figure 1 and 2 show the foreseen location of the crates in the racks both for side A and C of the ECAL and HCAL.

1.3 Board overall organisation

Picture 3 shows the first prototype of the Front-end board. Another previous version was used as a test board for the analog electronics and a feasibility study. This version treats 32 channels and is already based on the final components. It is supposed to be as close as possible to the final version.

As shown on Figures 4 and 5, one can identify 6 major components in the board:

1. the front-end block (4 identical blocks) contains the analog electronics, two dual-ADC, two FPGA (called Front-end FPGA in the following) and a GBT-X component and produces E_{T} measurements for the data stream and calibrated E_{T} for the LLT paths,
2. the trigger/sequencer FPGA (TrigSeq FPGA) which is used to perform the LLT calculations but also provides some bits to the optical links (BX-id, etc...),
3. the GBT-SCA that is in charge of the slow control on the board,
4. the block of (de-)serialiser for the exchange of the LLT data among different boards in the same or different crates (neighbours),
5. the block containing the DC-DC converters and the protection delatchers,
6. the light emitters that receive the data from the four GBT-X and send them to the counting room.

The architecture is based on:

- 8 ICECAL chips,
- 8 FPGA of type M2GL025-1FG484, in the 4 front-end modules
- 1 FPGA of type M2GL150-1FC1152, for the LLT and event building processing
- 4 GBT-X driving 4 VTTx emitters produced by CERN

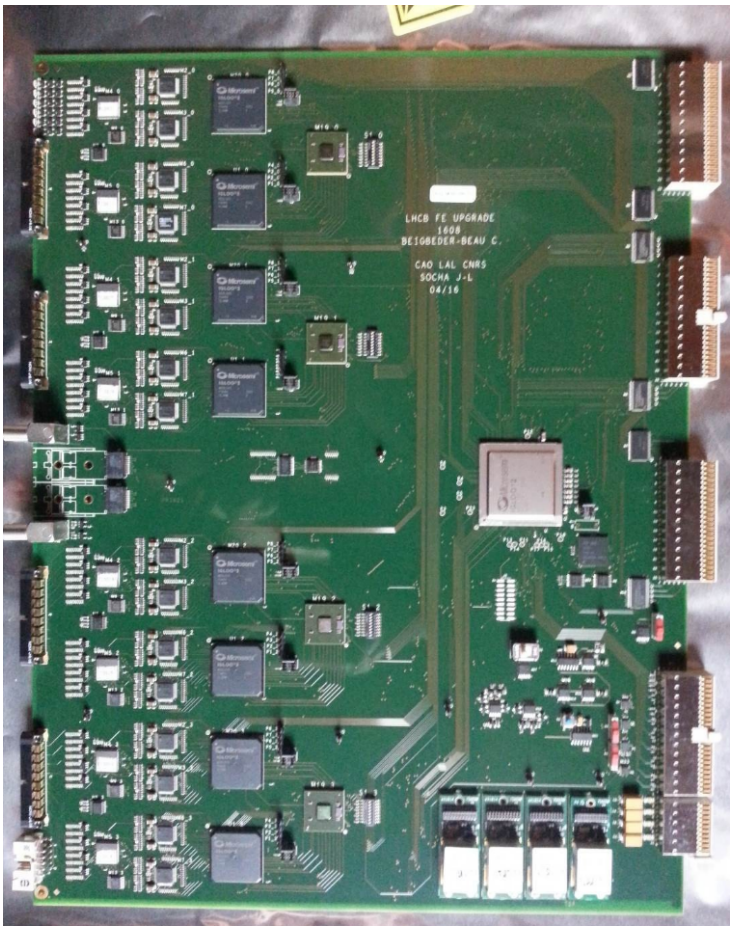

Figure 3: Picture of the first prototype of the Front-end board.

- A single GBT-SCA component for the slow control and receiving its e-port lines from the backplane and the 3CU board.
- DC-DC converters designed by CERN and MAX 869 (2A) components for the power line protections.

All register storing configuration and permanent information are protected with a triple voting technique (TVR).

2 Front-End module

2.1 Analog part

The signal of the PMT is clipped on the base in order to produce a pulse which is mainly contained in a 25 ns window. Then, the signal propagates in a ≈ 12 m coax cable and is

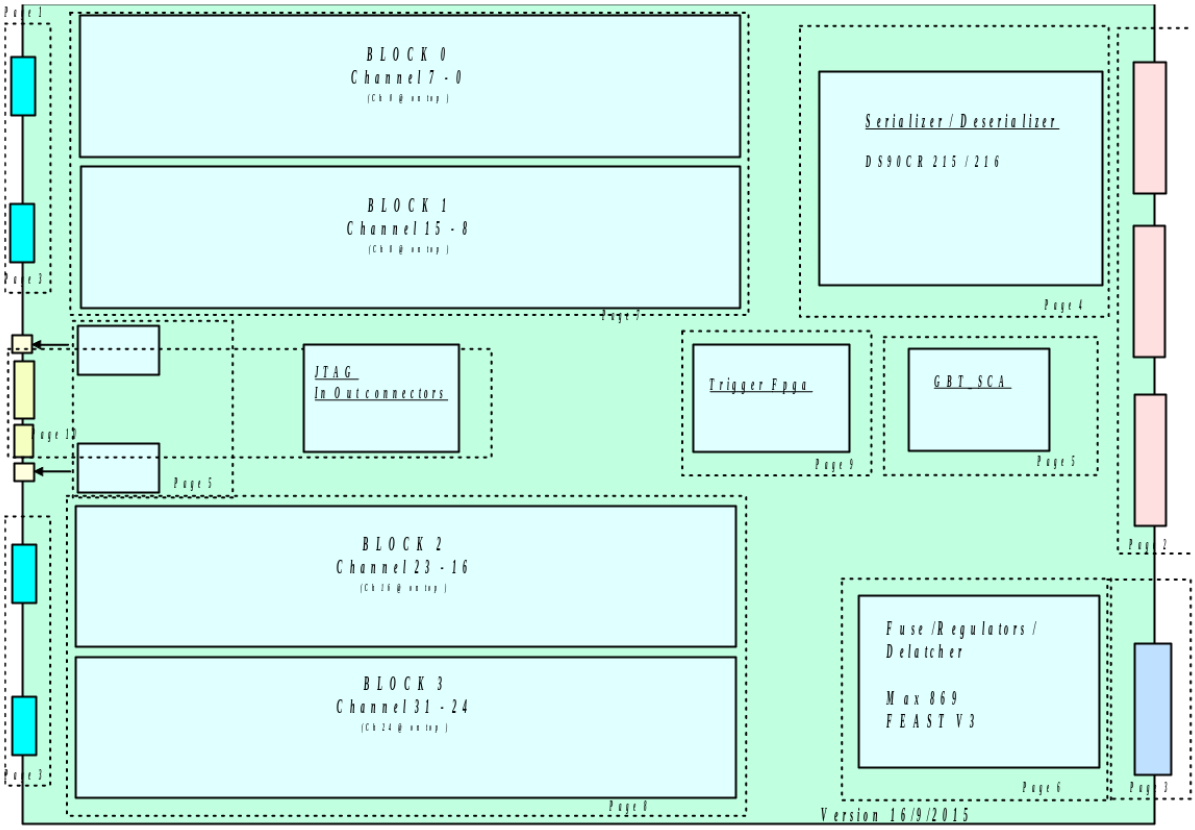

Figure 4: Topology of the Front-End board.

injected on the positive input polarity of the ICECAL chip (see Figure 6). In a first stage, the input signal is amplified with a current amplifier. Then, the ICECAL contains two interleaved processing lines running at 20MHz synchronous with the 40MHz global clock. Each processing line

- shapes the signal with a pole zero compensation,
- integrates the signal or is reset,
- stores the integrator signal in a track and hold module.

This processing is followed by a multiplexer presenting at the output the integrated signal. A driver sends the measurement of the input charges to the ADC.

The ICECAL receives its clock from the GBT-X of the front-end module it belongs to. It is configured through the TrigSeq FPGA with the SPI protocole. Among the most important parameters are the pole zero compensation parameters, the gain of the integration processing and the clock phase to be used to integrate fully the PMT signal on

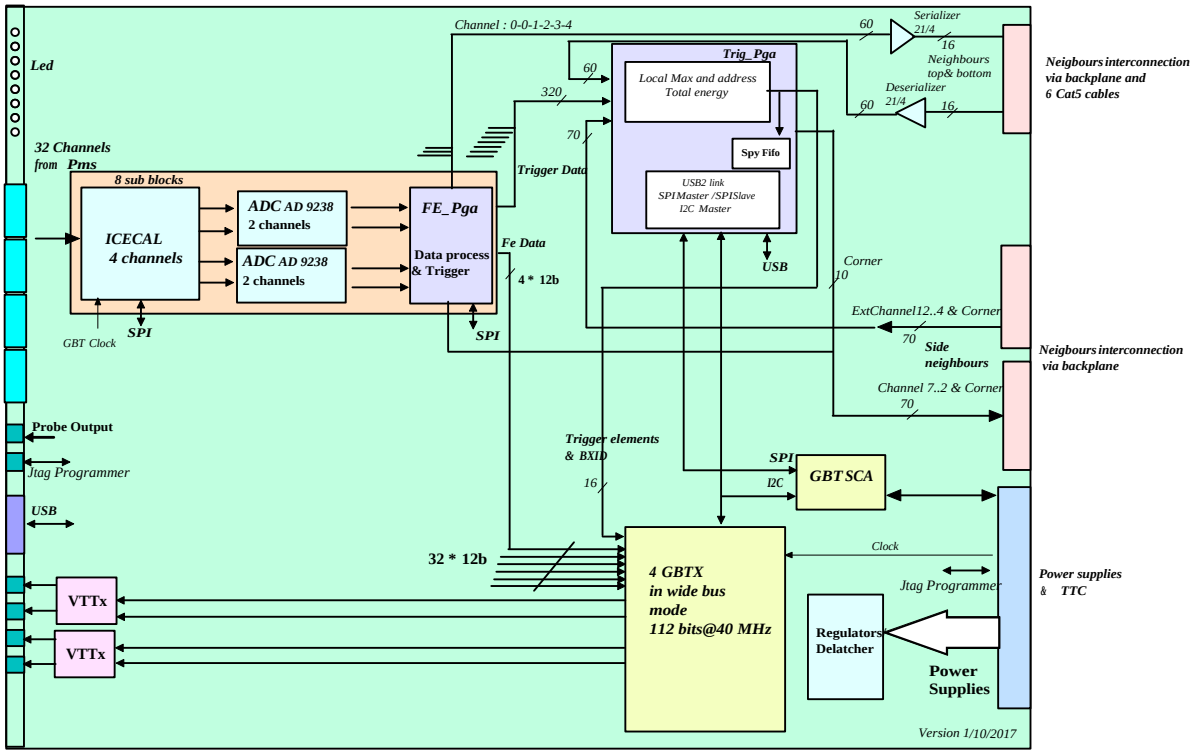

Figure 5: Functional schematics of the FEB descibing the front-end block, the power circuitry, the slow control (GBT-SCA) and trigger modules.

a single integrator in a 25ns window.

The ADC that converts the analog output signal of the ICECAL into a 12 bit digital word is a dual ADC AD9238 component from Analog Device. It requires a clock to properly sample the ICECAL output. The clock phase of each one of the 32 channels of the board can be adjusted independently. The adjustable clocks are produced by the ICECAL and directly injected into the ADC.

The ICECAL treats four channels in parallel and is connected to 2 dual ADC.

2.2 Front-end FPGA processing

The four differential output lines of the ICECAL are sent to 2 dual ADC which produce 4 times 12 bits acquired by a single FPGA. As the output bandwidth of the board requires four optical links, the board contains four GBT-X and the front-end modules of the board are based on one GBT-X, 2 FPGA, 2 ICECAL and 4 ADC. This defines a front-end unit as shown on Figure 7.

The front-end FPGA processing is divided into 3 distinct modules (see Figure 8).

1. The first one processes the input ADC data, which needs to be re-synchronized (each

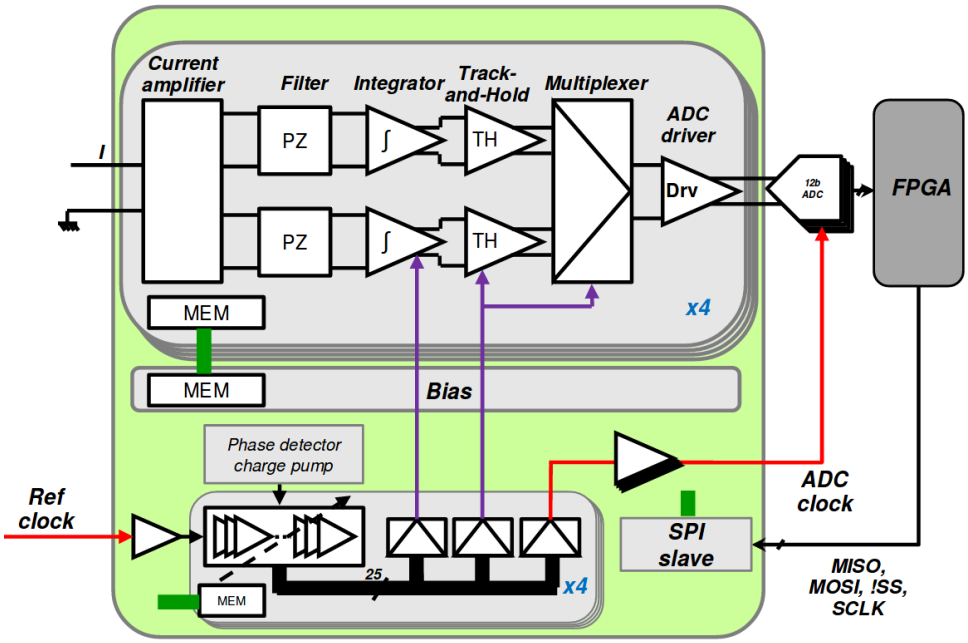

Figure 6: Schematics of the analog electronics.

ADC channel has its own clock) and processed to remove the low frequency noise and to subtract the pedestal. At this level, we could think of compensating for the spill-over by applying some correction factor. This is not foreseen at present and was not used in the current electronics of the calorimeter. The data are then sent to the GBT-X for serialisation.

2. The LLT data is calculated by applying a conversion factor and converting the 12 bits of the ADC to 10 bits. The data are then sent at 80MHz to the TrigSeq FPGA for future processing or to the neighbouring FEB for 2x2 cluster calculations of the FEB border regions of the calorimeter (see Figure 10).

3. A SPI interface is included into the FE FPGA for the configuration and monitoring of the FPGA. Several FIFO are used to

   - inject digital patterns,
   - store digital processing results,
   - store LLT calculation results.

2.2.1 ADC data synchronisation

The ADC data synchronisation is performed in two stages (see Figure 9). A multiplexer(adjustable through ECS) selects the clock polarity to be used to sample the ADC

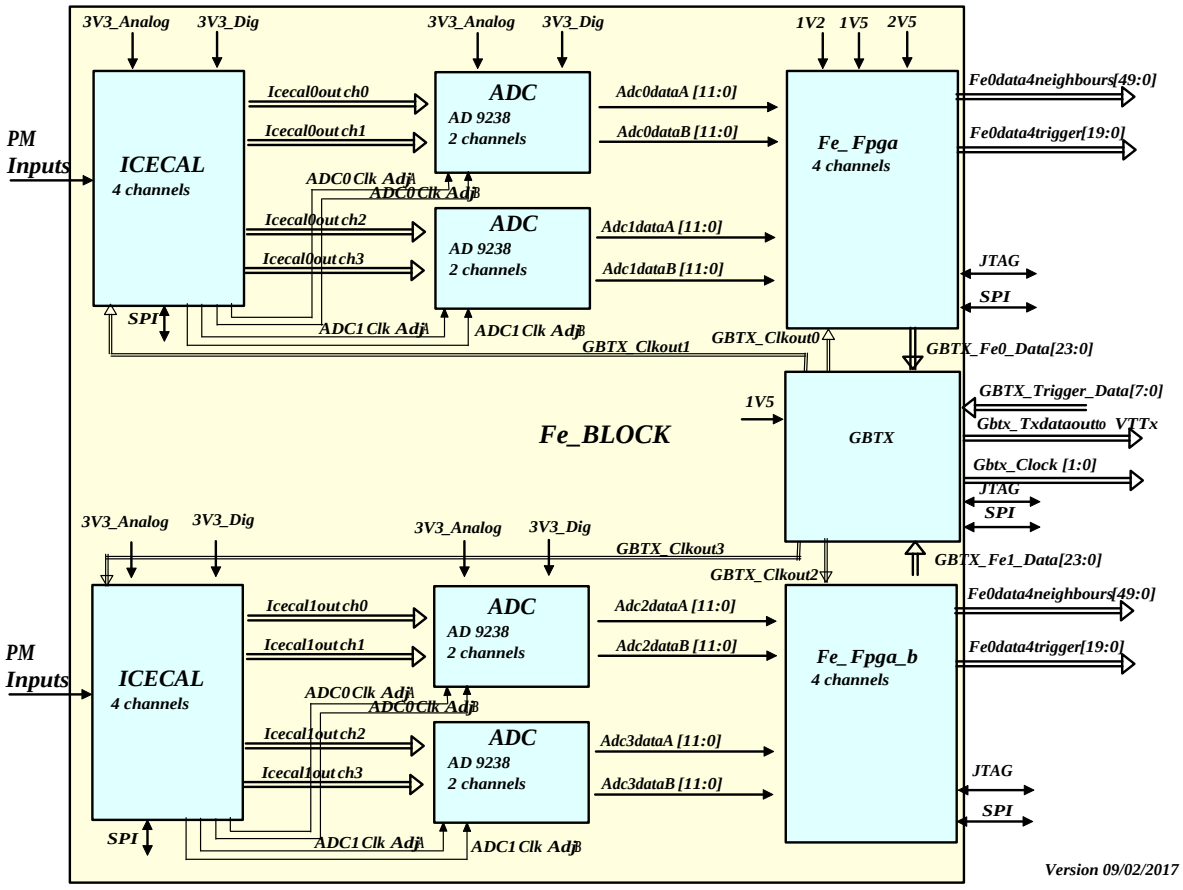

Figure 7: Detailed schematics of a Front-End module of the FEB.

data. The polarity can be adjusted independently for each channel. In a second stage the positive edge clock polarity is used to sample again the data in order to prepare them to be used by the FE FPGA digital calculations.

The phase difference from channel to channel may be such that a single event may be sampled in two different and consecutive bunch crossings at this level. Hence, a tunable latency is introduced after the data synchronisation in order to correct for any bunch crossing id mismatch between channels.

2.2.2 Low frequency noise removal

Then one wants to suppress the low frequency noise. We implemented two options for this suppression.

1. Standard method: one subtracts the smallest of the previous two measurements (according to a single integrator of the ICECAL, hence, the t-2 and t-4 signals). The idea is that a channel has a low occupancy, and then the probability that there was a

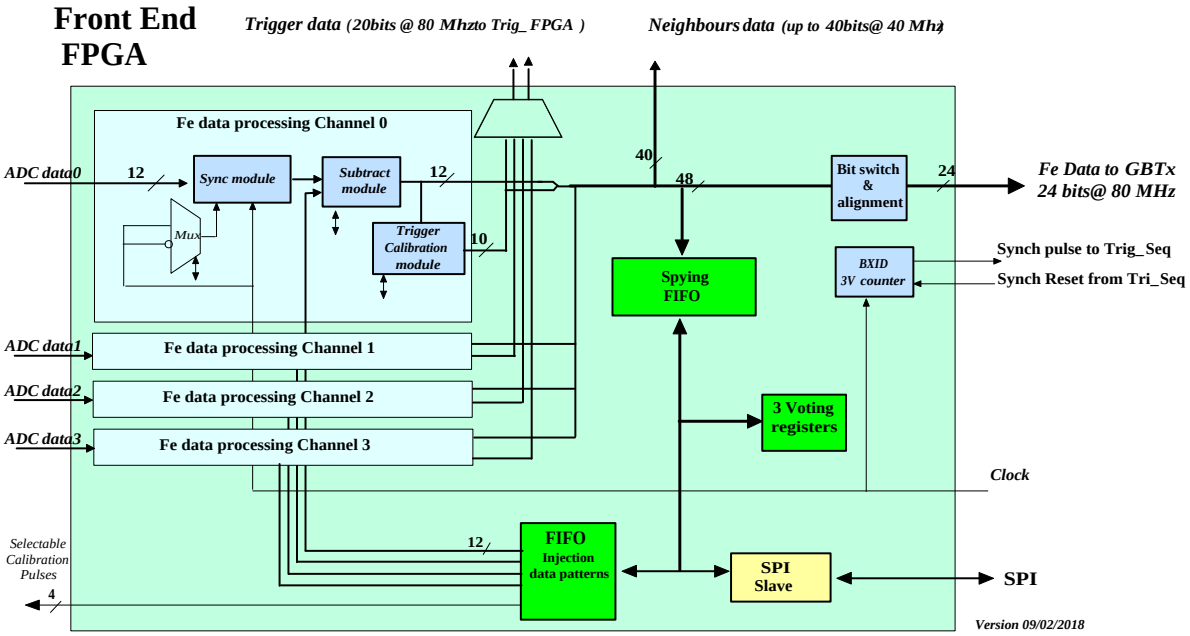

Figure 8: The front-end FPGA processing.

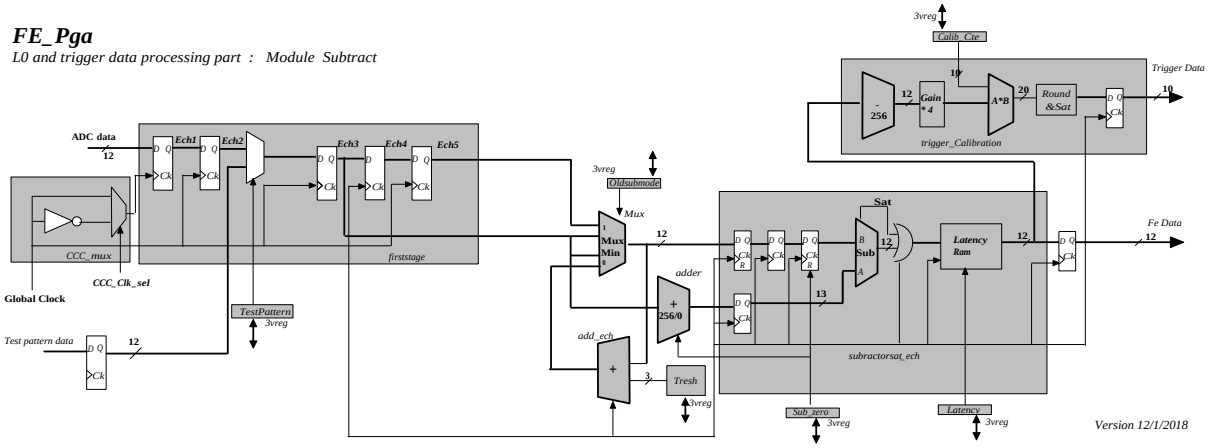

Figure 9: Front-End block of the FEB.

signal in previous crossings t-2 AND t-4 when there is some signal in the current one is negligible. It has been shown that this underestimates the pedestal (one selects the low fluctuations) by 0.42 times the pedestal sigma, which means about half a count (this has been measured on the current electronics).

2. Improved method, to avoid brutal fluctuations: the estimated pedestal is the lowest of the previous pedestal plus a constant, and of the previous measurement (according

to a single integrator of the ICECAL, i.e. t-2). The constant is small, between 1 and 3 counts. Using 2 counts as pedestal step, the shift of the pedestal is less than .1 counts for a nominal sigma of 1.5 counts.

Simulations and measurements show that the second method is better. The measured sigma is lower than with the other method by .2 counts. When adding an exponential signal with a width of 100 counts and a frequency between 1 and 10%, the degradation of the sigma is small, less than 15%, while it starts to be huge for the standard method, as the case of 2 consecutive signals starts to become relevant. However, as the second method may not follow fast enough upwards variation of the pedestal, and more generally depends on a longer history of the signal, we implemented both methods, with a control switch to be able to choose, and a parameter on 2 bits for the second method. Both methods have been used in the current electronics and have been tested with different event occupancies.

For testing purpose, it may be useful to not subtract any data at all, and to read the raw ADC data. This is mainly for debugging, and is obtained by forcing a 'reset' on the register storing the pedestal.

After correction, the signal can be negative. We therefore first add a positive value, approximately +256 [2] and obtain a 13-bit number before performing the subtraction, the result being saturated at 0 and 4095. This means that the effective range of pedestal-corrected ADC value is approximately –256 to 3839.

The scheme for this processing is shown in Figure 9, where several control registers are clearly shown: "Clkinvsel" to select if the inverted clock is used, "Oldsubmod" to select between the two modes of pedestal subtraction, "Thresh" which contains the increment for the second method, "Sub zero" to avoid subtracting any pedestal. The top right part of the figure contains a subtractor by 256 (see above the discussion on the constant term added) with negative value saturated to zero to restore a range 0-3839 required by the trigger part.

2.2.3 LLT calculation

The purpose of this processing is to convert the ADC data to 10-bit E_{T} with saturation. The ADC will have a full scale around 10 GeV E_{T} with variations from channel to channel due to the gain of the PMT, but one wants calibrated data with saturation at 10 GeV E_{T} for the trigger. A Look-Up Table is not acceptable as it is not SEU immune. However, the linearity is good enough so that we need only to multiply the (pedestal corrected) ADC value by a number. And we don't need a very accurate calibration.

The proposed solution is to multiply the 12 bits by a 10-bit number, and to select the appropriate bits in the result such that a well-calibrated channel (4095 = 10 GeV E_{T}) will produce a calibrated trigger signal (10 GeV E_{T} = 1023) for a calibration constant of

[2] The value +256 is not a good choice and is presently used in the current electronics. If so, the mean value would be +256 after pedestal subtraction which means that the random fluctuations will flip many bits of the FPGA output with a high frequency. Adding +258 or +254 would probably be safer. This will be decided in the future and is tunable by a triple voting protected register. However, we keep the value +256 in the present document.

512. We can then recover a factor between 0.5 and 2 in gain, without loosing too much in precision. If N_{ADC} is the input data sent for readout, N_C the calibration constant, and N_T the trigger result, the formula is

$$N_T = 1024 \times \frac{N_C}{512} \times \frac{N_{ADC} - 256}{3839}$$

Here again, the parameter 256 can easily be slightly adapted.

The resulting 10 bits are sent towards the TrigSeq FPGA, multiplexed at 80 MHz to decrease the number of necessary lines on this FPGA, and also at 40 MHz for those channels that have to be sent to neighbouring cards.

Another possibility has been added, in case one wants to operate the PMT at reduced gain because of excess anode current or instability with High Voltage: it is possible to shift the 12 bits data by two bits (with the necessary saturation implementation) after the -256 operation and before the calibration. This correspond to increasing the gain of the trigger calibration by a factor four.

It may happen that a channel produces bad data, permanently or intermittently, which may affect the trigger by causing spurious triggers at high rate. It is very simple to mask such a channel, just by setting the gain parameter to zero. Then the signal sent to the trigger FPGA is always zero, and the channel is ignored in the trigger. It is also foreseen to mask channels at the entrance of the trigger FPGA

2.3 Pattern and signal injection, data spying

The idea is to inject a known pattern of 12 bits in place of the ADC input, very early in the processing. The choice of ADC or test pattern is done by a multiplexer controlled by one bit of the channel registers protected by triple voting. Each channel can therefore be selected individually to be in the pattern mode or in the normal ADC mode. Three memory blocks, 16 bit wide, of the FPGA can be configured to fake for example 1024 words of 4 x 12-bits of data. This is enough to generate 1024 successive data words with 4 x 12-bits simulating the output of the 4 ADC. There is no need to protect the pattern from SEU by triple voting since either the test are done without beam or the loading of memory just precede the test. The start of the 1024 values test sequence is controlled by a test sequence command issued by the TrigSeq FPGA. This way the patterns are synchronized between all the FPGA that are in the test pattern mode. The test sequence command itself is generated by the calibration signal of the fast commands.

There exist different ways to use the RAM test:

- The standard one: the RAM address is increased every 25ns by the clock and the sequence of 1024 addresses is initiated by the test-sequence signal, originating in the calibration command of the fast commands (produced by the SOL40 and filtered by the 3CU board) and enabled by the corresponding status of a register. The sequence ends up after 1024 clock cycles.

- A variant with an enable loop bit loaded in a register. In this case after the sequence initialisation, the RAM address counter continues advancing and jumps automatically from address 1023 to address 0.

- Calibration mode where the RAM address is incremented upon reception of a test sequence command. In this case by definition the system will loop after address 1023.

Finally another test can be done by injecting, through a 4 channel 74F125 (Quadbuffers used as switches) and small capacitors, a test charge at the input of the amplifiers. The command pulse is derived from the test sequence pulse from the TrigSeq FPGA. A register in each front end FPGA chooses whether the test sequence pulse triggers this amplifier test or the test pattern described above. In this test all 32 inputs of the card can be tested simultaneously but it is also possible to test any channel individually or any combination of channels.

The data processing of the front-end FPGA is spied before being sent to the GBT-X and to the TrigSeq FPGA in two independent set of blocks of memories. Those memories can be downloaded though SPI in order to check the correctness of the front-end calculations.

3 Low Level Trigger

Electron and hadron candidates are defined as clusters of 2×2 cells in the ECAL and the HCAL, respectively. Their associated E_{T} is the sum of the energies measured in each cell of the cluster. With the upgraded LHCb detector, no distinction is possible between an electron cluster and a photon cluster when using only the calorimeter information. This is why in the context of the LLT, electron candidates is a term that refers both to electrons and photons.

In addition to the E_{T} of the most energetic hadron and electron candidates, the calorimeter LLT algorithms compute the total energy deposited over the entire ECAL and HCAL and the ECAL and HCAL multiplicities. The latter are defined as the number of cells with an energy deposit larger than a given threshold. These quantities may be used for the global event cuts. The first steps of the computations needed to obtain the electron and hadron candidates in the LLT are realised in the TrigSeq FPGA. In summary, the hardware-level processing consists in a rough calibration of the energy deposited in the calorimeter cells (performed in the front-end FPGA, see section 2.2.3) and in the computation of the E_{T} of the 2×2 clusters in each Front-End board. These clusters are added to the raw data on the optical links in order to be further processed in the event building farm by the algorithm implementing the final calorimeter LLT selection or to be possibly used as electron, photon or hadron seeds in the first stage of the HLT sequence.

The calculation of the 2×2 clusters leads to several situations (see Figure 10):

- The four cells are localized on the 4×8 cell region concerned by the FEB. In this case, the situation is simple and the TrigSeq FPGA makes the 2×2 sums from the data received from the front-end FPGA of the board.

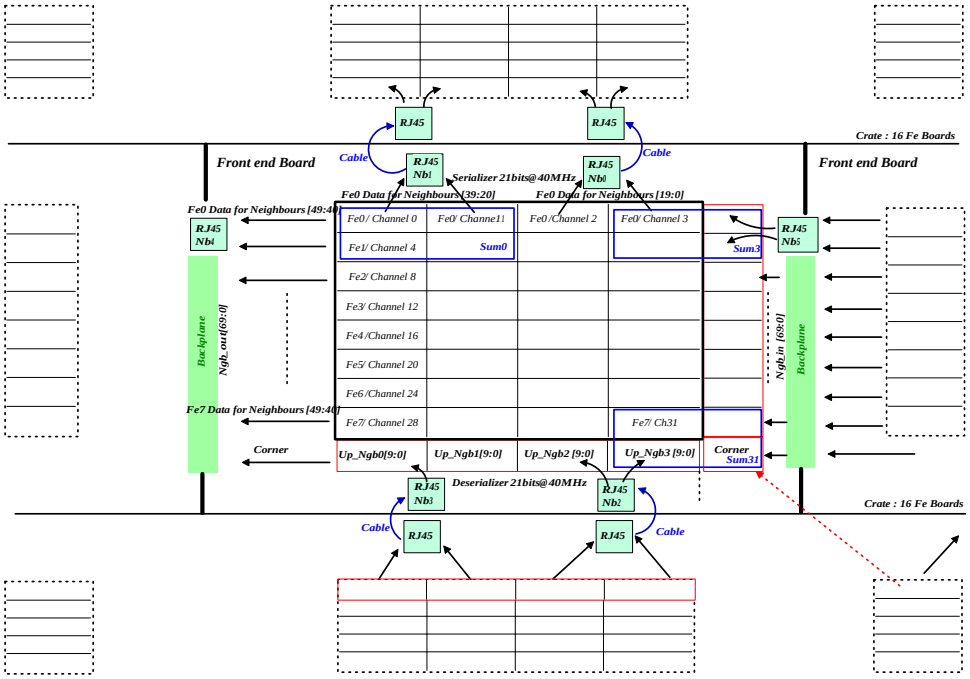

Figure 10: Trigger interconnections between boards and crates.

- The cells are partially localized on regions treated by neighbouring board.
  - If the numbers of the missing channels are even and localized along a column as shown on Figure 10, the FEB will receive the serialized data from the backplane of the crate, as the neighbouring FEB sends them. The TrigSeq FPGA can make the corresponding 2×2 sum after deserialisation of the data.
  - If the numbers of the missing channels are odd and localized along a column as shown on Figure 10, the TrigSeq FPGA does not perform the calculation, the FEB sends the channel data to the backplane after serialisation at 280MHz.
  - If the data are localized on the top row of the region, there are sent to a neighbouring FEB plugged in a different crate after serialisation at 280MHz.
  - If the data are localized on the bottom row of the region of the FEB, there are summed over with the data received from another crate after deserialisation.
  - The case of the corner is a bit specific. It is received from the region below, from another crate and is sent altogether with the data to the neighbouring FEB in the crate (see Figure 10, bottom left). Hence, 9 channels are sent to the neighbouring FEB in the crate.

The total E_{T}, $E_{\mathrm{T}}^{\mathrm{Total}}$ and the multiplicity do not need any interconnections and can be determined easily by the TrigSeq FPGA from the data it receives from the front-end FPGA of the FEB. Figure 11 show the TrigSeq FPGA processing.

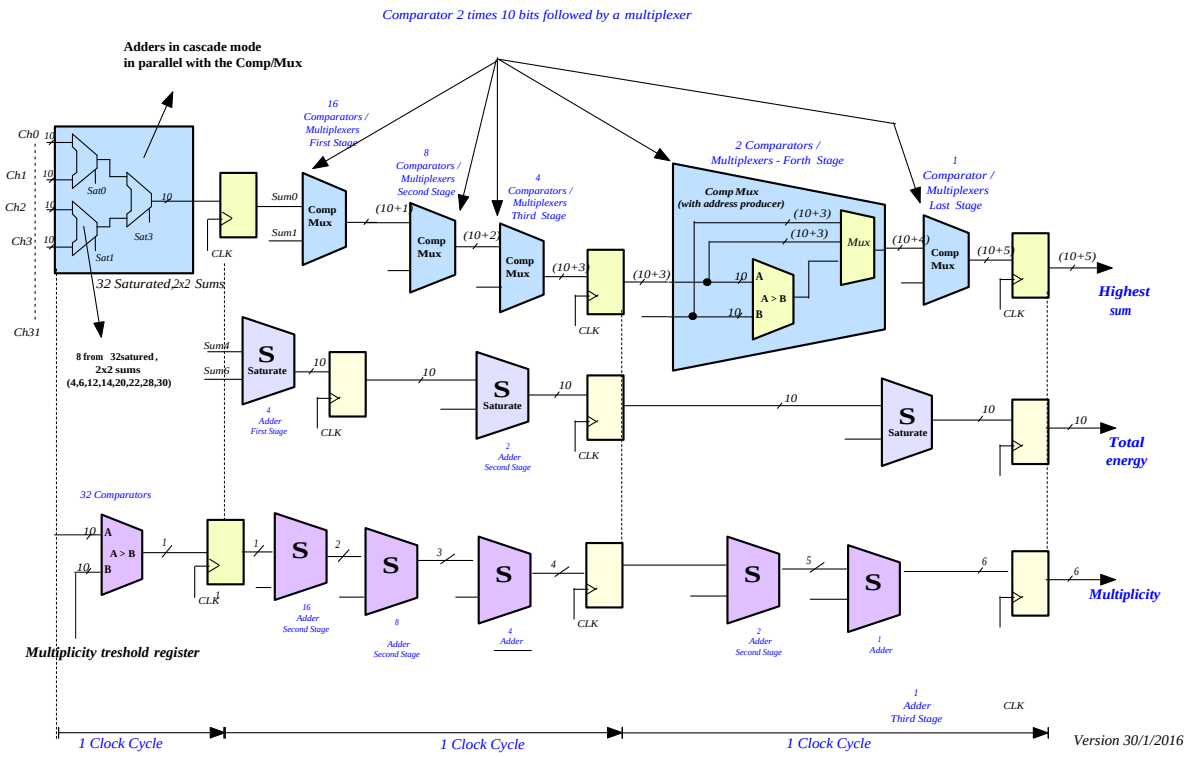

Figure 11: LLT calculations in the TrigSeq FPGA: $E_{\mathrm{T}}^{\mathrm{Total}}$, $E_{\mathrm{T}}^{\mathrm{Max}}$ and multiplicity above a threshold.

After the processing, the amount of data produced by the TrigSeq FPGA is shown in Table 1.

Information	Size (bits)
Addr($E_{\mathrm{T}}^{\mathrm{Max}}$)	5
$E_{\mathrm{T}}^{\mathrm{Max}}$	10
$E_{\mathrm{T}}^{\mathrm{Total}}$	11
Multiplicity	6

Table 1: Size of the LLT parameters sent by each FEB.

The LLT data will be sent split into 4 words, each one being sent to a GBT-X and inserted into the frame of the corresponding optical link. This mechanics is used in order to optimize the usage of the links (which will be configured in wide bus mode) and reduce their number from 5 to 4.

4 Data

4.1 Data format

Each FEB fibre encodes 8 channels ($8 \times 12 = 96$ bits); 8 more bits are used for the LLT whose information is shared among the 4 fibres (we recall that the LLT information is 32 bit wide). The GBT-X will be configured in the wide bus mode giving a bandwidth of 112 bits at 40MHz. Out of the 112 bits per link, the still not attributed 8 bits are used to send the 8 LSB of the bunch crossing identification which has a maximum of 12 bits. We suppose that 8 bits is a sufficient security margin considering the expected latency between the readout and the trigger, on the one hand and among the channels on the other hand. Moreover, the channels as well as the trigger and the data readout should be time aligned at the output, before bying injected into the GBT-X for serialisation. This will be ensured by adding extra latencies at the Front-end FPGA and TrigSeq FPGA output to time align the data. The LLT data in the GBT-X frame should correspond to the channel data word of the same frame.

By sharing the LLT information on the fibres, only 4 fibres are needed to send the full bandwidth. In this scheme, each fibre wraps 8 channels and 8 LLT bits. Table 2 shows the list of the four fibres of each FEB and the splitting of the LLT data among the four fibres.

A specific mode will be implemented so that, the data will be replaced by a crate and FEB identification number. This mode will permit to identify unambiguously any fibre mismatch in the system. The corresponding register will be loaded by ECS and secured by a TVR mitigation.

Fibre	BX identification	LLT data		Data channels							
0	BX< 7..0 >	$E_{\mathrm{T}}^{\mathrm{Total}} < 7...0 >$		0	1	2	3	4	5	6	7
1	BX< 7..0 >	$\mathrm{Addr}(E_{\mathrm{T}}^{\mathrm{Max}}) < 4...0 >$	$E_{\mathrm{T}}^{\mathrm{Total}} < 10...8 >$	8	9	10	11	12	13	14	15
2	BX< 7..0 >	$E_{\mathrm{T}}^{\mathrm{Max}} < 7...0 >$		16	17	18	19	20	21	22	23
3	BX< 7..0 >	Multiplicity $< 5...0 >$	$E_{\mathrm{T}}^{\mathrm{Max}} < 9..8 >$	24	25	26	27	28	29	30	31

Table 2: Data format of the calorimeter electronics readout.

4.2 Optical links for the front-end electronics

4.2.1 Number of links

Table 3 list the number of links needed for the readout of the data, and the control of the front-end crates through the 3CU boards.

5 Slow control and JTAG

The configuration and monitoring of the board can be done in different ways:

- The default mode is based on the GBT-SCA component that provides

DAQ (mono-directional)			
Detector	FEB	FEB (Pin-diode)	Links
ECAL A	94	2	(94 + 2) x 4 = 384
ECAL C	94	2	(94 + 2) x 4 = 384
HCAL Inner	30	2	(30 + 2) x 4 = 384
HCAL Outer	20	2	(20 + 2) x 4 = 384
Total			984

Table 3: List of optical links needed for the readout of the calorimeter data (no spare).

- I2C for the GTB-X,
- SPI for the FPGA and the ICECAL chips.

The GBT-SCA receives its e-port from the GBT-X of the 3CU board plugged in the central slot of the FEB. The levels of the e-port is modified by translators soldered on the 3CU board and on the FEB so that the signal transmission on the backplane is done in LVDS and not SLVS in both directions.

- A USB connection with a configuration and acquisition computer can be used. For this purpose a specific connector is soldered on the board. A small USB interface, FT232H type, (including a FTDI component), can be plugged on the connector. The TrigSeq FPGA embeds a USB decoding/encoding module that permits to convert the USB protocol into another protocole used on the board, either SPI or I2C. The USB interface is not soldered on the board and should be plugged on it on demand as it is not radiation tolerant. It can easily replace the GBT-SCA functionalities for debugging and test purpose.

A JTAG chain (see Figure 16) reaches most of the programmable and configurable components (FPGA and GBT-X). The JTAg chain is accessible by the Microsemi pod, the GBT-SCA, or through a bounding scan test.

6 Clock

The main clock of the FEB may have three sources:

- A LEMO connector on the front-face of the board permit to feed the board with a clock produced by a clock generator. This is for testing purpose only. It should permit to vary the frequency of the clock and to test the margin of the firmware of the FEB, for example.
- The bottom GBT-X may produce the global clock for the FEB. This is also for testing purpose only.

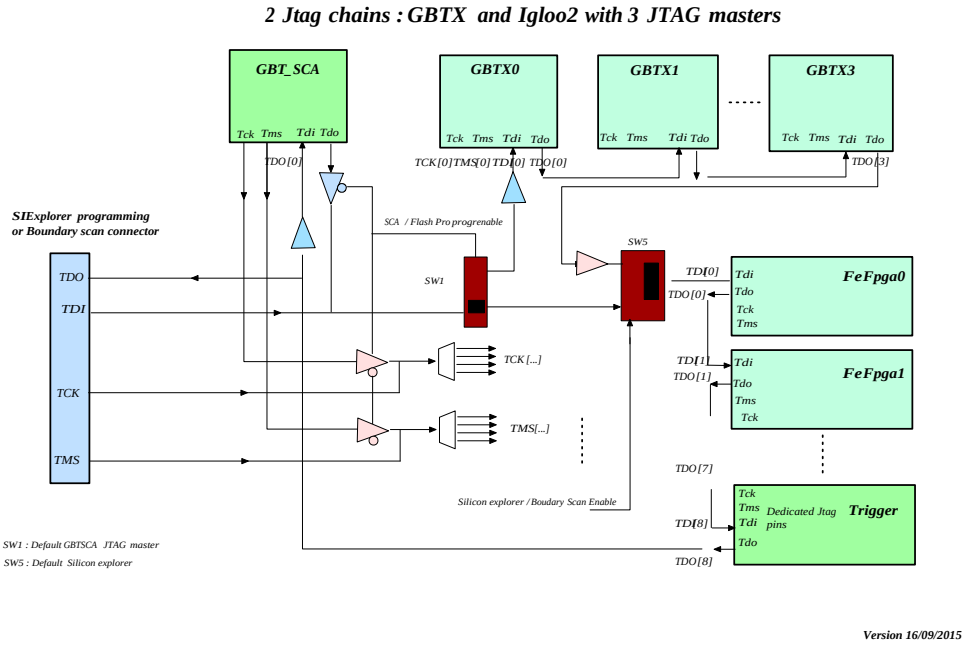

Figure 12: JTAG chain on the board.

- The default mode consists in receiving the clock (LVDS) from the GBT-X of the 3CU that becomes the master.

The clock is sent to the TrigSeq FPGA and to the four FE blocks, see Figure 13.

7 Power supplies

The powering scheme of the front-end crates will also be identical to the present one, a Wiener Maraton being powered at 380V from a rectifier located in the safe side of the wall of the cavern. Nearby the rectifier, the RCM crate and boards give the ability to control the power supply with the online computers. Figure 14 shows the power scheme used.

The front-end boards include a few components leading to a large consumption: eight ICECAL ASICs, 16 dual ADCs, a GBT-SCA, and mainly nine FPGA, four GBT-X and the four corresponding optical line drivers. The voltages requested by those components are: 3.3 (analog), 3.3 (digital), 2.5, 1.5 and 1.2 V. They can be either produced directly by modules of the power supply: 3.3 (digital) and 2.5V. Or through a voltage drop in a DC-DC converter (CERN Feast type): 3.3 (analog), 1.5 and 1.2V. The input voltage for the DC-DC is then 7.0, 5.0 and 2.5V, respectively [3]. Fig 15 shows the power tree of the FEB with the estimated consumption of the electronics connected to the different lines.

[3] In the lab, the power used is not 7.0 but 6.0V and the system is properly functionning. This new value would reduce the power required from the power supplies and would probably increase their long term reliability. We plan to tune the Maraton power supplies to this voltage instead of 7.0V

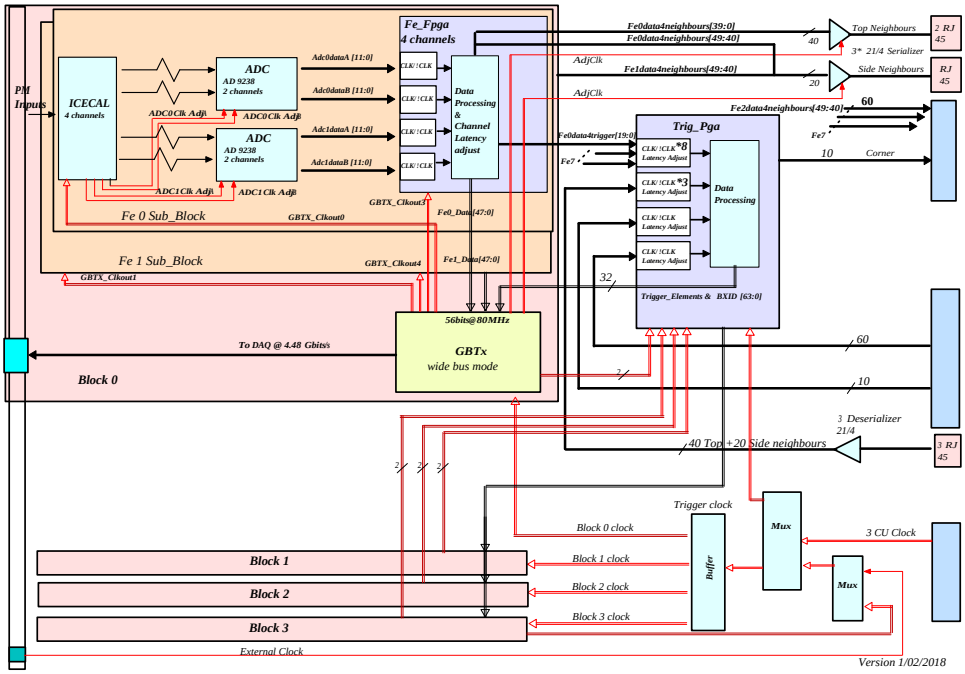

Figure 13: Schematics of the clock tree.

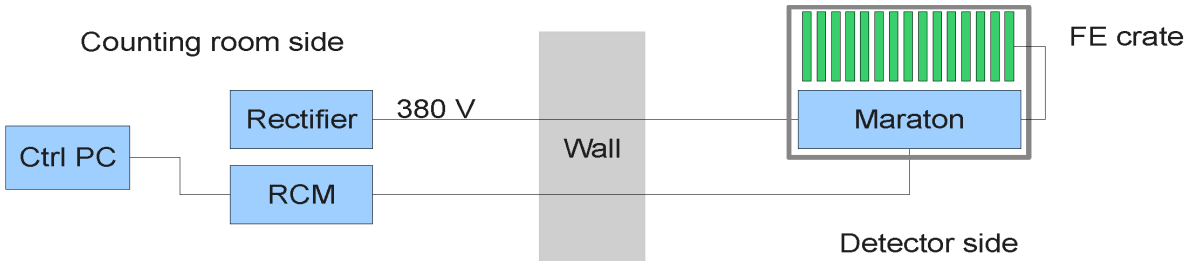

Figure 14: Power sheme used for the Maraton PS used to power the front-end crates.

Input (V)	DC-DC	Output (V)	DC-DC power(A)	Power (W)	Current (A)
7.0 X	3.3	3.0	9.9	1.4	
5.0	X	1.5	7.0	10.5	2.1
5.0	X	1.2	1.5	1.8	0.4
3.3		3.3	2.0	6.6	2.0
3.3	2.5	5.0	12.5	5.0	

Table 4: Summary of the estimated consumption of a board.

Table 5 gives the list of the voltages required and whether a voltage drop is obtained

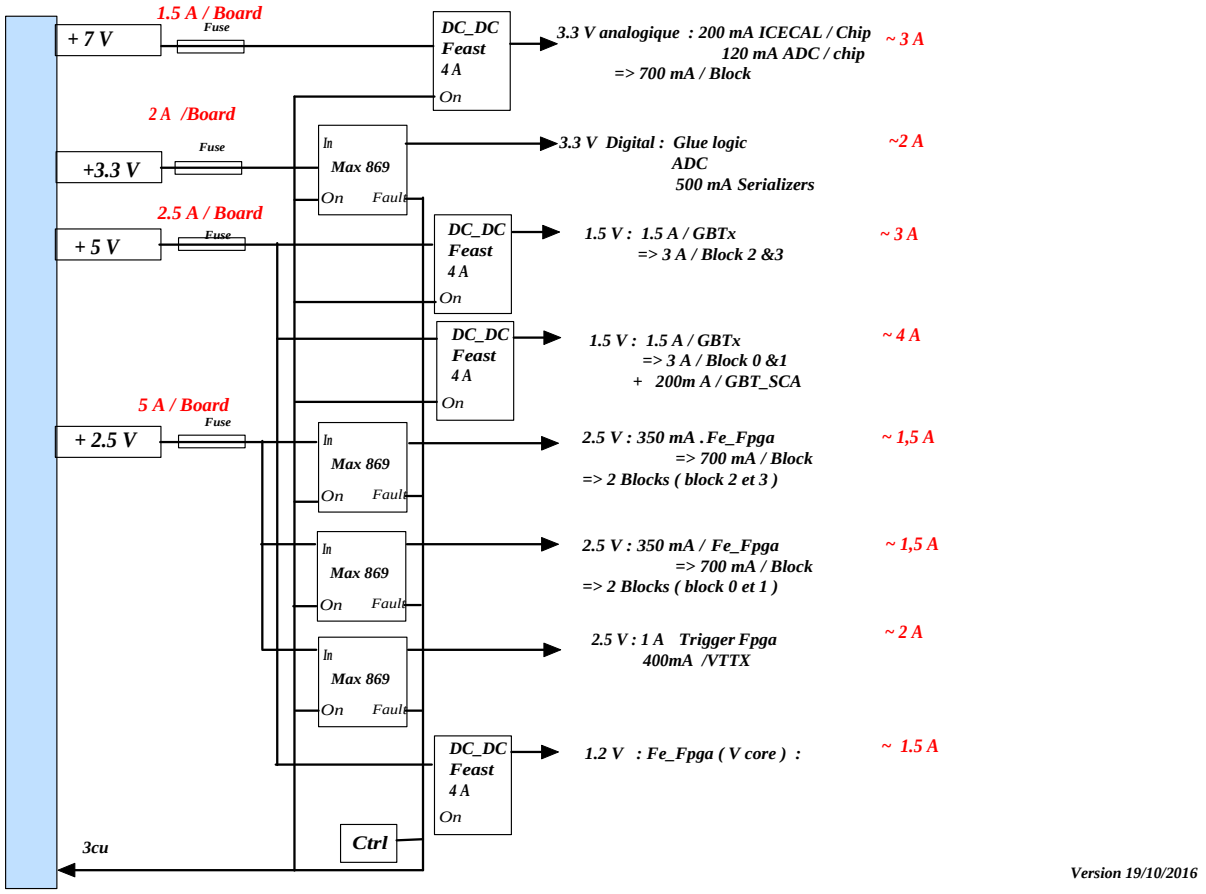

Figure 15: Power tree of the Front-End board.

from a DC-DC converter or if the power is obtained directly from the crate and the power supply. It also gives a total estimate of the consumption of a board.

Several power lines on the board are protected by delatchers of type MAX 869, as indicated on Figure 15. In case of overcurrent (the threshold is set by a resistor network), the delatcher will open the circuit. This is useful in case of single event latchup (SEL). SEL can be triggered by the passage of a particle through a component. The ionisation of the medium of the component can lead to a short circuit between the power and the ground and may eventually destroy the component. A delatcher, by opening the power circuit, should clear the SEL before the component is damaged.

8 Radiations

The components of the FEB have all been either qualified independently or tested in July 2016 during an irradiation test at Louvain-la-Neuve with 62MeV protons. The flux during the irradiation was such that on average we could obtain 50krad in 30 minutes.

The components tested are

- OPA4350EA,
- BFR92A,
- FDV305N,
- IDT8SLVD1204,
- SN74AVC4T774PW,
- MMBT3094,
- NB6L11S,
- HC14,
- AD9238.

Table 5 gives the dose delivered to each type of component and each component irradiated (up to 8 components per type). For all the components, the current pulled was monitored. In the case of the ADC, an analog ramp was injected at the input. The digital output was compared with the signal continuously during the test.

No specific current drift, single event effect or unexpected behaviour was observed during the test in spite of the cumulated dose reached.

Component	1	2	3	4	5	6	7	8
OPA4350EA	70	70	70	70	70	70	70	70
BFR92A	50	50	50	50	50	50	50	50
FDV305N	50	50	50	50				
IDT8SLVD1204	50	50	50	50				
SN74AVC4T774PW	50	50	50	50				
MMBT3094	50	50	50	50				
NB6L11S	50	50	50	50				
HC14	50	50	50	50				
AD9238	50	100						

Table 5: Dose delivered (krad) to up to 8 samples of each component type tested.

In the cavern of LHCb, we expect up to 5krad for 50fb^{-1}. The simulations performed for the design of the current detector show that at the maximum upgrade luminosity and during the full period of activity of the experiment, the flux in the worst location of the electronics will be 4.2×10^{10} particles per cm^2, mostly low energy neutron.

Table 6 shows the comparison of the flux delivered during the test with the expected flux reached during the full activity of the calorimeter electronics. The limit on the number

Component	Fluence cm^{-2}	$/50fb^{-1}$	#Test	SEL (limit)	Limit (HI)
OPA4350EA	4.2×10^{12}	100	5x250	12.5	0.125
BFR92A	3.0×10^{12}	71.4	5x250	17.5	0.175
FDV305N	1.5×10^{12}	35.7	5x250	35	0.35
IDT8SLVD1204	1.5×10^{12}	35.7	5x250	35	0.35
SN74AVC4T774PW	1.5×10^{12}	35.7	5x250	35	0.35
MMBT3094	1.5×10^{12}	35.7	5x250	35	0.35
NB6L11S	1.5×10^{12}	35.7	5x250	35	0.35
HC14	1.5×10^{12}	35.7	5x250	35	0.35
AD9238	1.1×10^{12}	26.2	16x250	150	1.5

Table 6: Estimated radiation tolerance of the components tested. The fluence is given per cm^{-2} first, then with respect to the fluence expected for $50fb^{-1}$. The number of components necessary to equip the full system and the number of SEL expected during the activity of the electronics (this number being a maximum limit) are also given. The last column is the same limit assuming an heavy ion test with an efficiency 100 times larger.

of SEL expected during the full life of the experiment and for the full electronics is given. This is only a limit as no SEL has been observed. Considering that a heavy ion test is 100 times more efficient, the same number but with a heavy ion beam is also given.

Notice that the doses reached during the test make our component tolerant to the dose expected in the cavern.

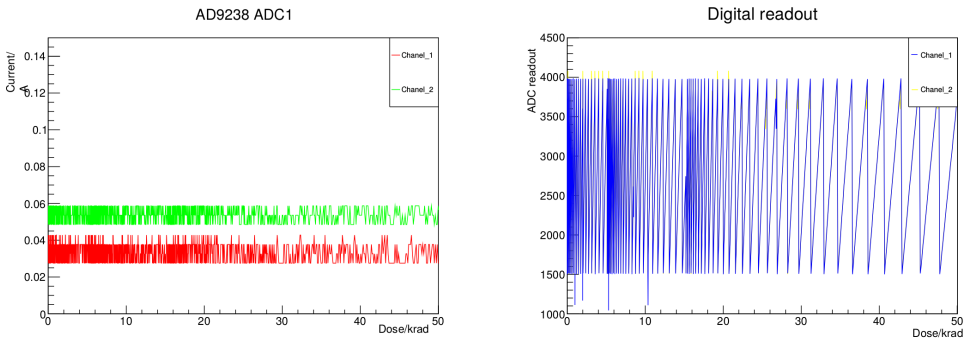

Figure 16: Measurement of the current pulled by the ADC and the response to a ramp during an irradiation with protons up to 50krad.

9 Performances

9.1 Optical path

9.2 Data acquisition

The data stream has been tested by loading the injectio RAM with specific values. Then, an acquisition through the optical link is performed and the MiniDAQ is used to store the data value. The values stored on the MiniDAQ are then compared with the values loaded into the FPGA of the FEB.

9.2.1 Bunch crossing identification number and synchronisation

The bunch crossing identification is calculated by the Trig-PGA and sent to the optical fiber altogether with the data and LLT values. The firmware has been written and the continuous increase of the Bunch crossing identification number has been tested.

A specific mode permits to synchronize the optical fibers. In this mode, the FEB sends the BXId on 12 bits (instead of 8 in data mode) and a fixed pattern on the remaining bits. This mode can be triggered for 10 consecutive samples. And it was checked that the synchronisation of the fibers is obtained.

9.3 Noise

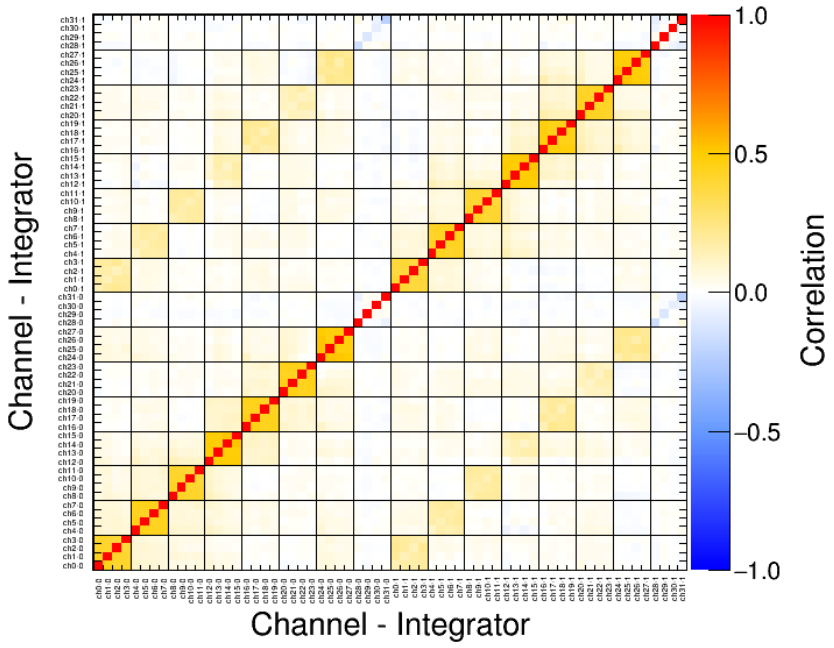

Figure 17: Noise correlation between subchannels.

The noise has been measured by performing an acquisition of the data without injecting any pulse at the input of the board. Noise correlation between the two integrators of a channels, between two channels of a group of 4 channels corresponding to an ICECAL and between two channels belonging to two different ICECAL components.

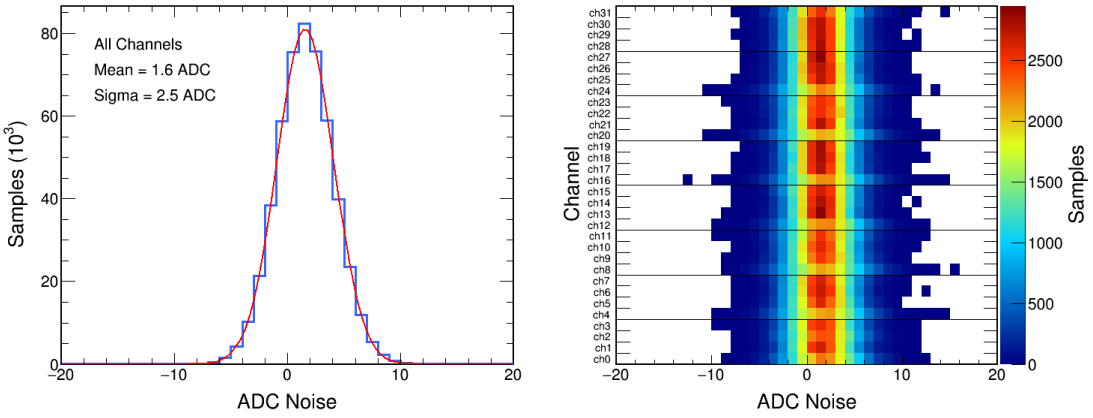

Figure 18: Noise averaged over the 32 channels of a board (left) and for each channel of the board (right).

The noise reaches typically 1.8 ADC counts without subtraction. However, the subtraction which has been used in our test consists in removing from the current sample the smallest sample stored at $n-2$ or $n-4$. Hence, by performing the subtraction and supposing the two samples are uncorrelated, we get an extra factor $\sqrt{(2)}$ on the current noise.

The Fig 18 shows the averaged noise for all the channels and gives the detail of the noise per channel. In both case, the measurement is performed after subtraction, leading to an extra contribution as explained above.

The correlation of the noise (see Fig 17) depends on the two channels considered:

- Two integrators of the same channel: ≈45%
- Two channels of the same ICECAL chip: ≈17%
- Two channels belonging to two different ICECAL: ≈3%

9.4 Linearity

The linearity is measured by injecting an alalog pulse of high amplitude into the FEB. A precise attenuator is used in order to reduce the amplitude of the pulse. The data are stored and the linearity is extracted.

A linearity of ≈ 2% is obtained on the dynamic range. Figure 19 shows the amplitude measured with respect to the attenuation applied. Some distortions have been observed

of the order of ≈1%, but they vanish by changing the attenuator. We also checked the linearity curve for several channels belonging to other blocks and the curve is almost identical, making us confident that the distortions observed, which are nevertheless limited and are in specification, are related to the attenuators.

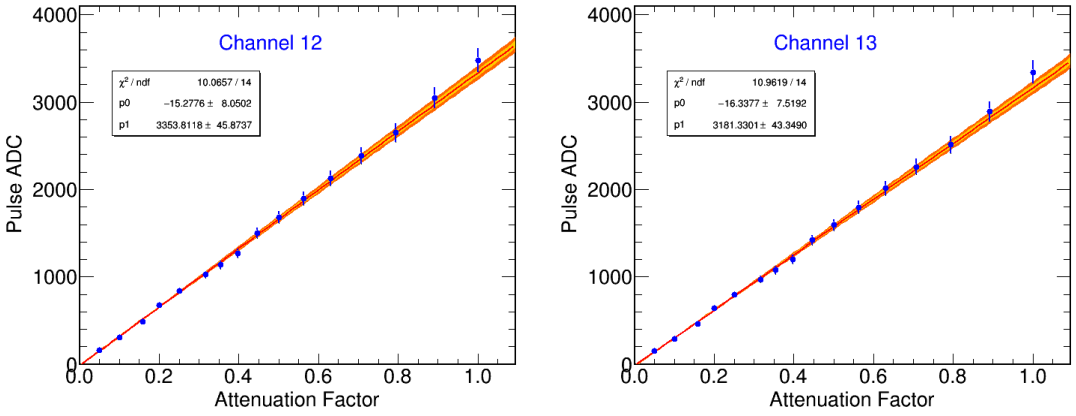

Figure 19: The linearity curves on two channels of the board.

9.5 Cross-talk

The cross-talk has been looked at by injecting a pulse on one channel and determining the digital signal seen on the other channels. Depending on whether the second channel is has a cable and a 50 ohms termination or is open, without cable, the cross-talk is very different. The figure 20 shows the crosstalk for the second situation which is pessimistics. In the former case, the cross-talk is negligible and has been measured to be less than ≈1%.

9.6 Time stability

The time stability has been looked at with a pulse which has been recorded in test beam with the appropriate cables. The pulse is injected in the electronics and a timing scan on the integrator clock and on the ADC clock is performed (see 21. The timing stability is measured to be better than 1% over ±2 ns on the integration pulse. The stability is even better on the ADC setting. This is in the performances requested.

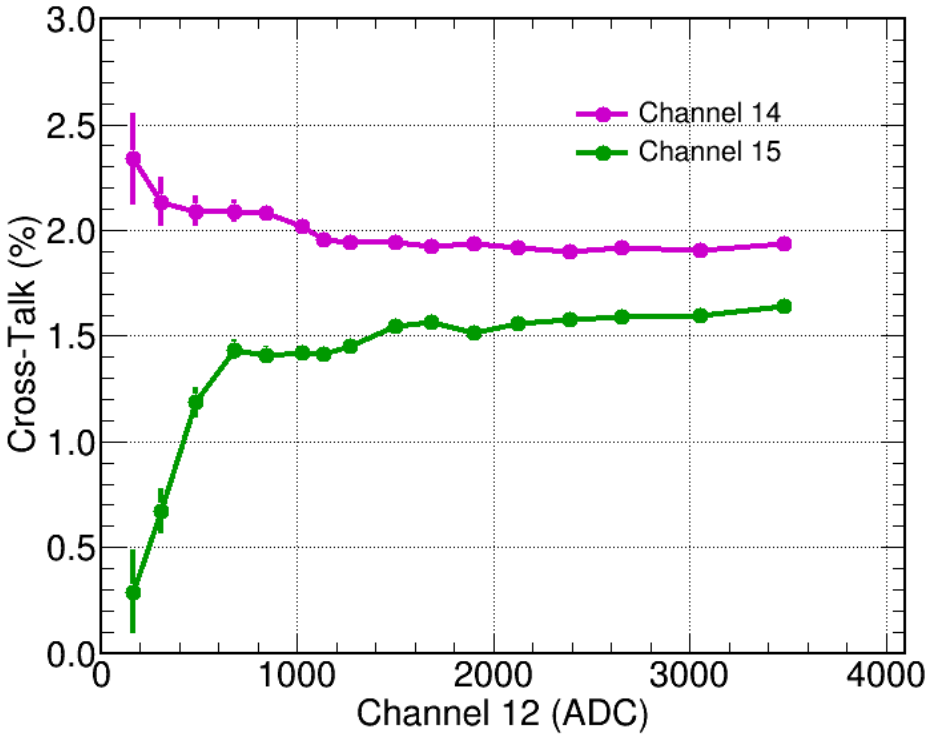

Figure 20: Cross-talk seen by pulsing a channel and looking at the next one. In this case, the second channel is not connected to a cable with a 50 ohms connexion eading to a pessimistics measurement.

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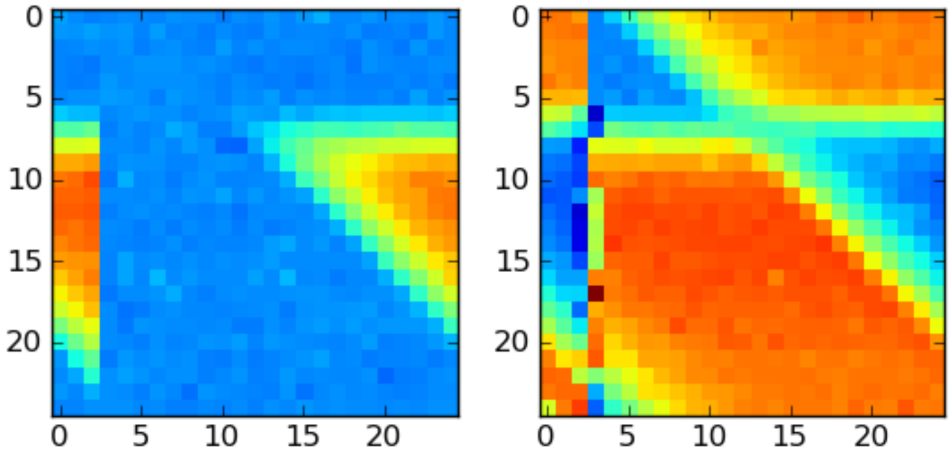

Figure 21: Plot showing the result of the synchronisation scan. The x axis corresponds to the ADC sampling clock phase tuning and the y axis to the ICECAL integration clock configuration. The colour indicates the amplitude of the injected pulse as seen by the acquisition. The two plots correspond to two consecutive samples acquired by the FPGA. For some ADC clock settings, the FPGA with see the pulse in an adjoint sample.

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