HCAL and ECAL Calorimeter Front-end board PRR

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Overview

The objective is to replace the 246 + spares existing Feb with new boards (300) adapted to the new requirement/architecture of the experiment.

The increase of the luminosity and consequently the volume of data produced by the detector leads to suppress the bottleneck of the L0 derandomiser and the circular memory associated to the latency trigger and transmit all the data to the DAQ.

Consequently it is about ~50 time the actual amount of data that the Feb will produce.

The 2 Calorimeters are part of the L0 Trigger.
Part of the L0 decision is built in the Validation board, receiving information from the Feb via the backplane (2 Validation per crate) and from the Preshower and SPD. This card and these 2 subdetectors are no longer used.

Overview

- The part of the trigger elements calculated on the Feb have a dynamic enlarged and are transmitted together with the Front-end data to the TELL40.

  - The timing performance showed a large advantage to calculate the trigger elements at the FEB level rather than in the farm.

    ~3 ms per event in the Farm to calculate the Sum and address compare to few clock cycles in the FEB plus ~10 us to decode it in the FARM

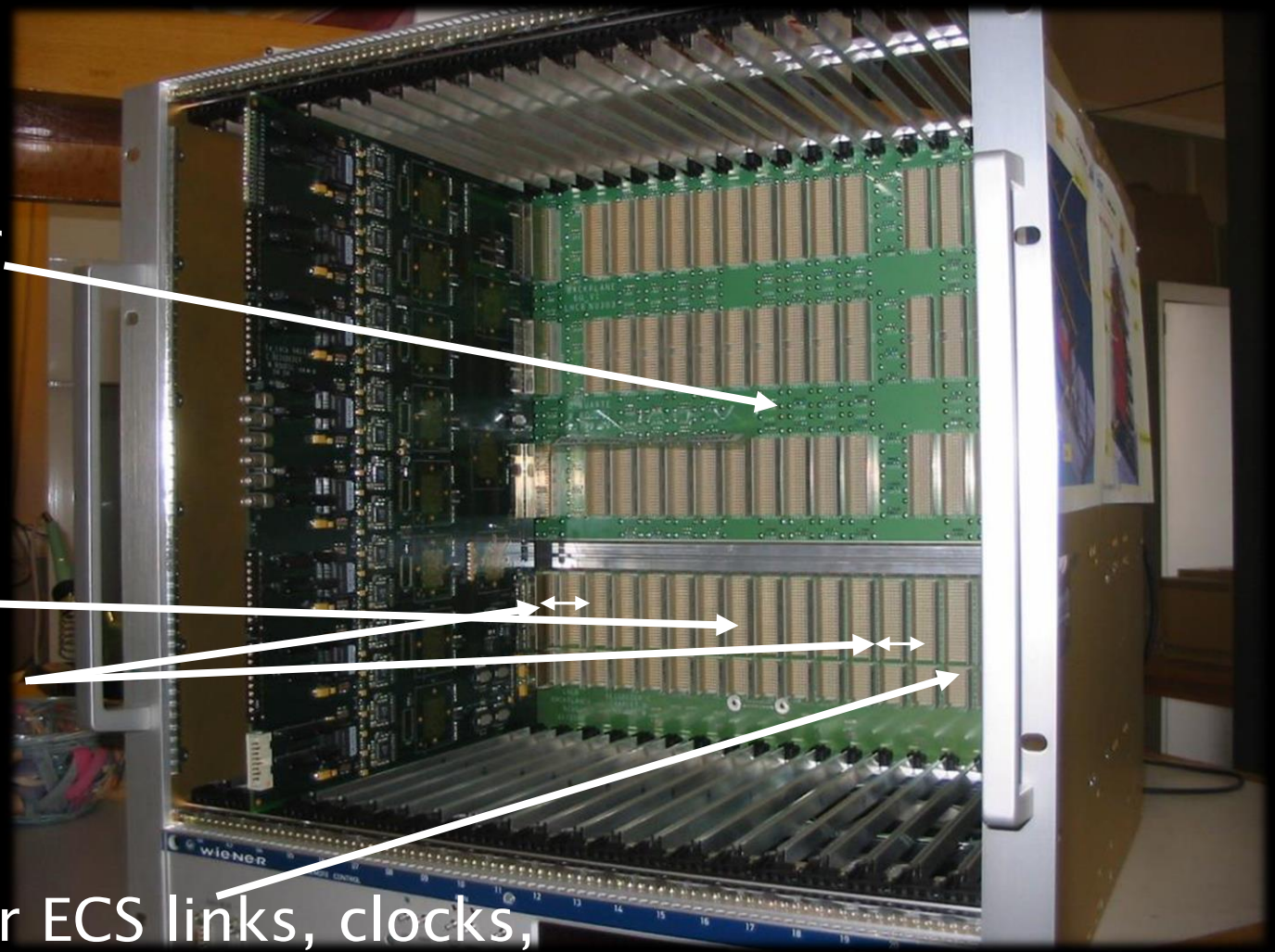
- The control board CROC is fully redesigned (rename 3CU) and the Validation boards are removed.

- The crates, their location on the balconies, the backplane and the interconnection between crates are unchanged .

- Power supplies are kept and adapted to the new requirements in term of voltage and current.

Overview

The Calorimeter Crate



Overview

- The Feb receives the 32 PMT signals via ~ 15 meter long cables from the HCAL and ECAL detectors.

- The Feb performs @ 40 MHz:

  The shaping and the integration of the analog signal thanks to the ICECAL chip.
  The 12 bit conversion thanks to a commercial ADC.
  The processing of the signal in FPGA–Microsemi (ACTEL) Igloo2 family.
  - The pedestal subtraction and low frequencies noise cancellation
  - The numerical correction and the event formatting
  - The trigger calculation

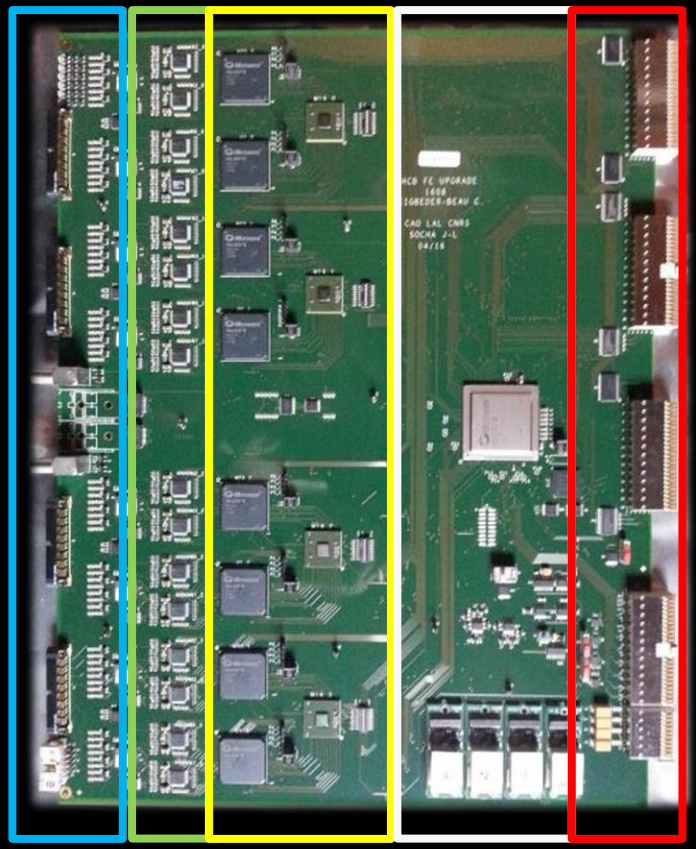
- The Feb transmits and receives Fe data from its left and up side neighbours via the backplane (@40 MHz) and Cat5 cables after serialization (21bits@40 MHz) for the trigger calculation

- The Feb transmits Fe data together with the trigger elements and the BXID information to the TELL40 via 4 optical fibers (2 VTTx) .

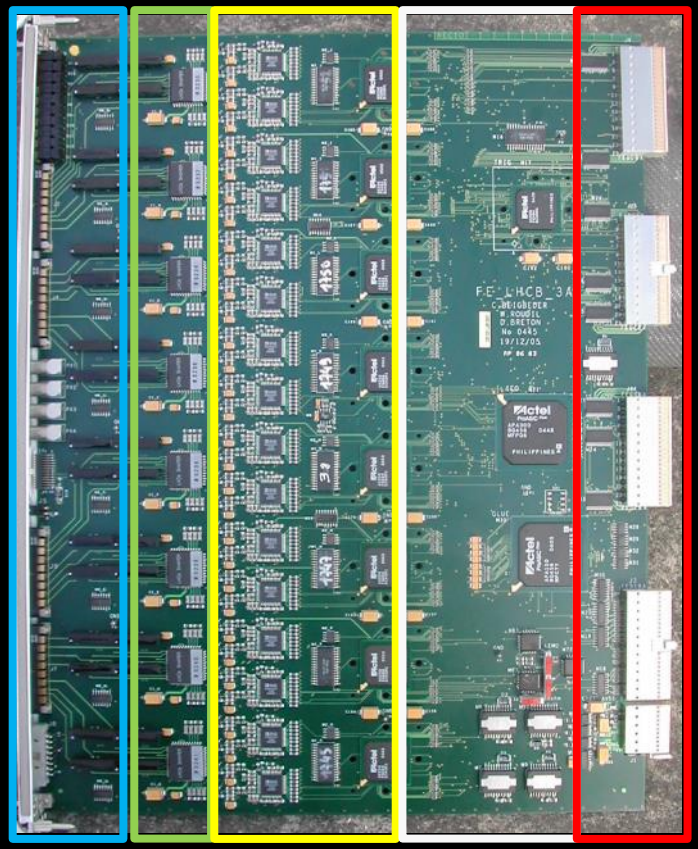
Overview

The global architecture and the topology of the Feb looks similar compare to the old version even if almost all the components have changed.

New version



Previous version



Front panel Analog input

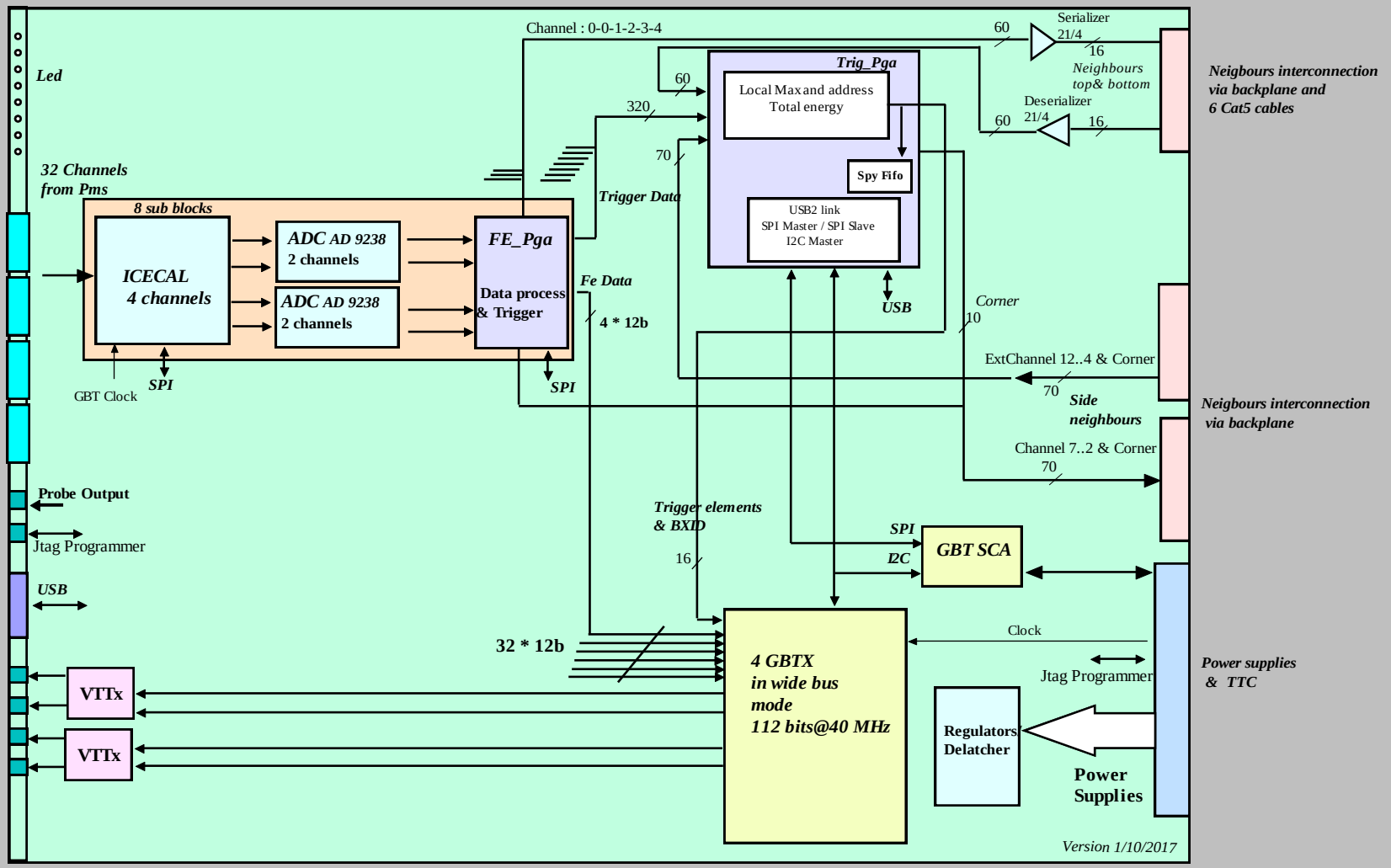
Analog part

Digital part

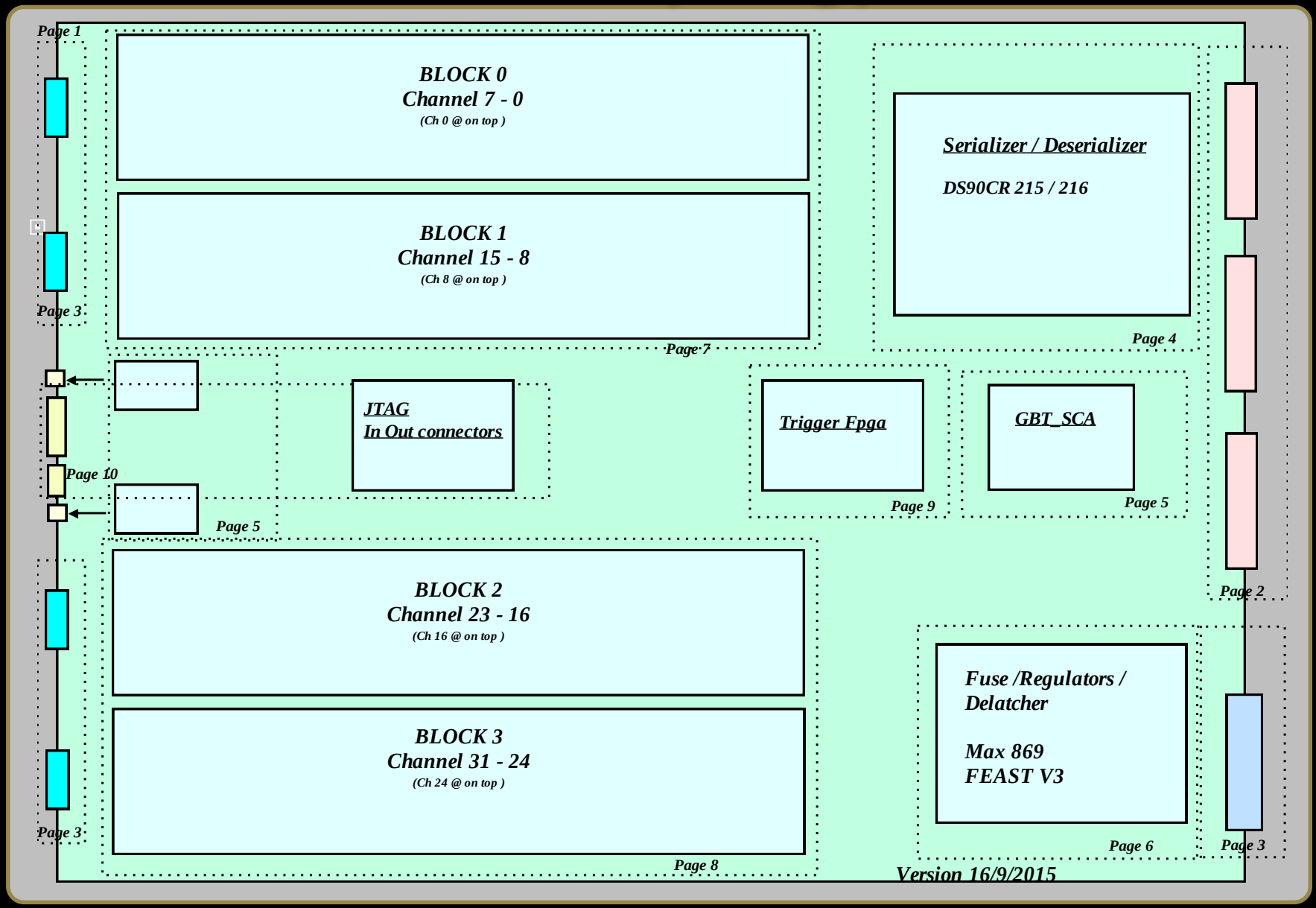
Digital part Ctlr and ECS.Regulators

Interconnection Power

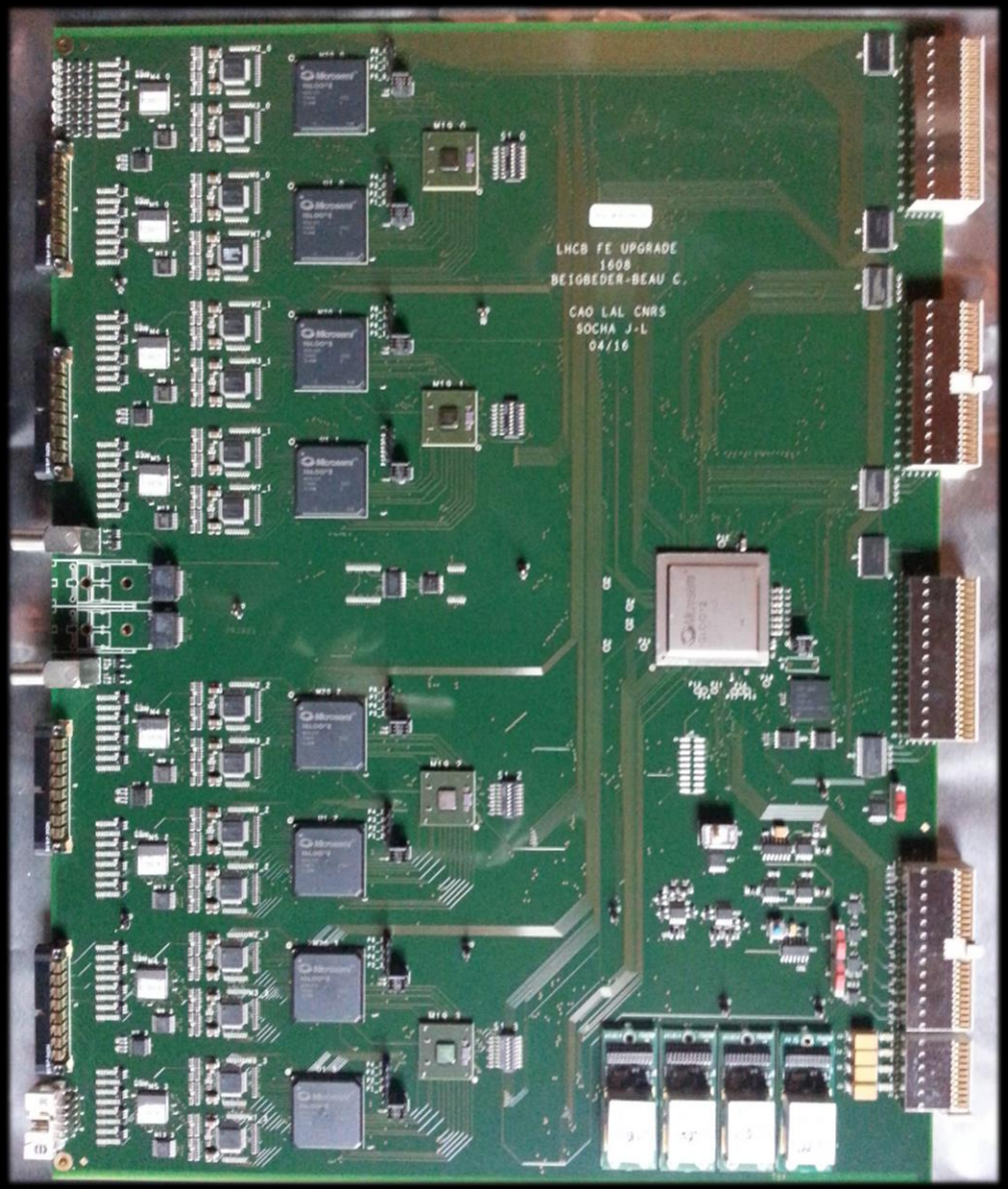
Feb : simplified synopsis



Feb-Topology



Feb proto 1

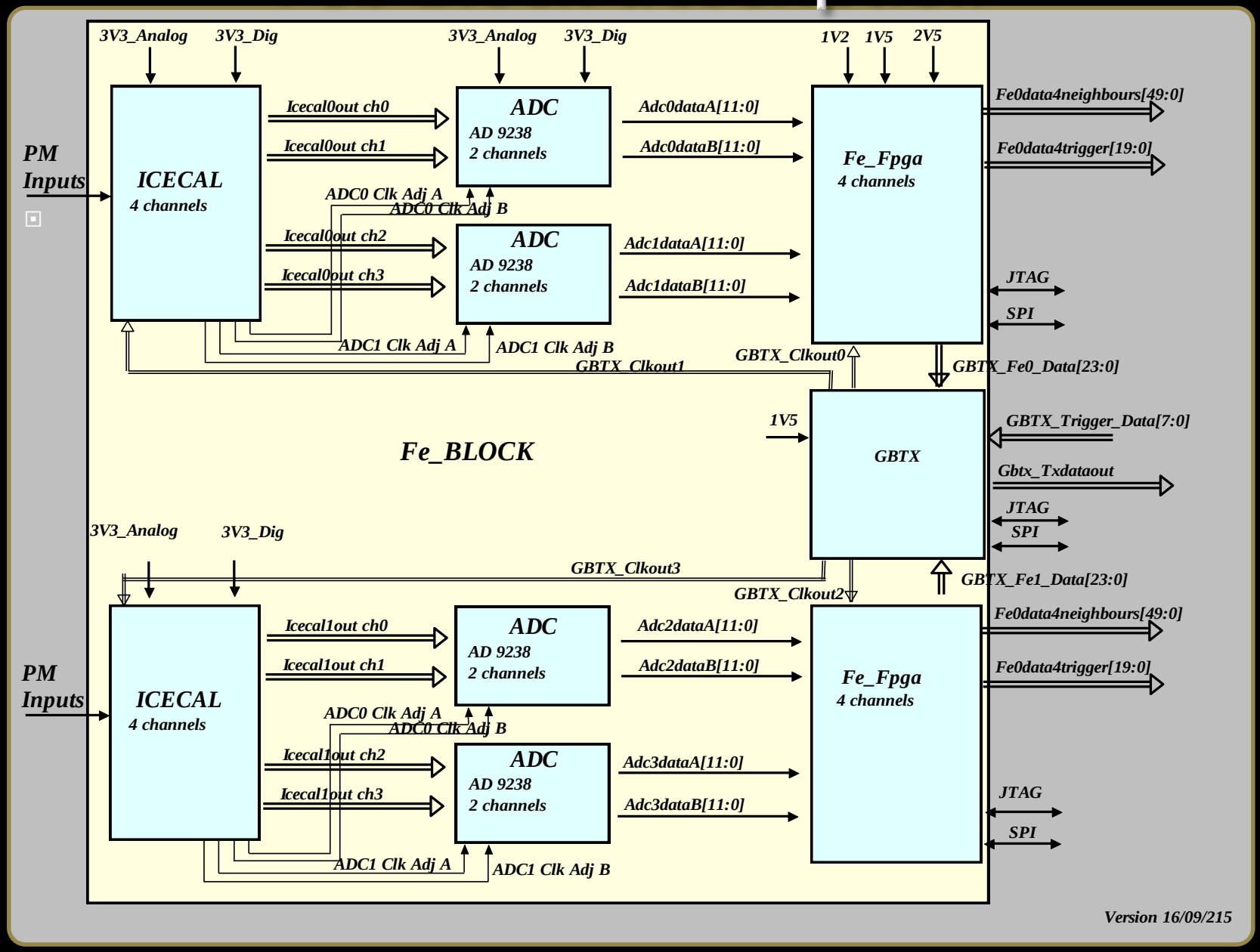


- Feb : CAD Cadence
  - 12 layers
  - Class 7
  - 3950 components
  - 3535 wires
  - Printed board : Pro Techno
  - 4600 E / 3boards
  - Cabling : LAUDREN
  - Cost : 7500 (2100)

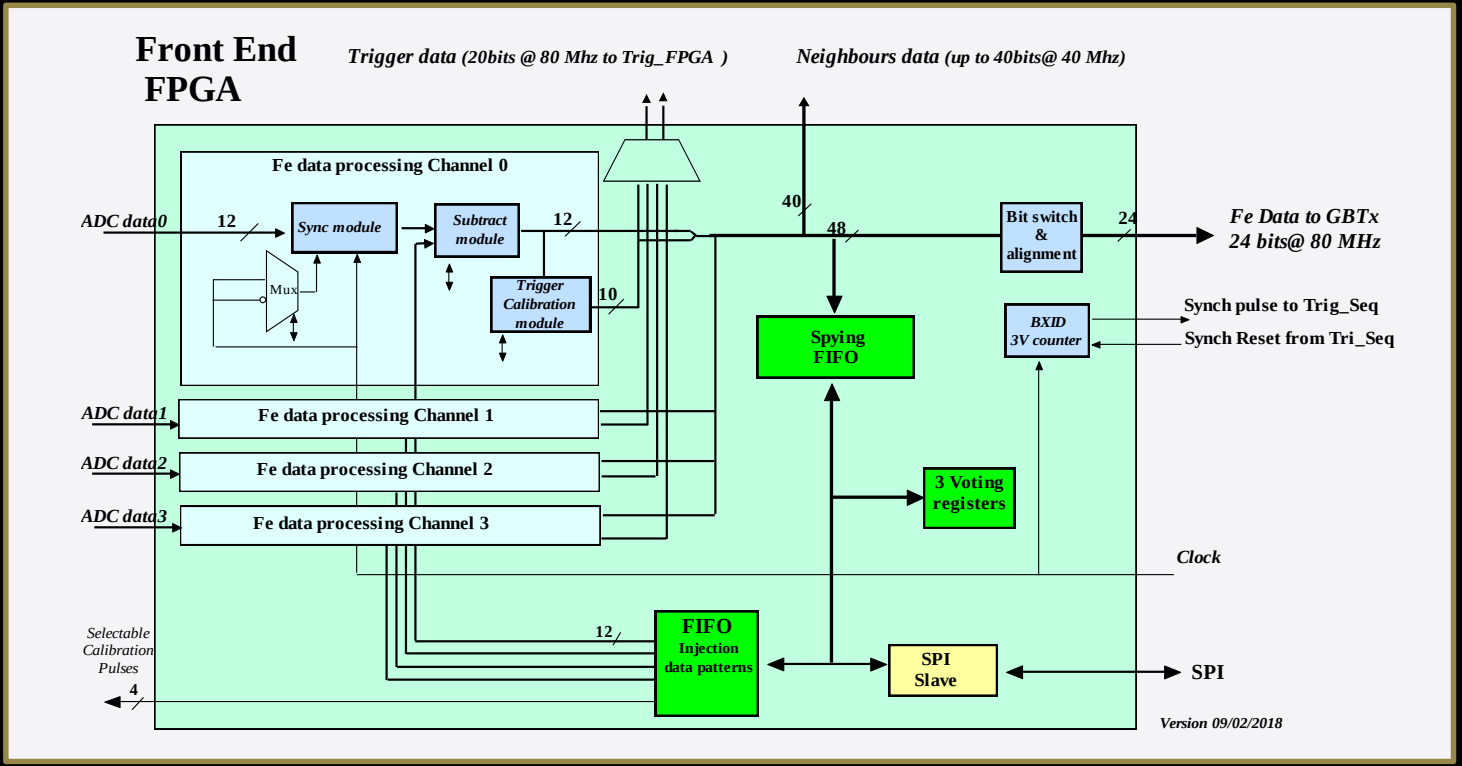
Overview

Presentation of the the ICECAL chip

Feb Block description



Feb : Front end FPGA



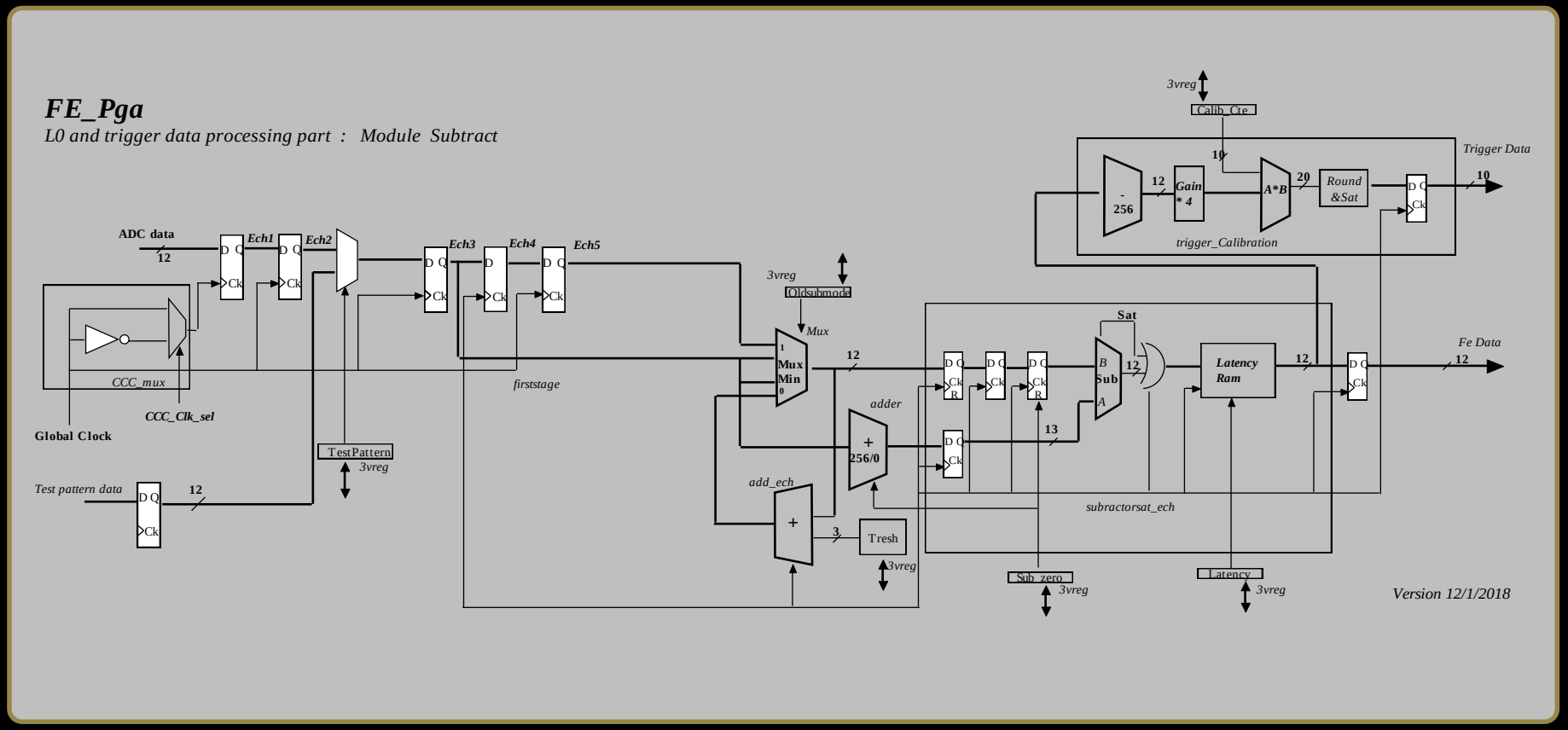
Fe FPGA is divided in 3 different modules :

- One process the ADC data : resynchronize and remove the low frequencie noise, transmit the data to the GBTX
- One calculate the LLT and transmit the data to the TrigSeq FPGA or the neigbouring Feb
- One is dedicated to test and debug with injection and test FIFOs

Fe FPGA signal processing

Three stages to process the incoming 12 bit ADC data :

- Resynchronization on Clk/!Clk and pipeline to" generate" t-2 and t-4 samples
- Process to remove the low frequency noise and subtract the pedestal . 2 methods are implemented
- Generate the LLT data after applying a conversion factor : 12 to 10 bits for trigger elements



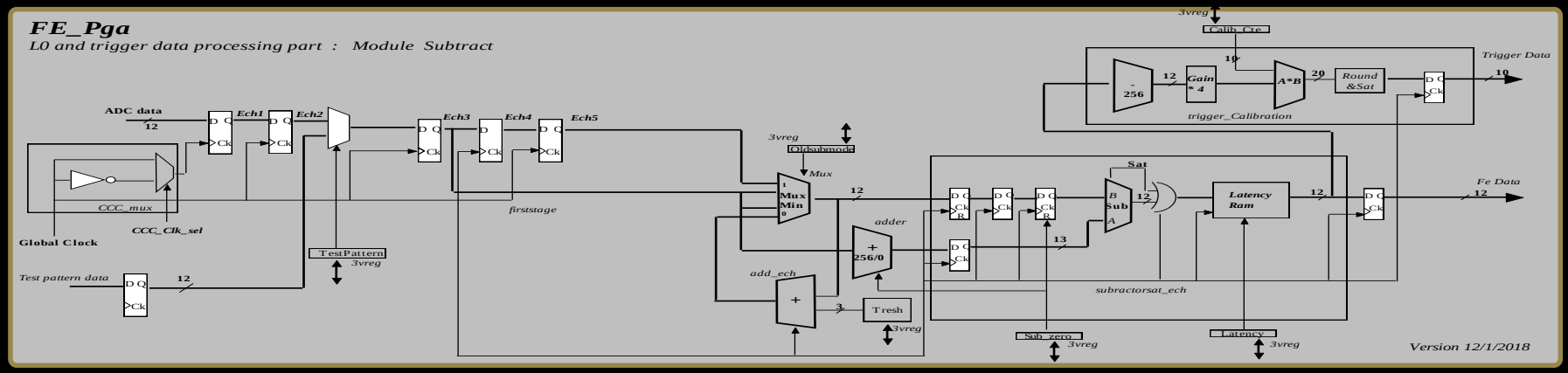
Fe FPGA : signal processing

- Dispertion of the analog signal (PMT,cables) and consequently the clock adjustment for integrating the whole signal in the ICECAL may introduce a phase difference from channel to channel. An adjustable latency is introduced on each channel to adjust and insure they are in the same BC over the all board, the whole crates.

- For low frequency noise removal and the pedestal subtraction, two methods are implemented

  - Standard one: one subtracts the smallest of the 2 previous samples which means the t-2 & t-4 samples (ICECAL chip based on a interleave integrators). Considering the occupancy we to have sizeable signal in on of the two is small.

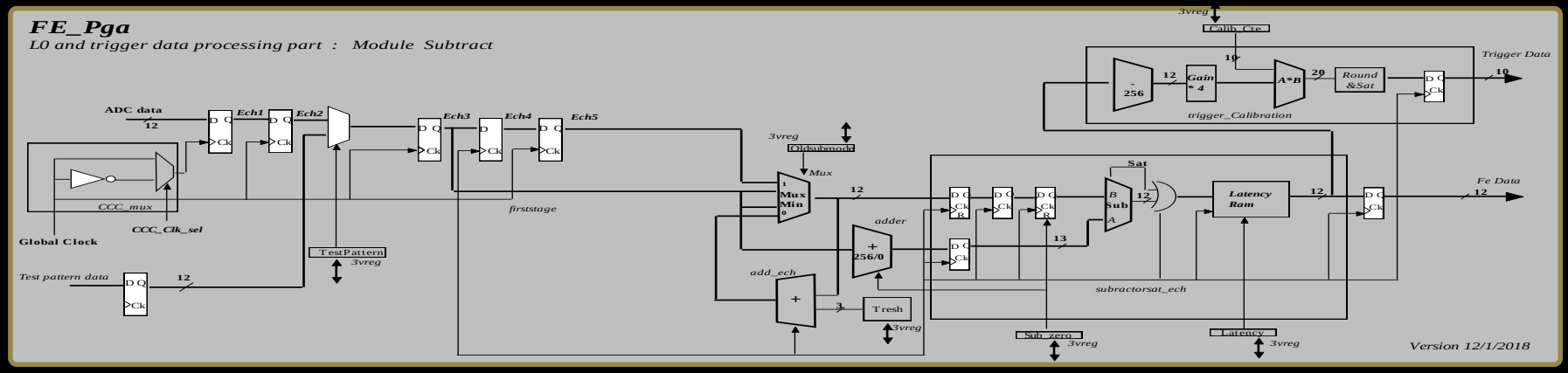
  - Improved one : the estimate pedestal is the previous pedestal plus a constant . This method is better and avoids brutal fluctuations
  Numbers and comparisons of the two methods are fully described on the document EDR page 10.



Fe FPGA : signal processing

- - LLT calculation :
  - We want to move from the actual 5 Gev transvers energy on 8 bits to a better dynamic and resolution of 10 GeV /10 bits.
  - We multiply the 12 ADC bits by a constant (N*c*) on 10 bits. We can recover a gain between .5 and 2 (aging, channel to channel dispersion …) without loosing to much precision.
  - In case a double ramp conversion could be implemented for better precision.

The implemented formula is : NT = 1024 x NC /512 x (NADC -256)/4096

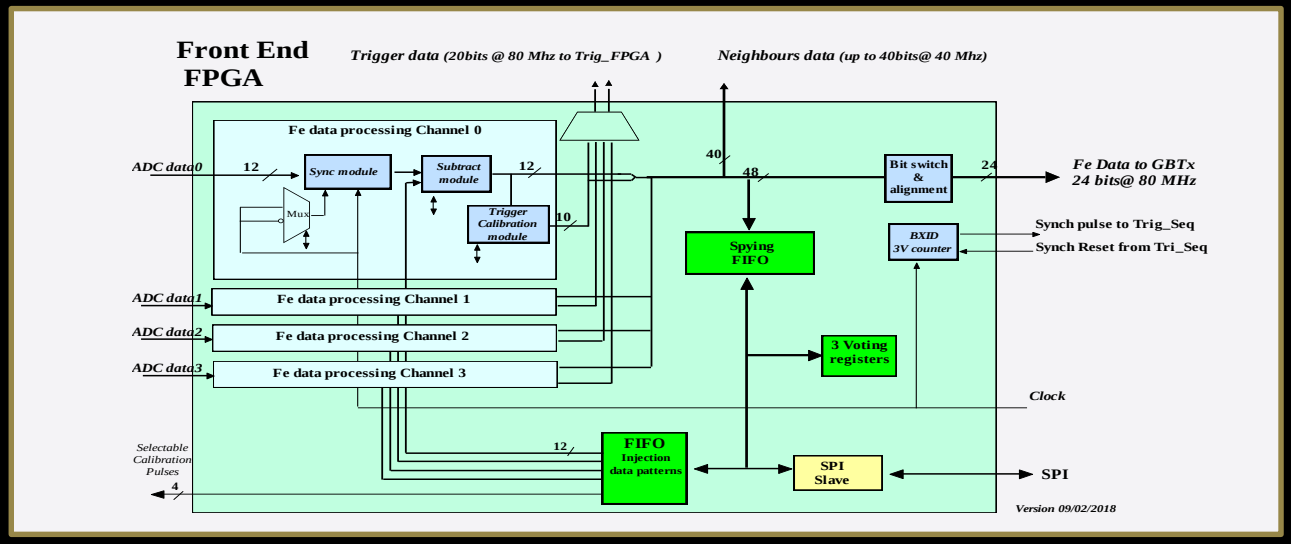


Fe FPGA : debug and test

- Possibility to inject patterns in place of the ADC data . The patterns are loaded in FIFOs (one per channel). Up to 1k words can be generated at 40 MHz upon the reception of a Testsequence signal generated by Trig_Seq FPGA(stand alone test) or the 3CU board (fast commands).

- Possibility to inject analog pulses in parallel with the PMT signals performing a calibration test per channel. The reflection of the signal on the clip gives also information on the reliability of the cable connexion with the board.

- Fe data and Trigger data are spied into test FIFOs

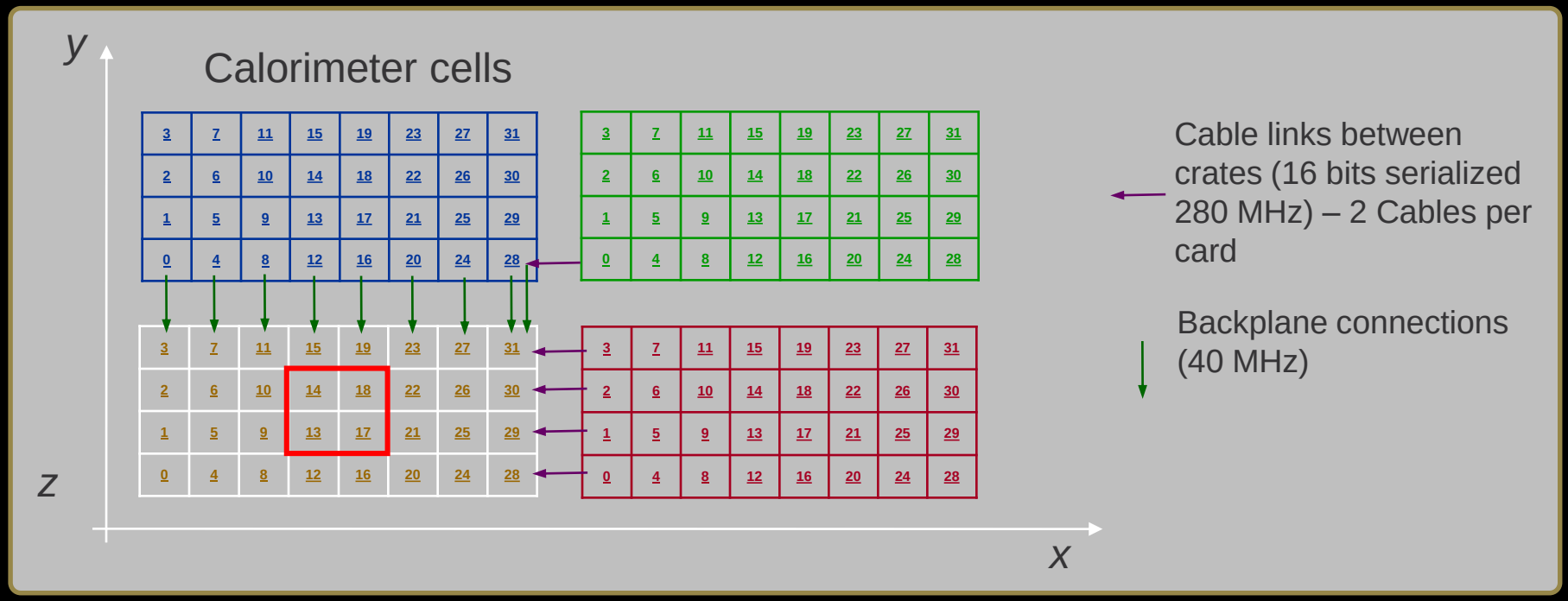


Low level Trigger

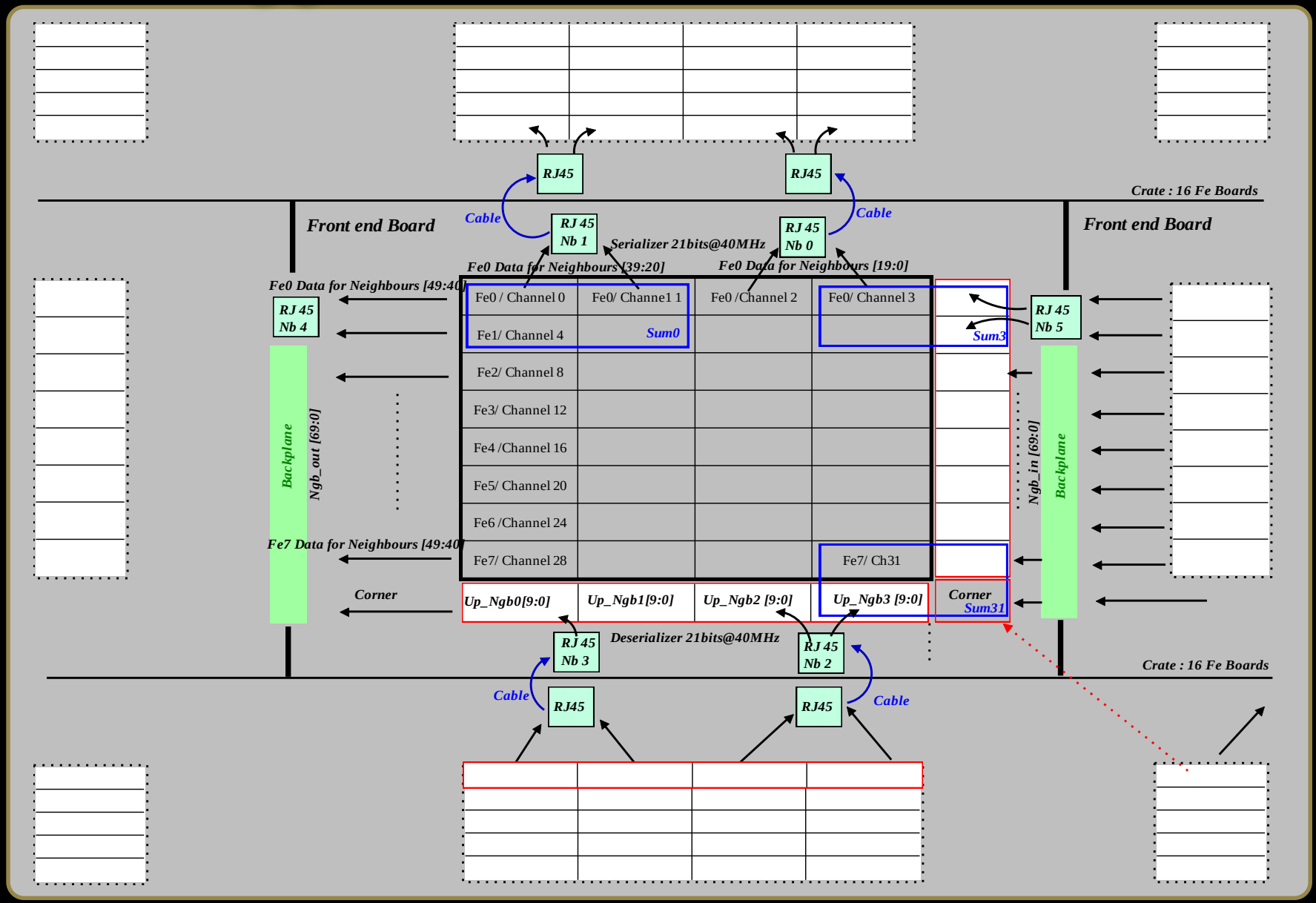
- A cluster is defined as a 2x2 cell in the ECAL and HCAL. Each board calculates the energy of each of the 32 clusters (*ET*) then extract the cluster with the highest energy and its corresponding address. We also calculate the total energy per board and finally determine how many channels are above a defined threshold (multiplicity)

- The calculation of the cluster with channels localized on different boards leads to interconnections between crates or boards.

- The trigger algorithm needs to concentrate all the data in a single chip to process the 45 X 10 bits. ->Trig_Seq FPGA : Actel - Igloo2- MG2L150 -1152 pins

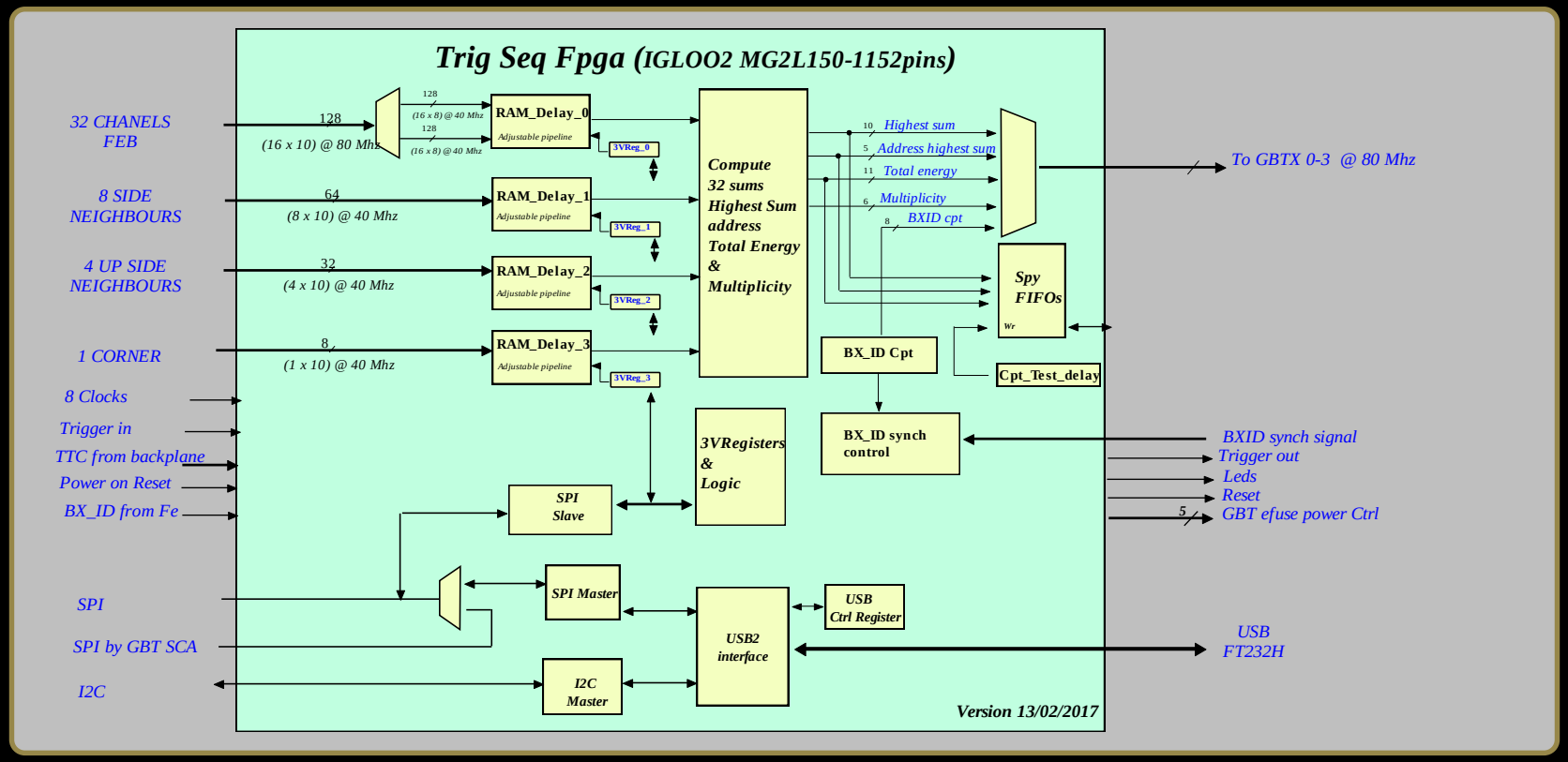


Trigger interconnection: details

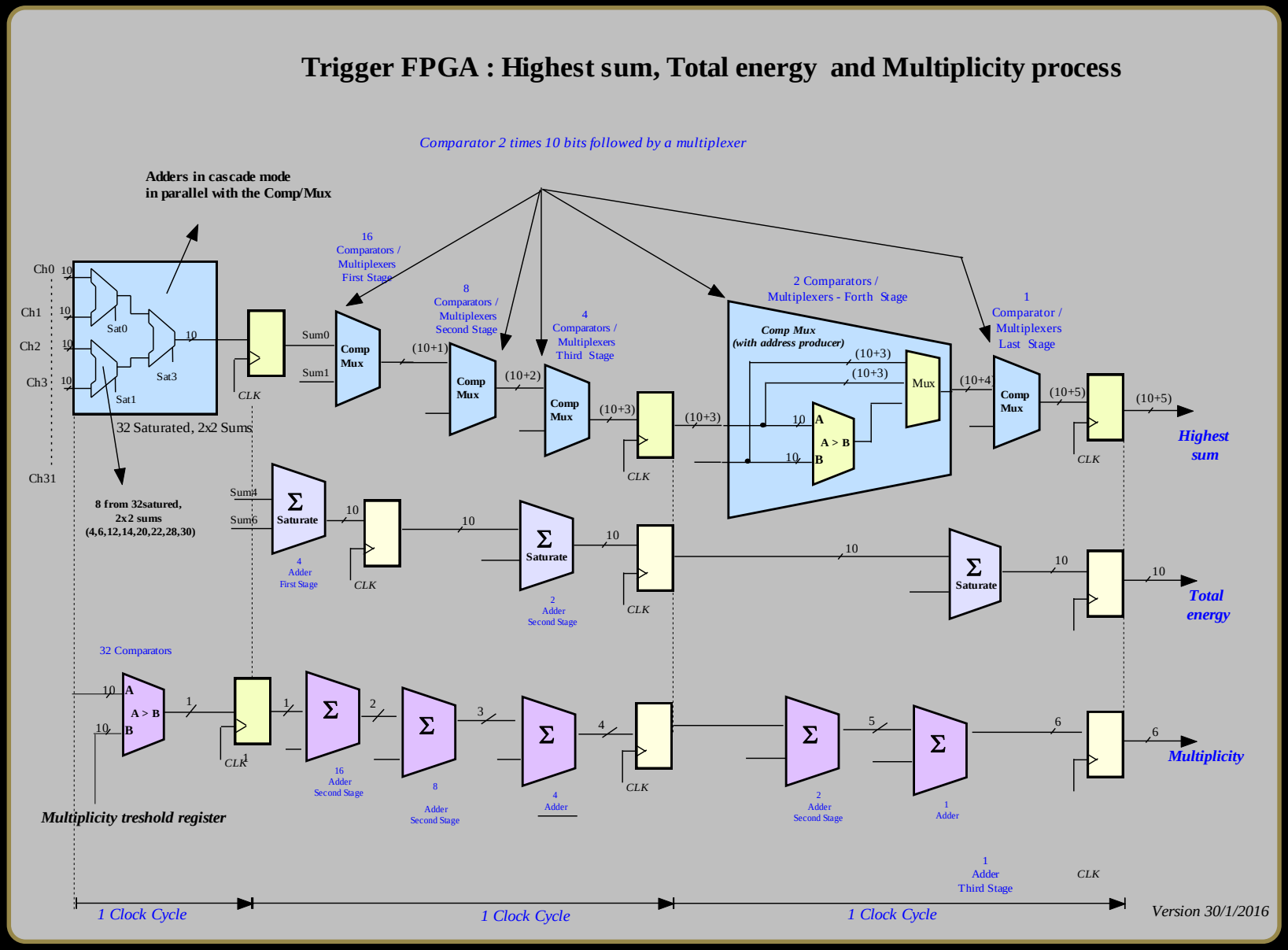


Trig_Seq FPGA

- Handles the Trigger processing and the control of the board.
- Embeds an USB2 interface. The FTDI chip is deported on the FT232h card for cost and radiation reasons.
- I2C and SPI masters are driven by the USB . These 2 bus are used to communicate with all the components.
- FIFOs monitor the complete Trigger data which are calculated and transmitted to the GBTx .
- Receives the fast commands from the 3CU and distributes it to the Fe FPGA.
- Compares the 4 Fe FPGA BXID synch signals with the local counter



Low level Trigger : calculation



Data format

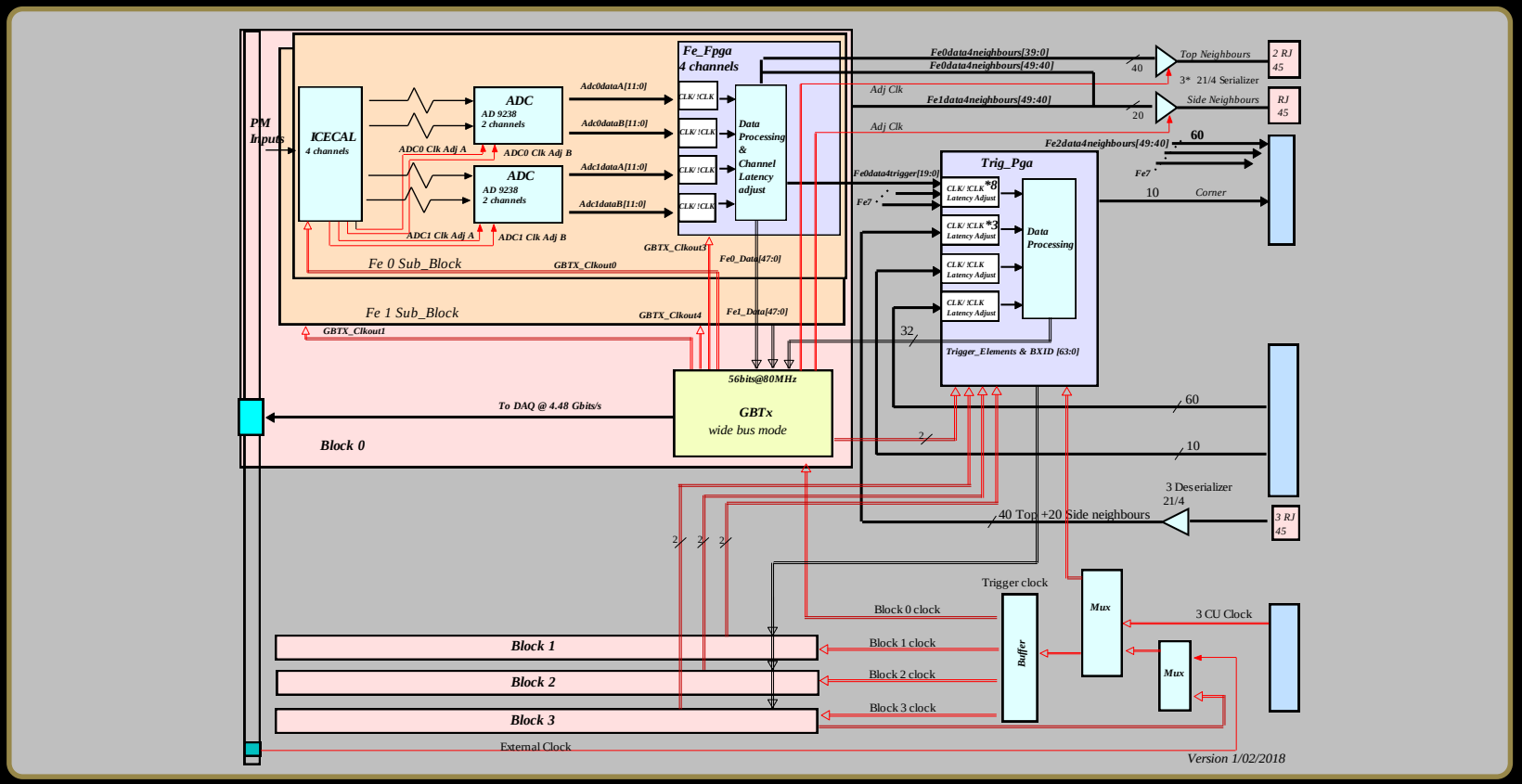
- Each Feb block encodes 8 channels -> 8 x 12 = 96 bits -> 4 x 96 bits for the whole board.
- LLT generate 32 bits which are split and transmitted together with the Fe data on the 4 fibers.
- We are using the GBTx in the wide bus mode offering a bandwidth of 112 bits @ 40 MHz .
- The 96 + 8 bits are completed with the BXID duplicated on the 4 fibers .

Fibre	BX identification	LLT data		Data channels							
0	BX< 7..0 >	E_T^{Total} < 7...0 >		0	1	2	3	4	5	6	7
1	BX< 7..0 >	Addr(E_T^{Max}) < 4...0 >	E_T^{Total} < 10...8 >	8	9	10	11	12	13	14	15
2	BX< 7..0 >	E_T^{Max} < 7...0 >		16	17	18	19	20	21	22	23
3	BX< 7..0 >	Multiplicity < 5...0 >	E_T^{Max} < 9..8 >	24	25	26	27	28	29	30	31

Table 2: Data format of the calorimeter electronics readout.

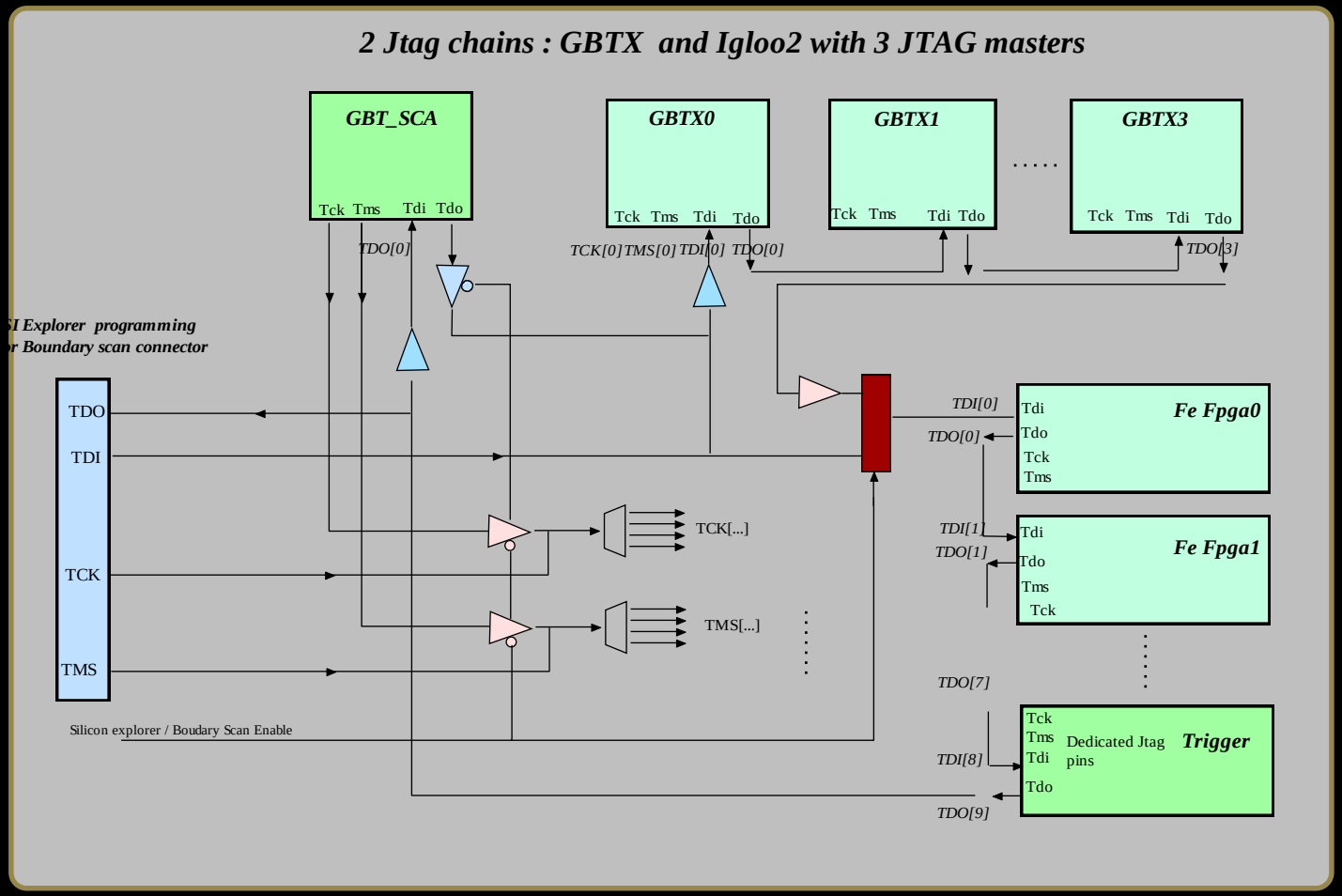
Feb - Clock synopsis

- The architecture of the board leads to a complex system for the Clock tree
- The challenge is to insure a proper setup taking into account various constraints
  - All the channels have to be in the same bunch crossing at the board and crate level and over the whole calorimeter
  - All the data coming from different chips have to be correctly phased at the input of each GBT
    - Detail strategy for commissioning have been already developed taking benefit or our experience on the previous design.

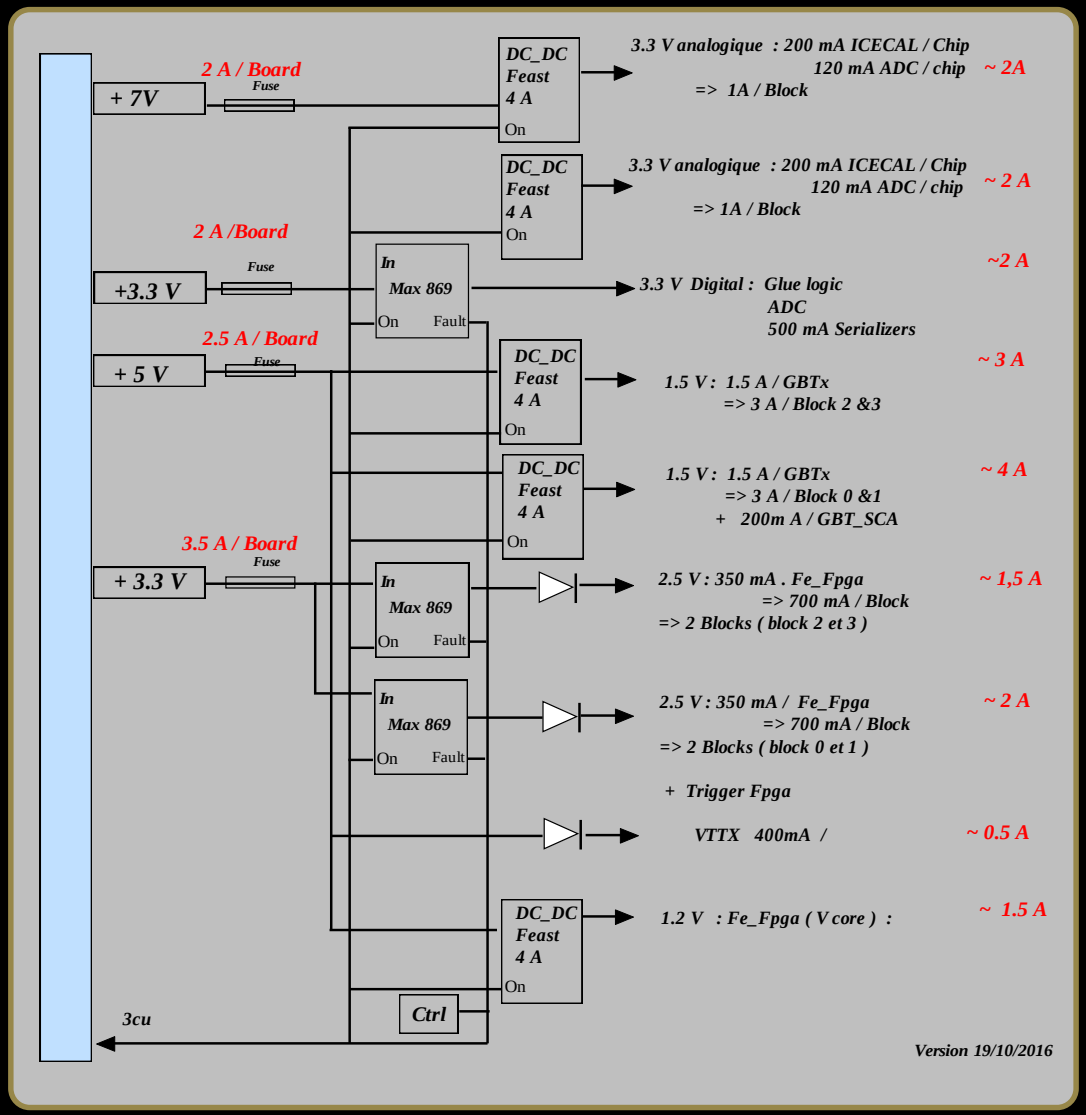


JTAG chain and GBTx configuration

- One JTAG chain for programming operation in parallel with dedicated SPI (Microsemi programmer)
- JTAG chain can be extended to include the 4 GBTX for boundary scan (production)
- JTAG chain can be driven by the Microsemi programmer or the GBT SCA or the tester.
- GBTx can be fused by a dedicated distributed power line and power pulse driven by the Trig_Seq .



Feb - Power distribution and Power budget



- Consumption of the FPGAs depends on the occupancy roughly estimate
- Electronics is protected against latchup by the FEAST and the Max869 which control the over current.
- Over current generate a alert to the 3CU
- The signal permits to switch off the board and remotely control the power on and off if a power on sequence is required.
- The 3U backplane is reused without modifications. Pins are just reattributed depending on the consumption : +7V in place of +5V. *Contact with V Bobilier*

Feb :Test status

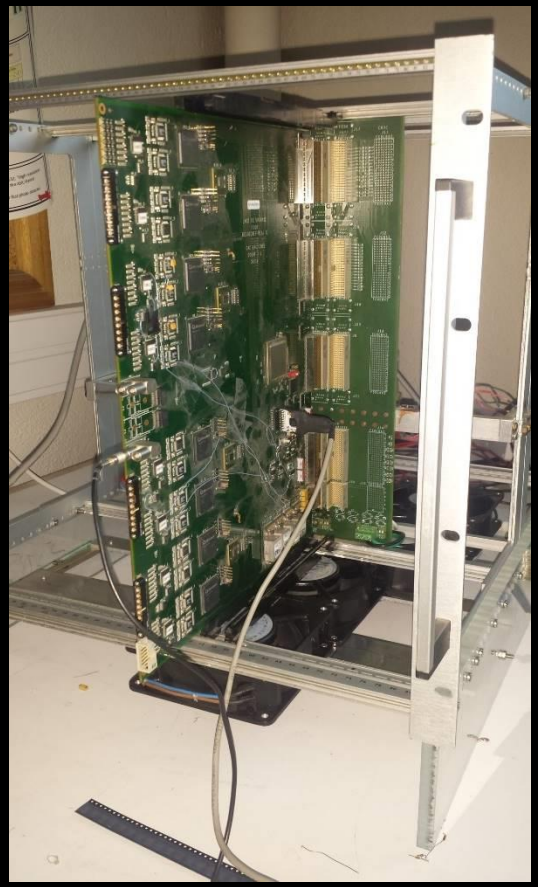
We test a large part of the Feb :

- The analog and data processing was tested and characterized with the help of Edu and Joao (See next talk)
- The down stream link with the DAQ was tested with Monique (see nex talk)

- The control of the Feb using the VLDB board to control the GBTSCA of the Feb was successfully done.
  - Some bugs with the SPI protocol between the master GBTSCA and the FPGA slave still have to be fixed(FPGA firmware)

- Test performed with injection patterns and cross checked with the software tools using in WINCC for Fe data and trigger data.

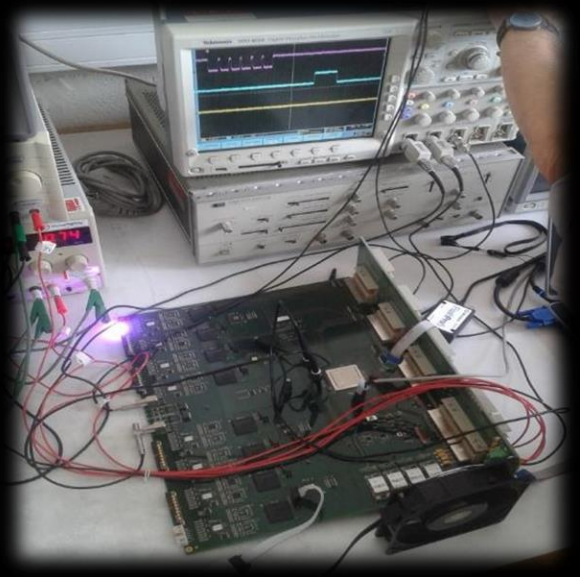
- Feb was plugged in the special crate/backplane which is a shrinked version of the calorimeter crate. It is dedicated to debug 2 cards (connection of the neighbours) connected with the 3CU distributing TTC.



Feb :Test status

Find some bugs on the actual prototype :

- ADC Vref not properly decoupled.
- Ground plane underneath the ICECAL missing
- Inversion of polarity at the ADC inputs on some channels
- Reset of the ICECAL : invertion of the polarity
- SPI connexion missing on block 3
- DC level adjustment between GBTX ADC-DAC and ICECAL Vcontrol-V coarse



Find some modifications to implement :

- Consumption higher than expected on the analog 3.3 V
  -> need an extra FEAST
- More latitude for timing adjustment in TrigSeq
  -> 8 adjustable clocks available
- Implementation of the USB connector on front panel
- Set the 2.5 to 3.3V on the backplane for compatibility with the LEDTSB.
- Zener diode to generate the 2.5 V. Solution for the MAX869 which are powered under their specs

Feb :Test status

Test still to be done or presently on study :

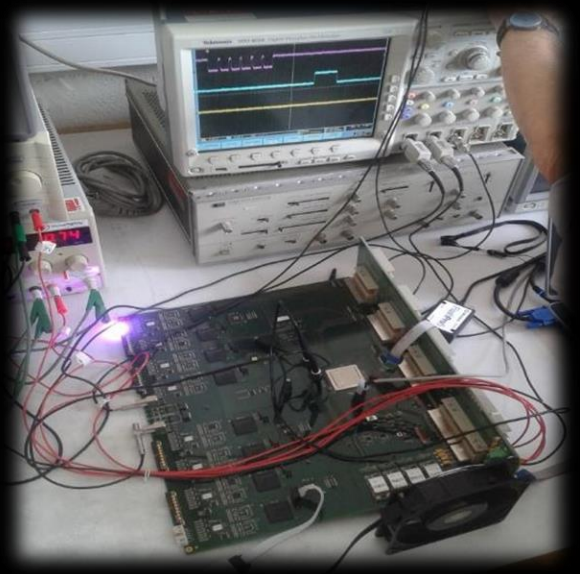
- Trigger
  - processing : firmware
  - interconnexion : hardware @ board level
  - combined test with 2 boards: software developpments

- Fuse of the GBTX (depends on the strategy @ the power up)

- FPGA programmation via JTAG/GBTSCA

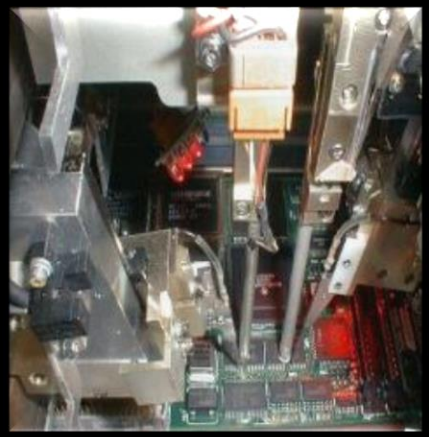
- Latchup control by the FEAST not properly set

- Combined test with the 3CU



Feb production

- We will start the market survey of the boards middle of 2018 depending on the spending profile.
  Estimate cost : ~1300 €/ board / 300 CERN components and connectors not included.
- Two prototypes are presently manufactured by the company.
- We will order the FPGA soon with Cern
- We will keep the same process we used for the production in 2006
- Production of 3 batch
- Aging by bunches of 16 boards powered in a dedicated crate with a standard industrial profile for the detection of badly soldered components and bad components.
- Boundary Scan with the JTAG is implemented and could be used after the production to help to debug the broken boards.
- “Takaya” test for checking :
  - Impedance values and interconnections
  - Badly soldered chips with “open checker”.
- Preliminary functionnal test done on 8 boards @ the manufacturer



Feb production schedule

- Two prototypes will be available by the end of February
- Tests and characterization will continue up to end of 2018 with priority given to the hardware, using mostly injection patterns. Firmware is also developped in parallel.
- Market survey will start first half of 2018. The process is driven by the CNRS.
- Tendering second half of 2018. (Cost will not be the only criteria to consider)
- First 16 boards by the end of 2018
  - Tests followed by the production
- Test of the production
- Installation and commissioning from mid 2019 beginning by the modification of the Crates.