Calorimeter Upgrade: Analog Electronics

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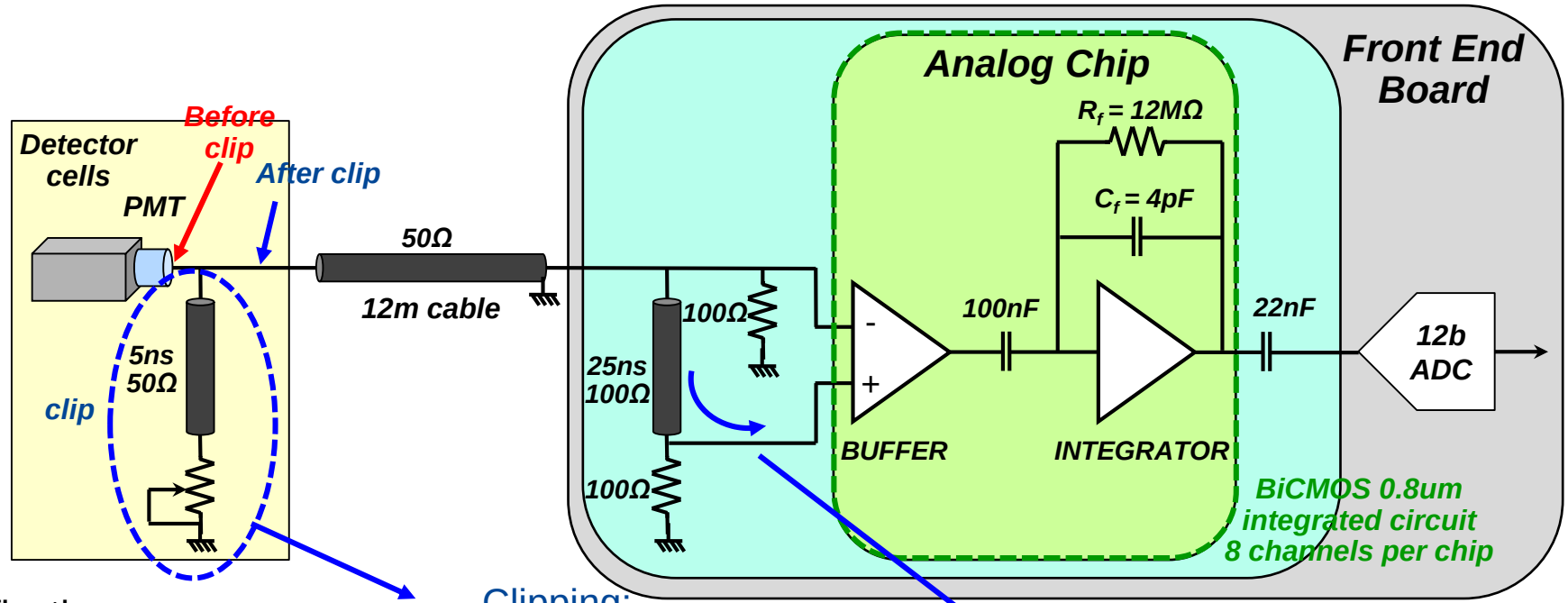
Institute of Cosmos Sciences

Outline

I. **Calorimeter upgrade: analog electronics**
II. System design
III. Digital building blocks
IV. Tests
V. Production

I. Current Analog Signal Processing



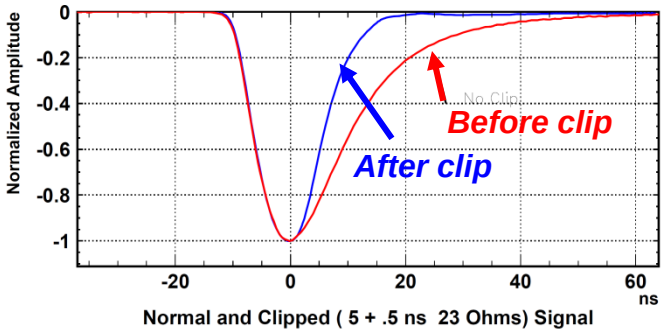
Specifications:

- Pulse shaping in 25ns
- Spill over (signal residue) < 1% after 25ns
- Integrator plateau: 4ns
- Linearity < 1%
- Rise time ~ 5 ns

Clipping:

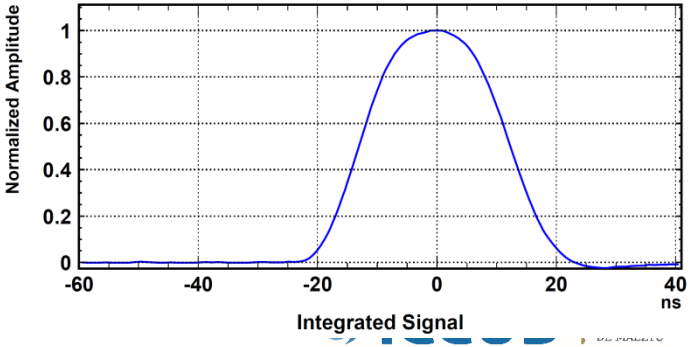
⇒ Reduce signal tail

⇒ Reduce spill over

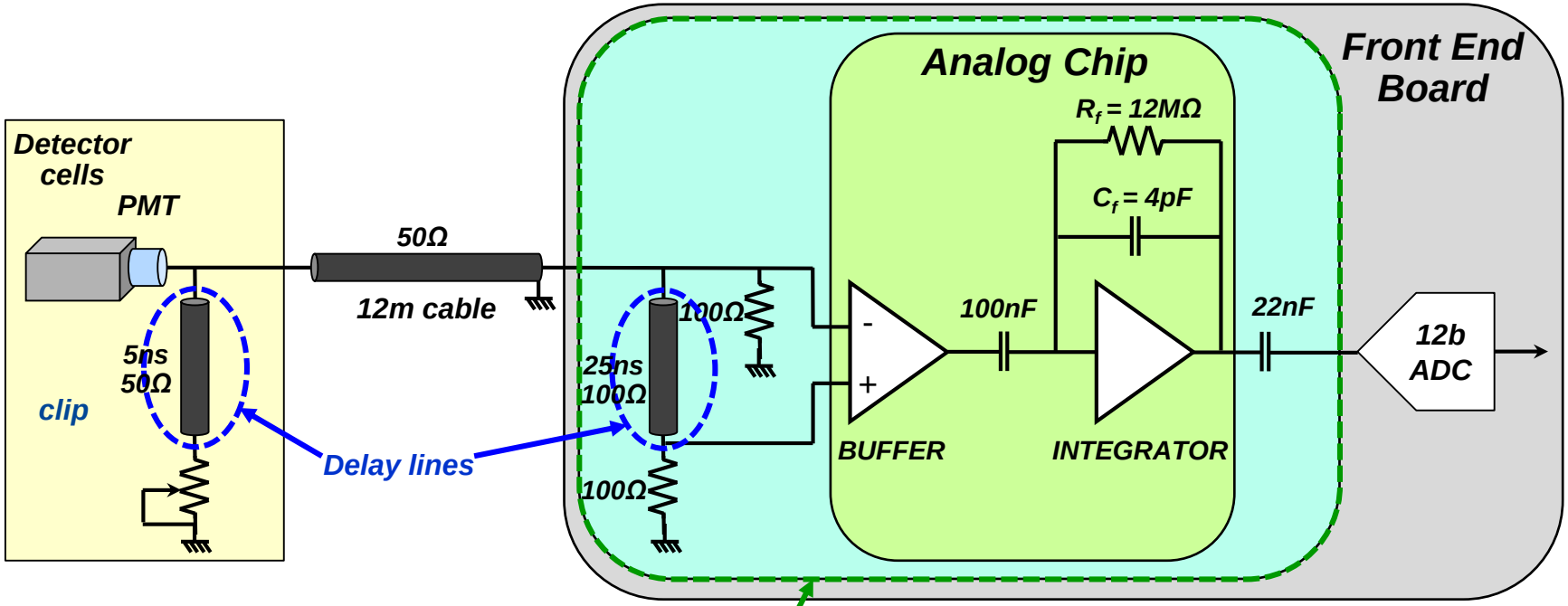


Integrator discharge:

Clipped signal + delayed negative clipped signal



I. Analog Electronics Upgrade Motivation



PMT current has to be reduced to increase lifetime

⇒ **FE electronics gain has to be increased correspondingly**

– **BUT FE noise should not be increased in the operation!**

Proposed solution:

– New ASIC
  - ✓ Increased gain
  - ✓ Reduced noise
  - ✓ Integration / shaping

Radiation tolerance:

– Dose 100 rad per fb^{-1}

✓ Radiation qualification tests

✓ Design techniques on ASIC

→ Enclosed transistors with guard rings

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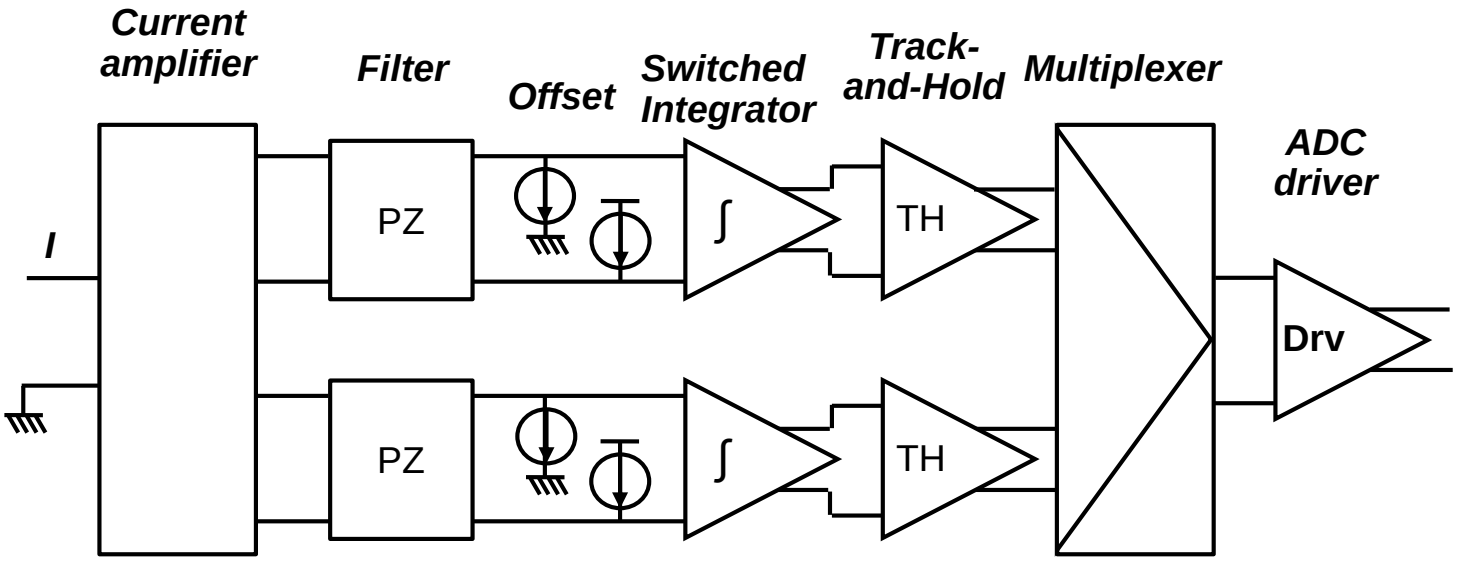
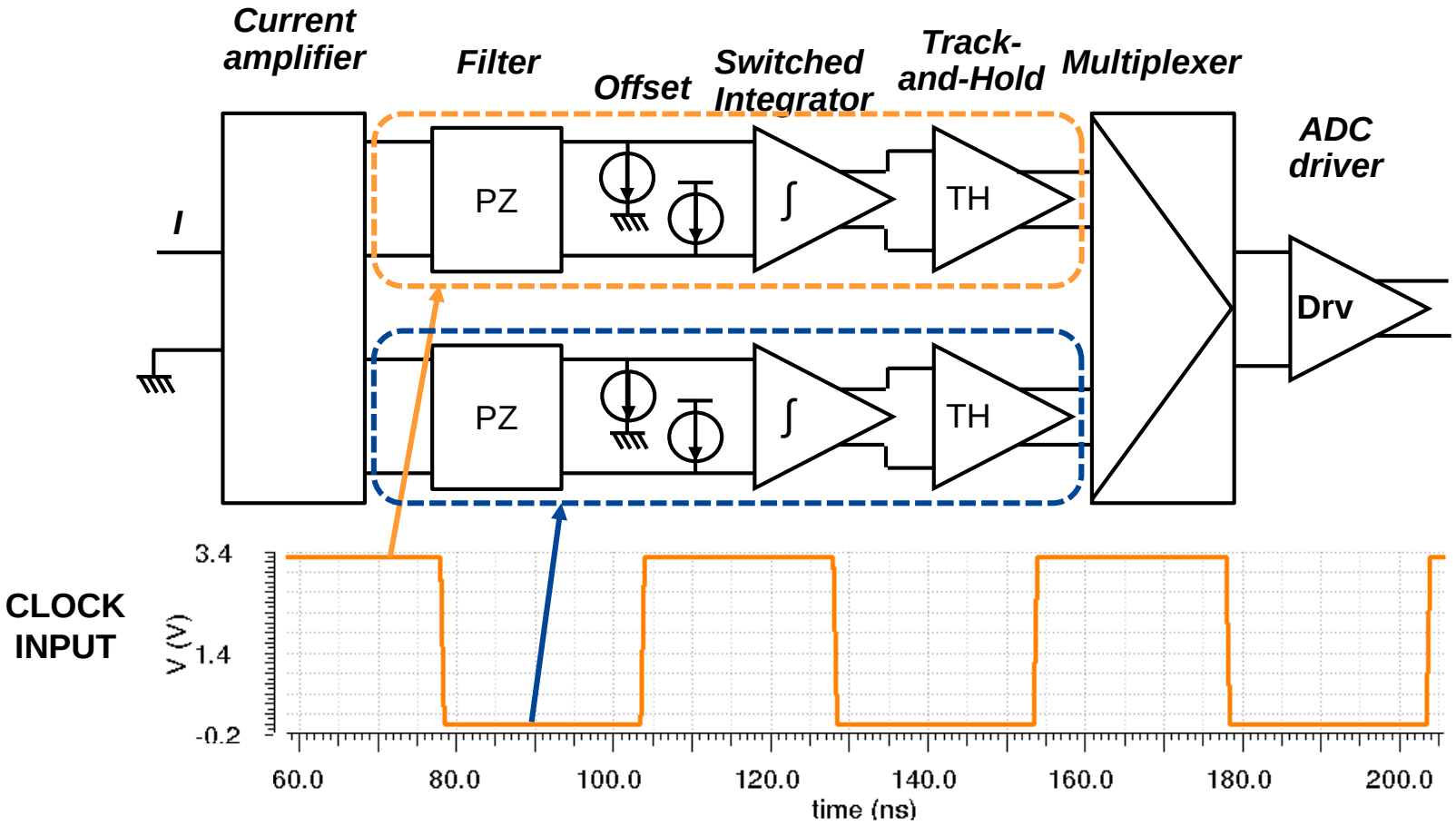
II. System design: channel architecture

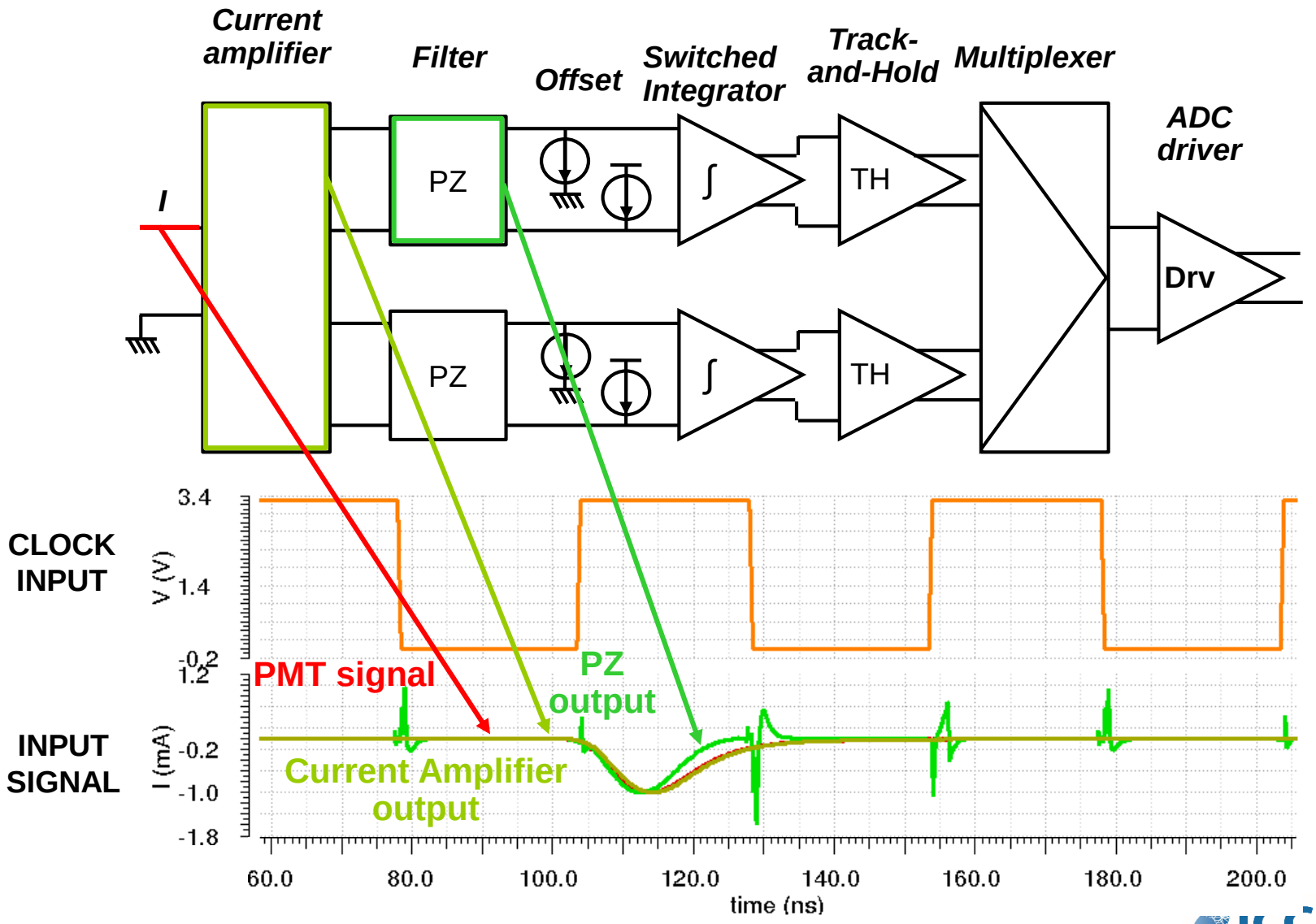


Very difficult to integrate HQ analog delay lines → ***2 switched alternated paths*** → ***Switching noise*** → ***Fully differential ASAP***

II. System design: channel architecture



II. System design: channel architecture



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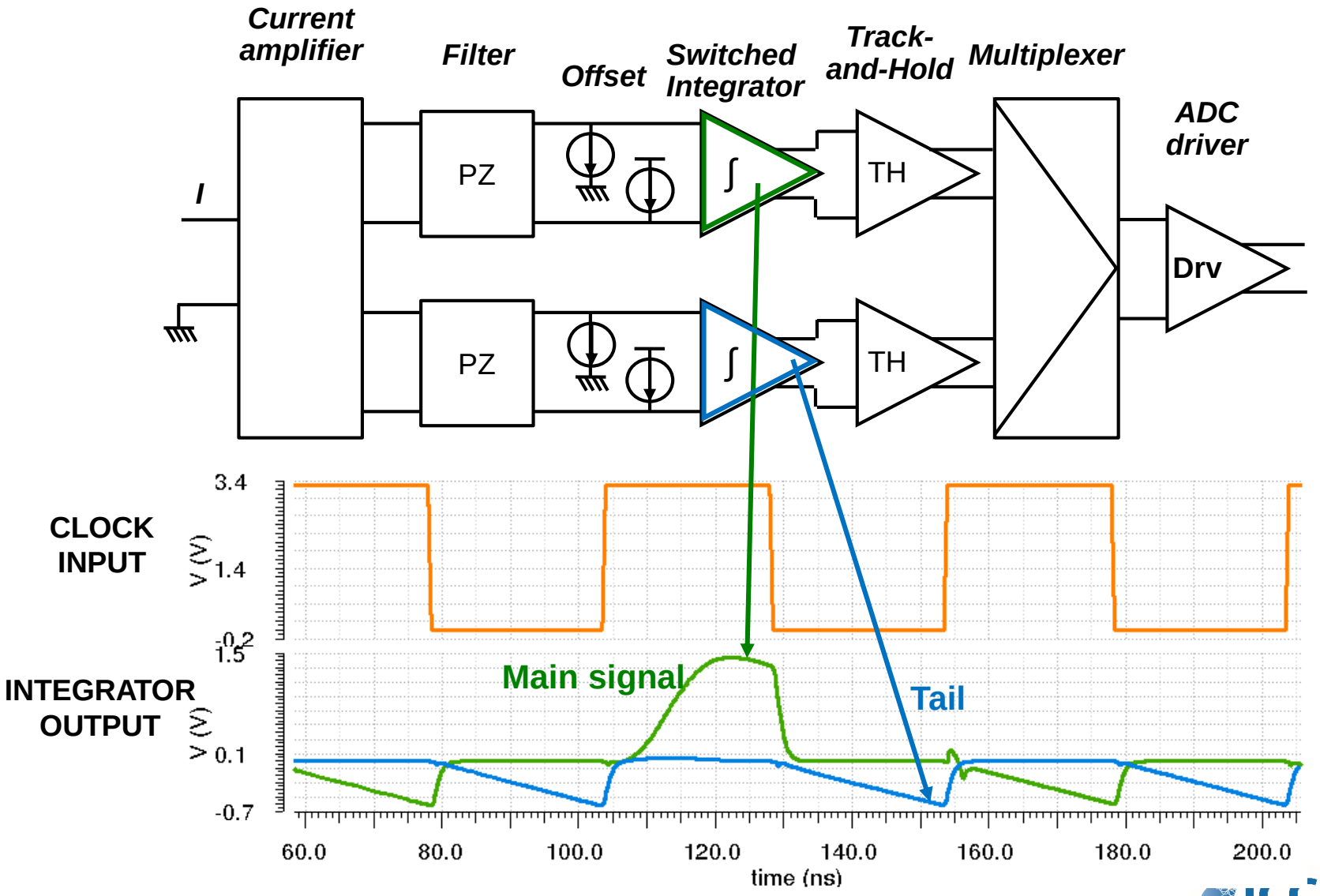

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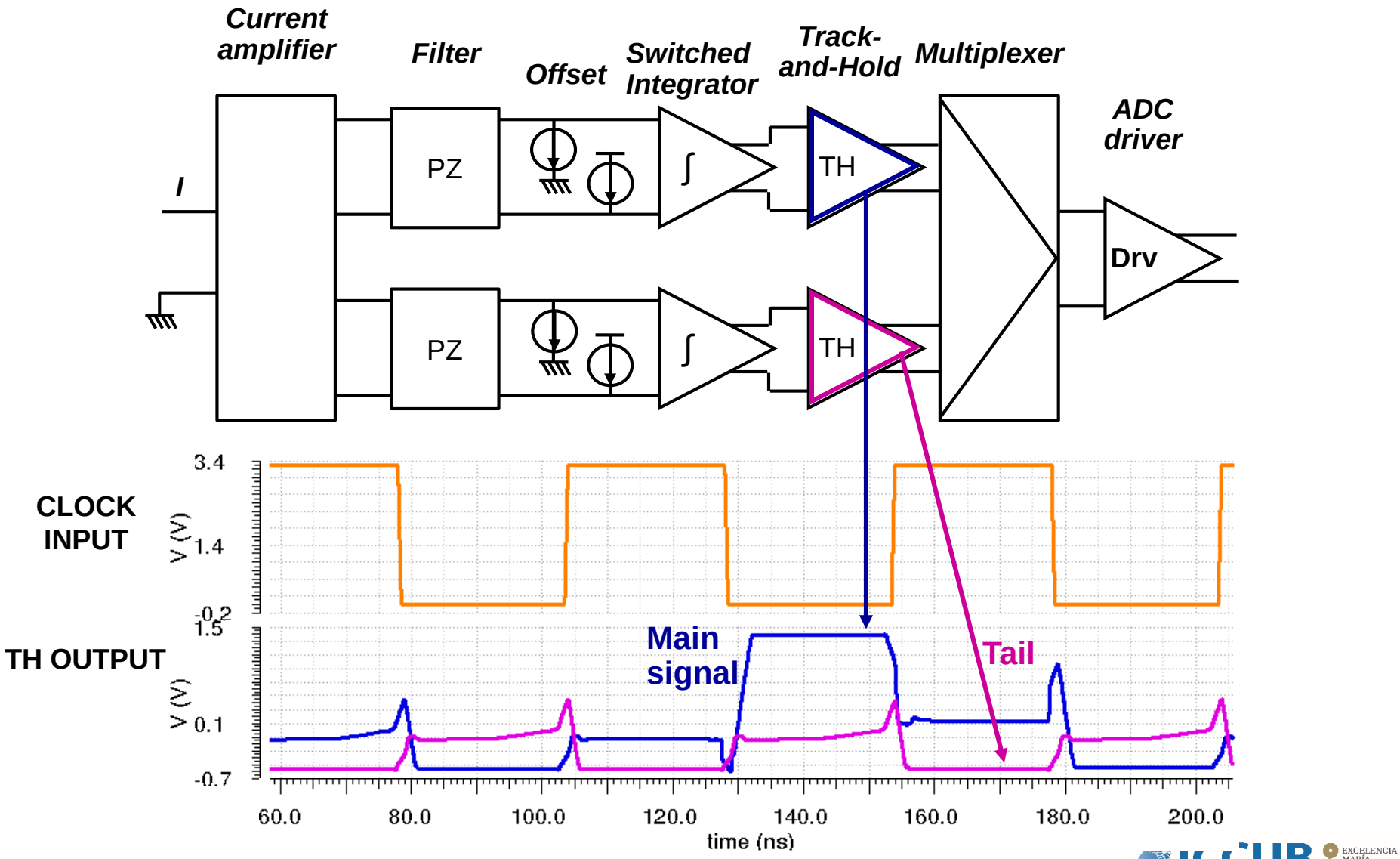

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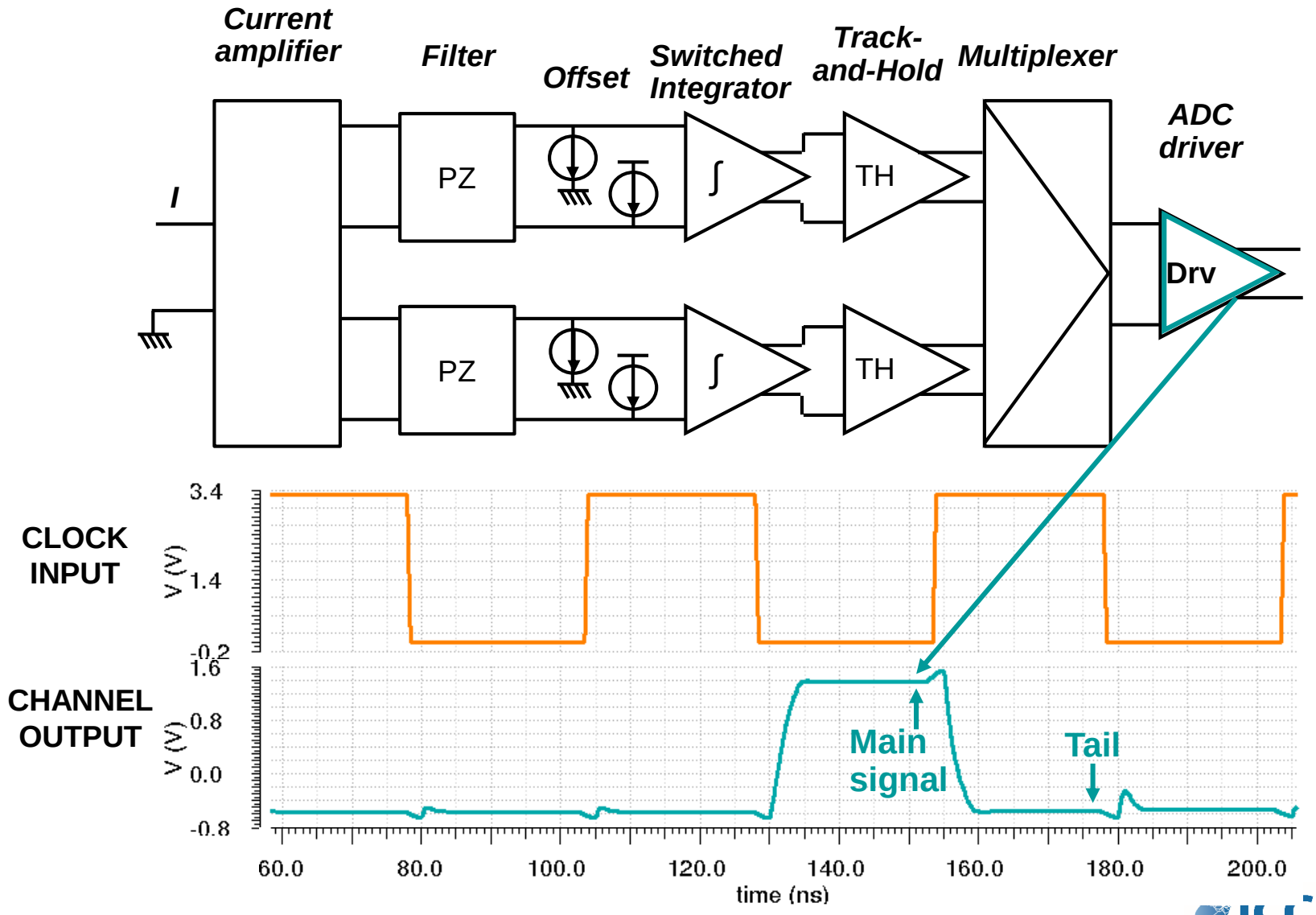
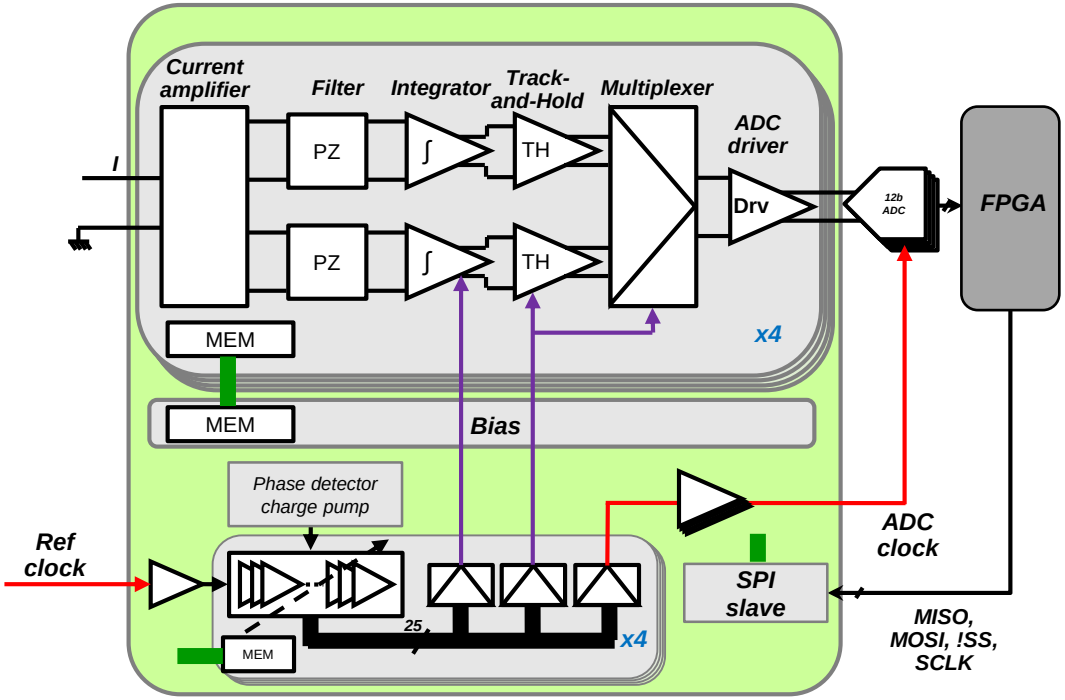
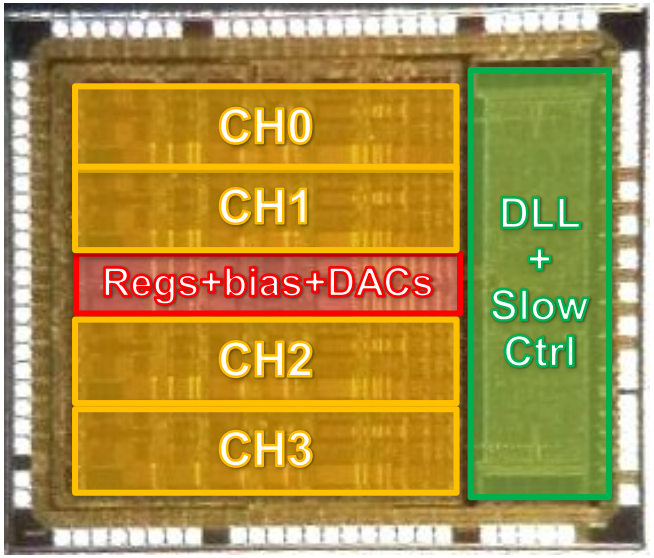


II. ICECAL ASIC



- Analog channel:
  - Very difficult to integrate HQ analog delay lines
  - 2 switched alternated paths
    → no dead time between consecutive events
  - Switching noise → fully differential ASAP
  - Input impedance control by current feedback
    → Low noise performance

- Complete 4 analog channels
- Tunable parameters
- 4 DLL for synchronization
- 2 versions with gain:
  - 4.5 fC/LSB
  - 9.0 fC/LSB



SiGe BiCMOS 0.35um
AMS 10.5 mm^2

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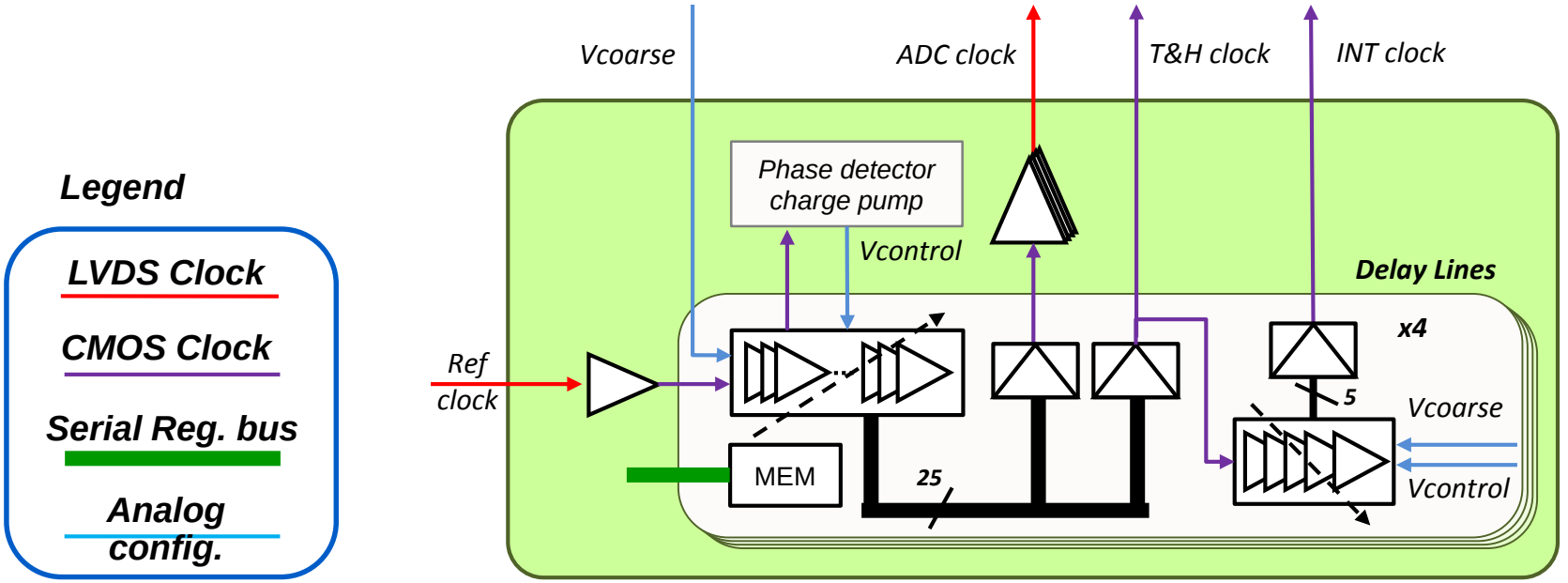
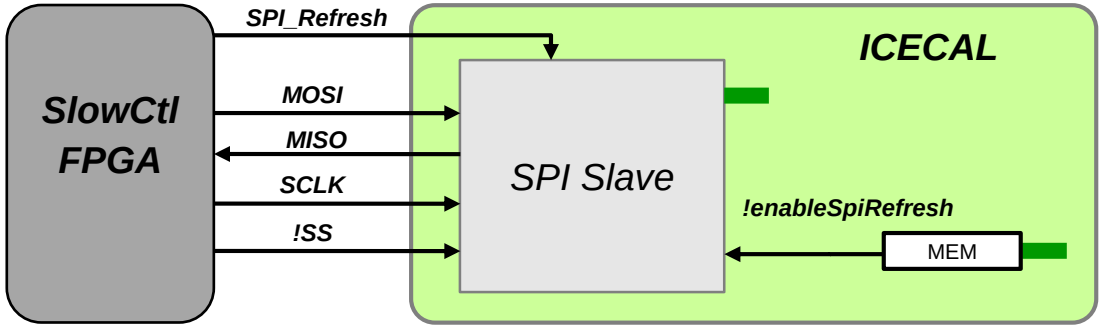
III. Digital building blocks: DLL

- Clock management is internally done by the ICECAL Chip:
  - Three clock phases are generated from an input reference (REF_CLK):
    - Track & Hold clock phase (Φ_{TH}). F_{CLK} = 20 MHz.
    - Integrator clock phase ($\Phi_{INT} = \Phi_{TH} + \Delta\Phi_{INT}$). F_{CLK} = 20 MHz.
    - ADC clock phase (Φ_{ADC}). F_{CLK} = 40 MHz.

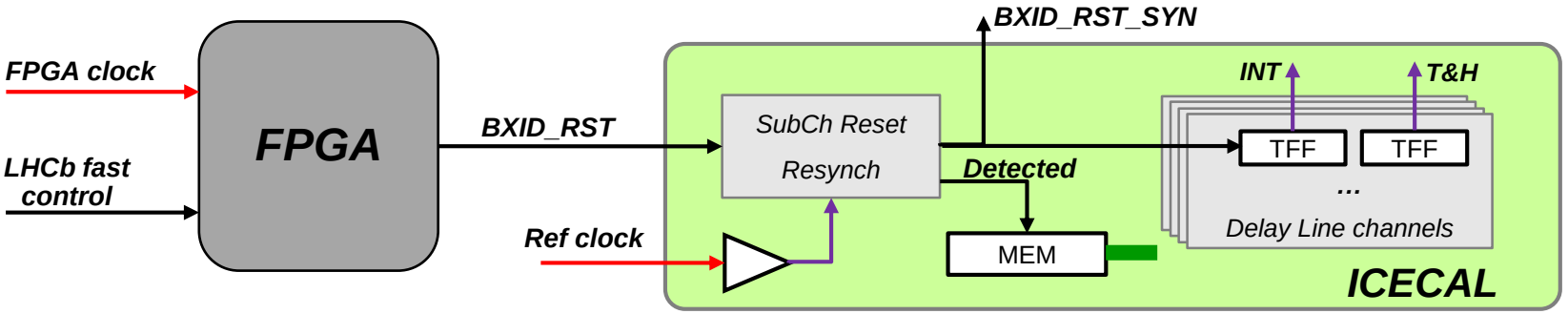


III. Digital building blocks: slow and fast controls

- Access to internal registers to configure the chip:
  - Analog channel parameters
  - DLL
  - SPI Slave



- Analog sub-channel reset circuit:
  - FPGA needs to know the analog sub-channel source of the ADC reading Gain & Offset compensations.
  - The first sub-channel is always the same for each configuration



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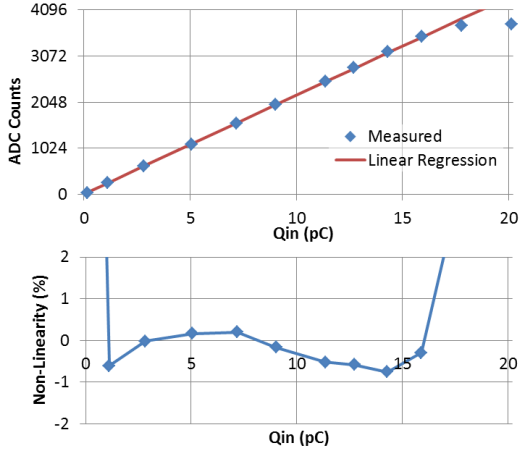
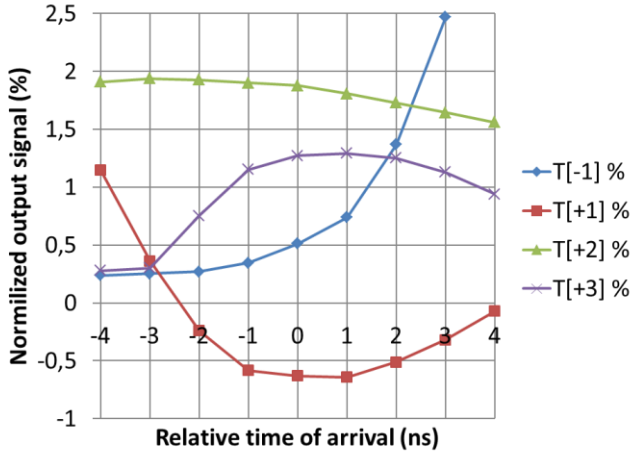
II. ICECAL ASIC: tests results

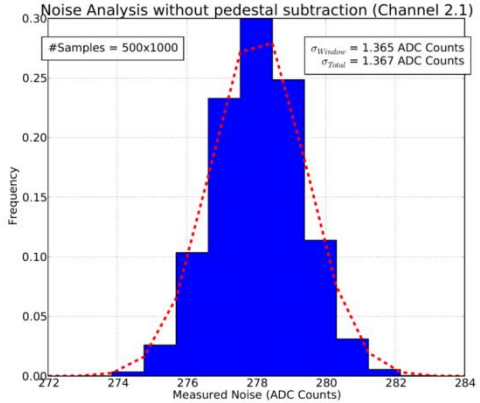
- Tests at lab and test beams:
  - Linearity



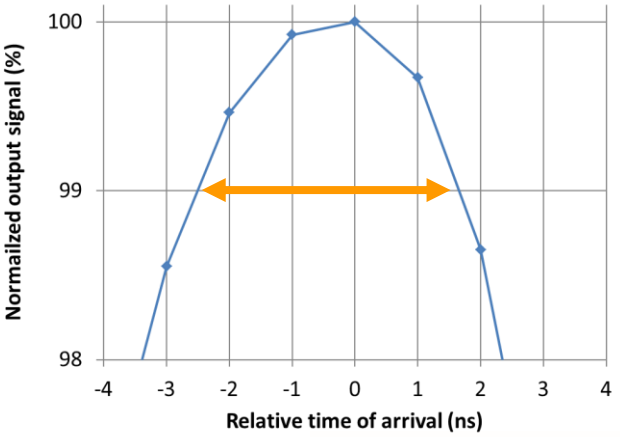
  - Spill over



  - Noise



  - Plateau



II. ICECAL ASIC: radiation hardness tests

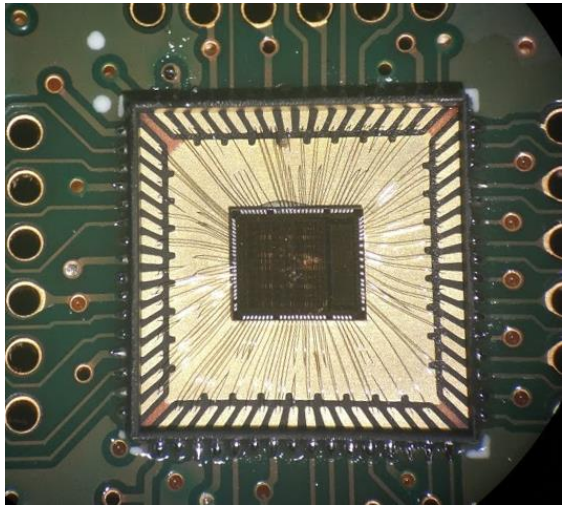
At CRC (UCL) in Louvain-la-Neuve (Belgium)

TID tests:

- Use beam of 61 MeV protons
- Dose up to 55 krad on 4 chips
- Results:
  - No SEU or SEL was detected
  - No relevant variation on the chips characteristics

SEE tests:

- Irradiate with heavy ions: 58Ni+18
  - LET = 20.4 MeV/mg/cm2
- Two chips were irradiated:
  - No SEU detected
- Use refresh signal
- Equivalent expected limits for all channels in detector lifetime:
  - 1.3 SEU
  - 0.9 SEL



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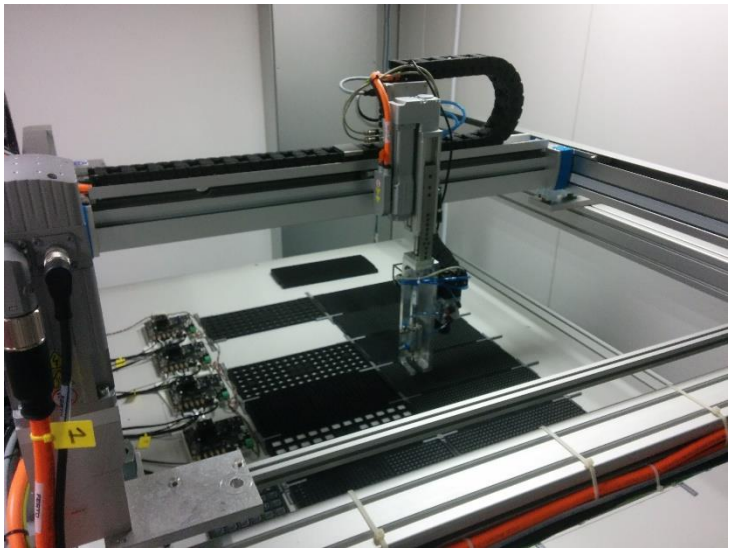
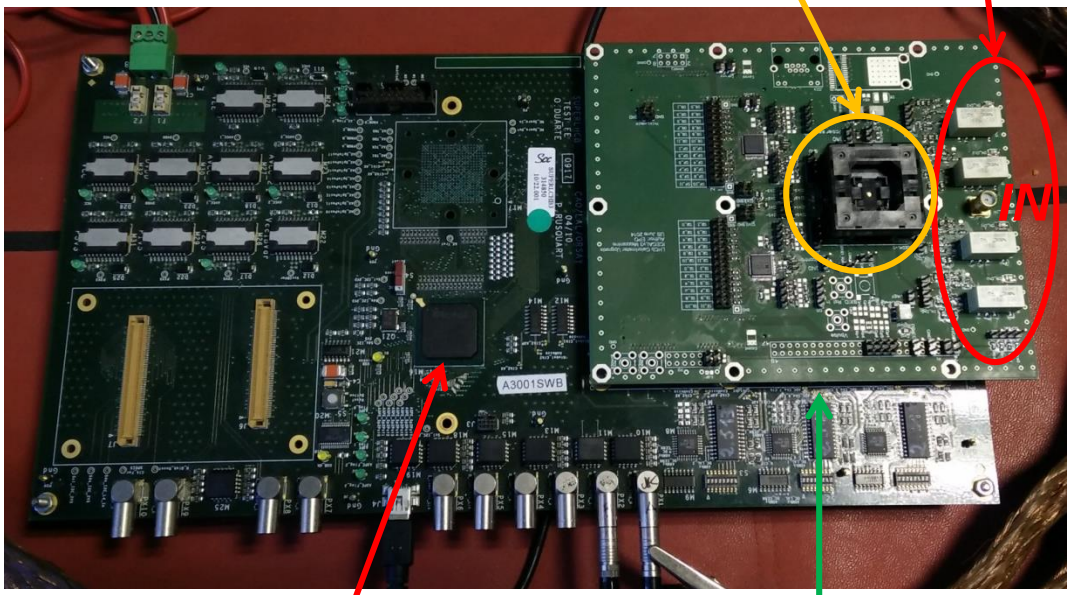
Robotic system



- Motorized horizontal gantry system to move the chips from tray to the test PCB and to final tray.
- Motorized stage in the vertical direction.
- Pneumatic suction.
- Pressure sensor.

FEB prototype (4 data channels)



V. Status

- Production
  - Standard version (v3.1): 3050 pieces
  - Reduced gain (v3.2): 3050 pieces

- Production test
  - Mezzanine: ready
  - SW:
    - Test defined: rejection limits are being prepared
  - Robotic setup ready in ~2 weeks
  - Estimated total test time: 2-3 months

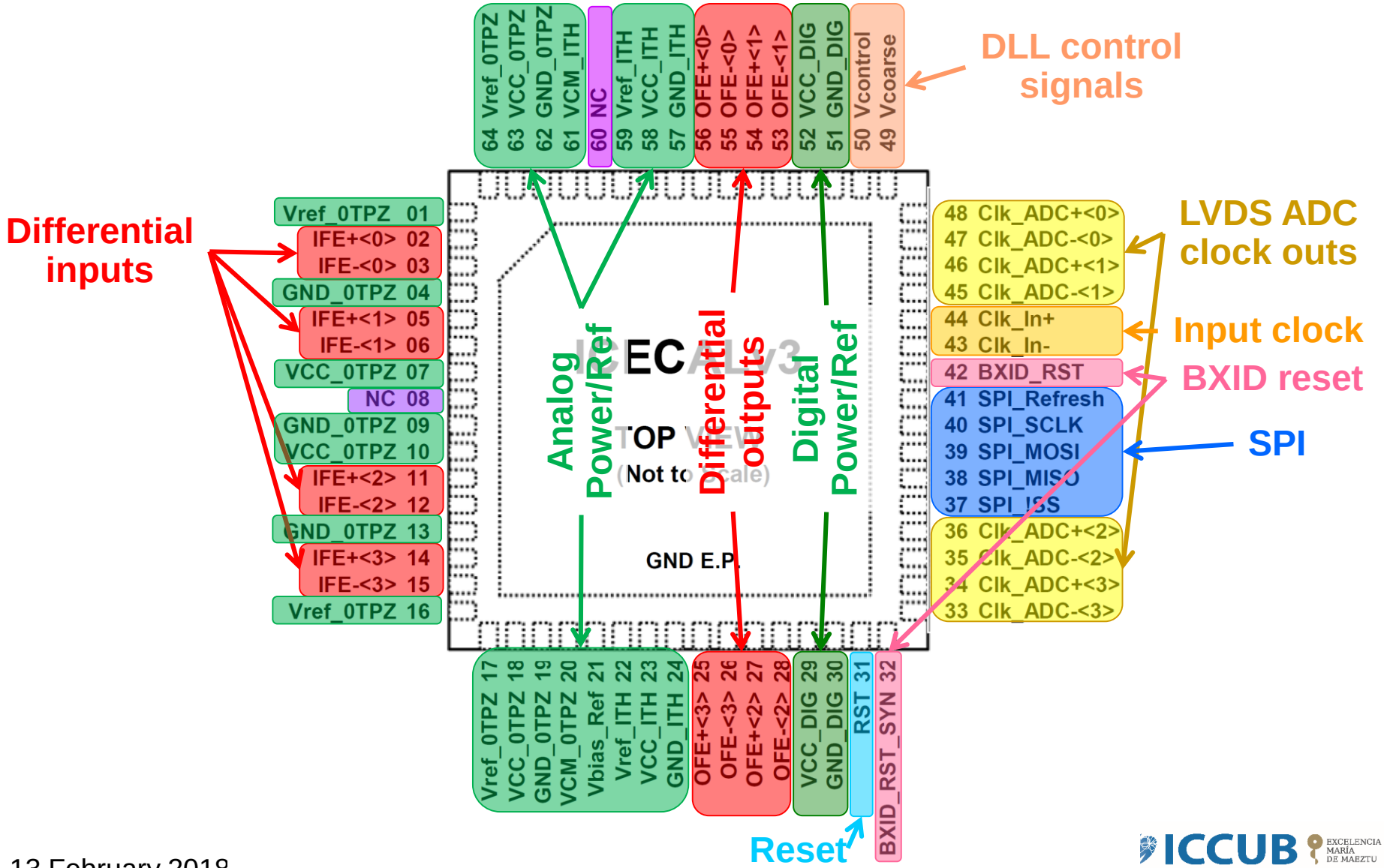
Backup

II. System design: Analog Electronics Specifications

- PMT current has to be reduced by factor ~ 5 to increase their lifetime:
  - FE electronics gain has to be increased correspondingly
  - FE input equiv. noise should still be ~ 1 LSB
- New ASIC:
  - Increased gain
  - Reduced noise
  - Integration / shaping
- New front end board is required:
  - Low noise analog electronics
  - Data transmission @ 40MHz

Energy range	**0-10 GeV/c (ECAL) Transverse energy**
Calibration	**4.5 fC / 2.5 MeV / LSB**
Dynamic Range	**4096-256 = 3840 : 12 bit**
Noise	**<≈ 1 LSB or ENC < 4 fC**
Termination	**50 ± 5 Ω**
Shaping	**25 ns (99% of the charge)**
Baseline shift prevention	**Dynamic pedestal subtraction (CDS)** **Pedestal is the smallest of 2 prev. Samples**
Max. Peak current	**4 - 5 mA (clipped)**
Spill-over residue level	**±1%**
Linearity	**< 1%**
Crosstalk	**< 0.5%**
Timing	**Individual (per channel)**

III. ICECAL pinout



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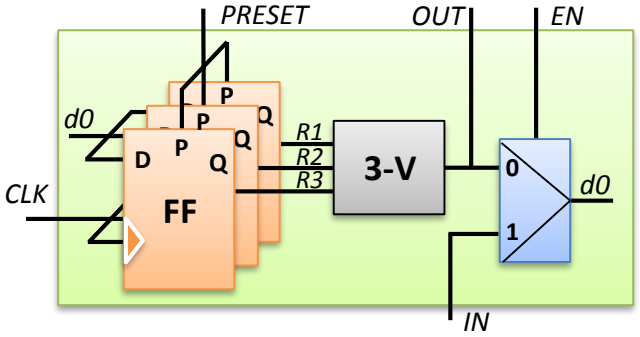
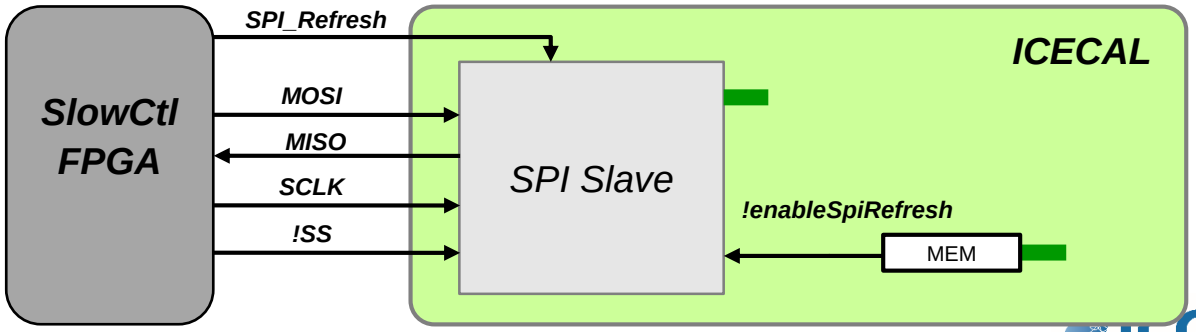
III. SPI refresh

- 16-bit TMR registers:
  - Each bit is stored in 3 flip-flops.
  - Majority is computed.
  - SEUs are automatically corrected.
    - Problem: correction is done as long as SPI clock is active.
    - Solution: SPI refresh signal.

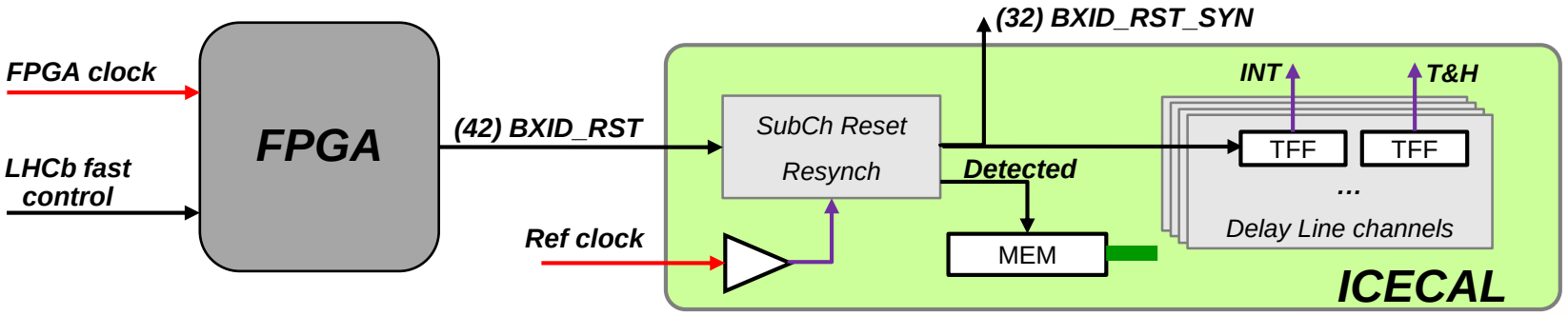


- SPI refresh signal:
  - An auxiliary clock is provided.
  - Only enabled when SPI slave is idle.
  - Is optional: can be disabled by software.



III. Fast control: BXID reset

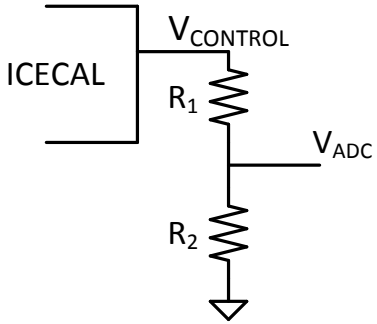
- Analog sub-channel reset circuit:
  - An ASIC channel consists in two sub-channels.
  - FPGA needs to know the analog sub-channel source of the ADC reading:
    - Gain & Offset compensations.
- **How it works:**
  - FPGA generates 1-cycle width synchronous reset pulse.
  - ICECAL resynchronizes this reset with its input clock.
    - Metastable phases (FPGA→ASIC) are discarded.
    - Debug signals:
      - + External pad: 32-BXID_RST_SYN
      - + Slow control bit (Detected)
  - Integrator and T&H clocks levels are preset (clock phases remain unchanged).
  - The first sub-channel is always the same for each configuration



III. Internal delay

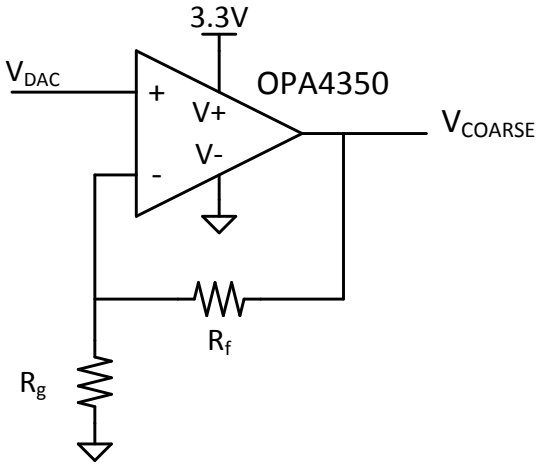
- Proposed circuits between ICECAL and GBT-SCA

DLL $V_{control}$ out



- It is recommended to use a voltage divider to read the DLL $V_{CONTROL}$ and adapt the voltage range to the ADC input.

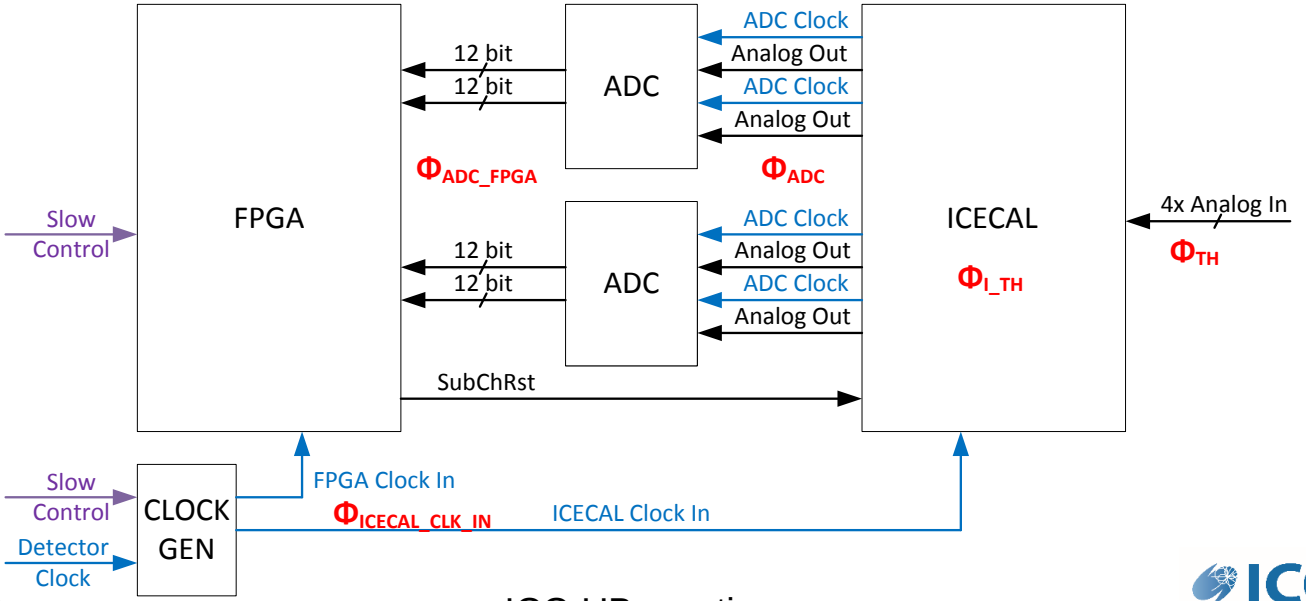
DLL V_{COARSE} input generation



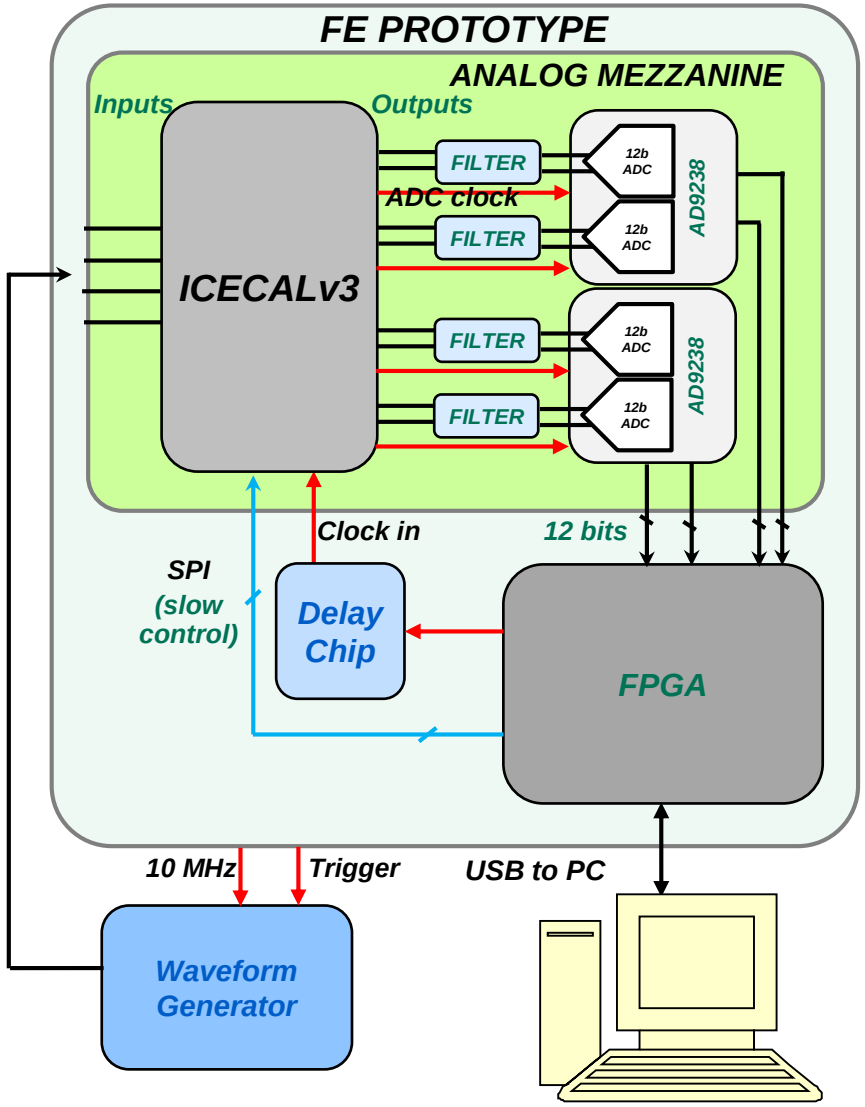
- The input VCOARSE voltage has to be controlled by a DAC.
  - Its expected value is 1.2V
  - Range: from 0.5V to 2V.

III. Time alignment

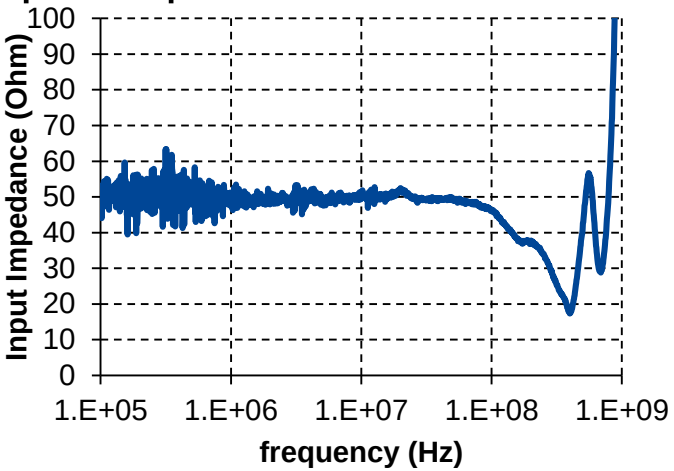
- Synchronization method:
  1. $\Phi_{ICECAL\_CLK\_IN}$: look for the most stable phase for which the sub-channel reset is performed (fixed for each PCB).
  2. Φ_{I_TH}: delay between the integration time and the Track-and-Hold clocks (internal delays of the chip, optimal = 1ns).
  3. Φ_{TH}: detector channel optimal integration time (particle time arrival, PM HV, signal cable length). Look for the maximum signal and minimum spill over.
  4. Φ_{ADC}: time at which the ADC performs the conversion (fixed for each PCB).
  5. Φ_{ADC_FPGA}: the ADC 12 bits of data have to be captured by the FPGA in parallel at the right phase or there will be data corruption. Use rising or falling edge of the FPGA clock (fixed for each PCB).



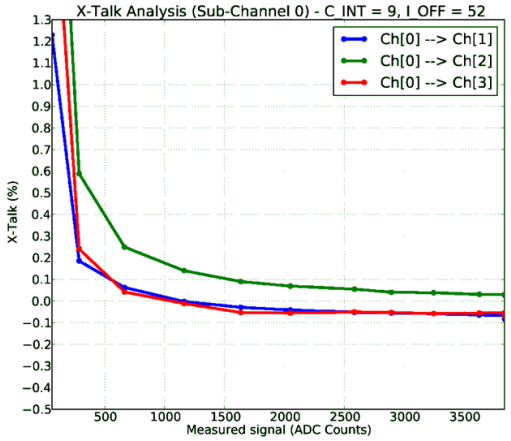
III. Calorimeter Upgrade: ICECALv3



- Tests at lab:
  - Input impedance



  - Crosstalk



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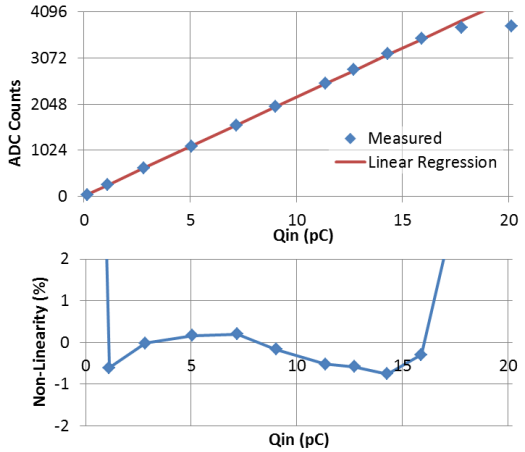
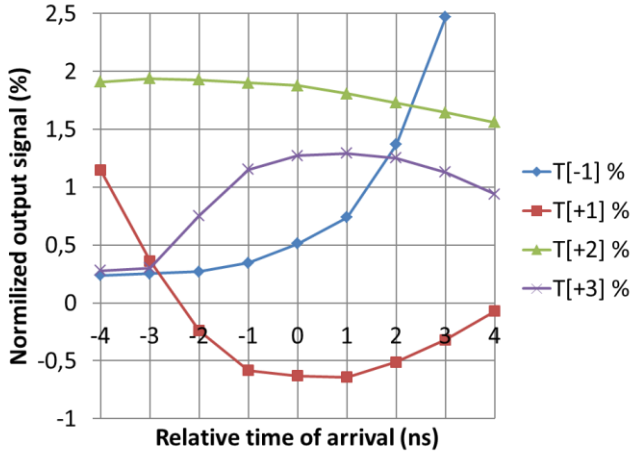
III. Calorimeter Upgrade: ICECALv3

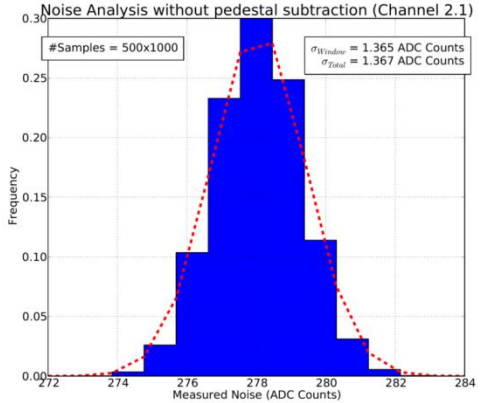
- Tests at lab:
  - Linearity



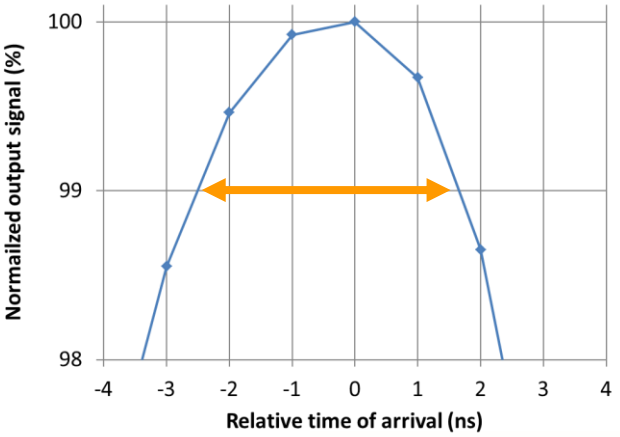
  - Spill over



  - Noise



  - Plateau



II. ICECAL ASIC: tests results

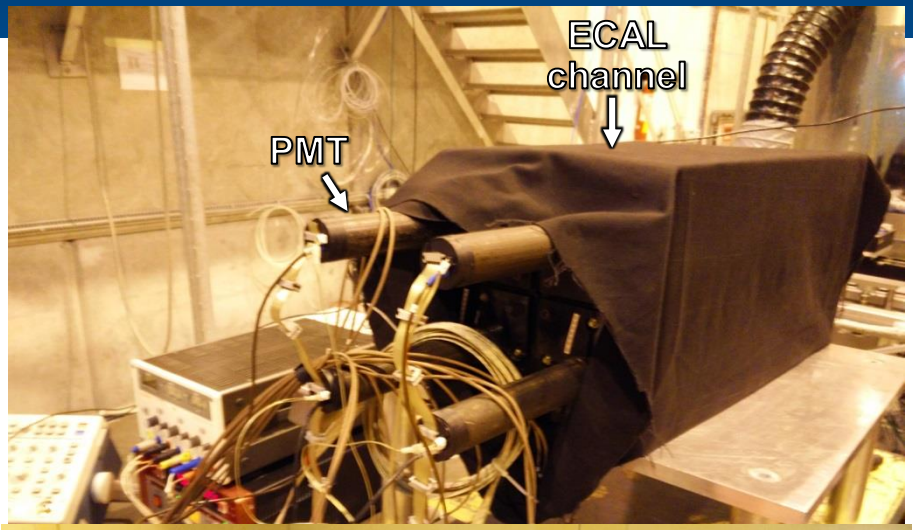
- Check noise in different conditions:

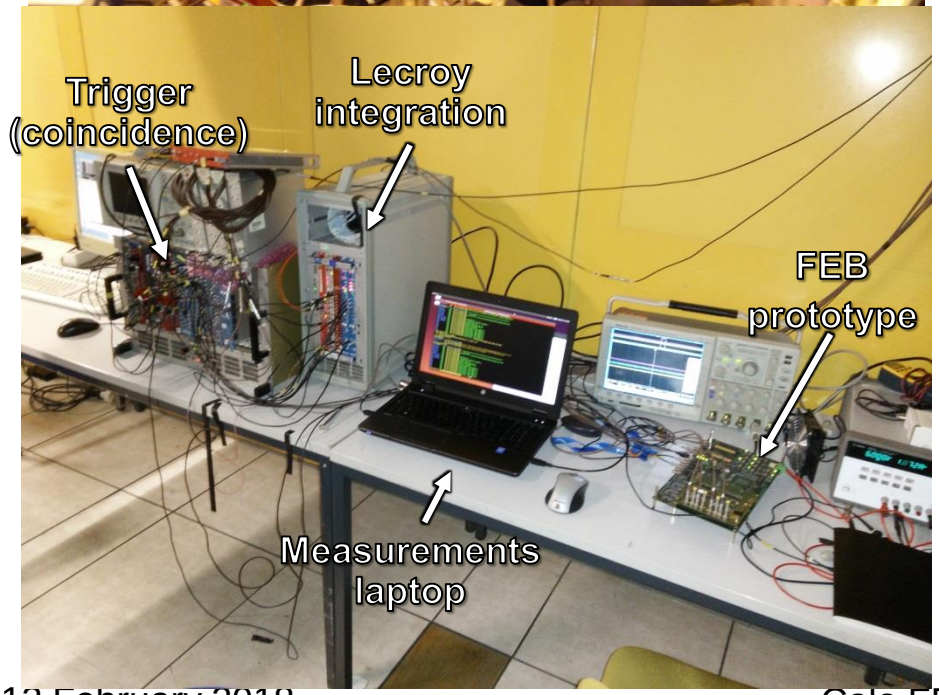
	Noise (LSB)	PS noise (LSB)
Laboratory	1.4	1.7
Lab + cable	1.6	1.8
Test beam	12	2.7
Detector	< 7.1	< 2.9

- **FEB prototype**
- **Provisional GND**

- Spec: ~1 ADC count
- The effects of Cockcroft-Walton HV sources and cables increase noise
- Upgraded detector expected pile-up ~5 LSB
  - Effect of electronics noise adds up to 5.8 LSB (vs. 5.1 LSB specified)

II. ICECAL ASIC: tests beams





- Beam line: T4-H8 at CERN Prevessin
- Beam: e^- with energy ranging from 20 to 120 GeV
- Elements used:
  - 4x(ECAL module+PMT+12m cable)
  - FEB prototype
  - Lecroy integrator
  - Time-to-Digital Converter (TDC)
  - ICECALv3 ASIC
- Main tests:
  - **Plateau and spill-over**
  - Linearity
  - Noise

II. ICECAL ASIC: radiation hardness tests

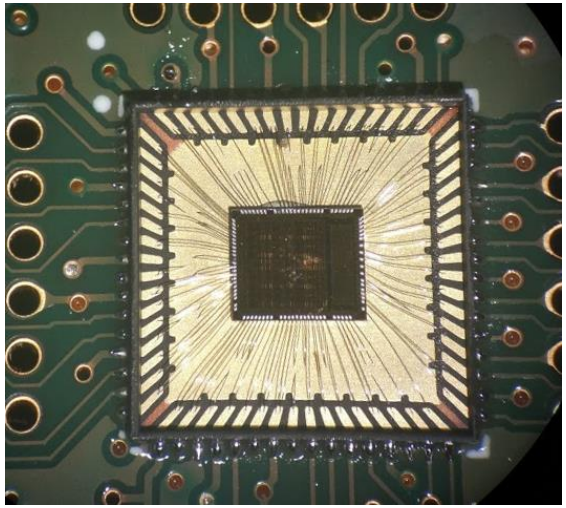
At CRC (UCL) in Louvain-la-Neuve (Belgium)

TID tests:

- Use beam of 61 MeV protons
- Different irradiation steps. Dose:
  - 55 krad over 3 chips
  - 40 krad over 1 chip
- Results:
  - During irradiation no SEU or SEL was detected
  - No relevant variation on the chips characteristics was observed

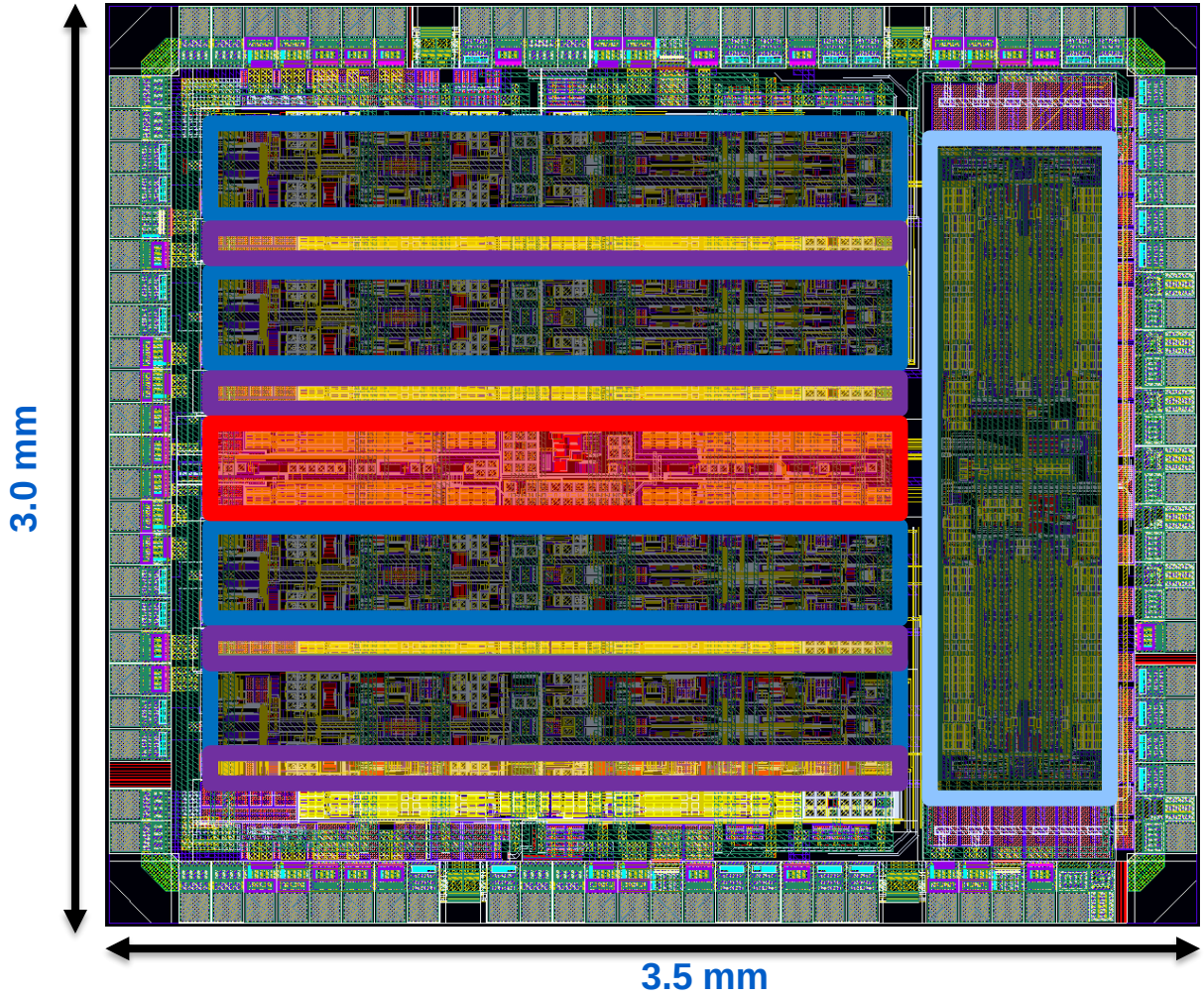
SEE tests:

- Irradiate with heavy ions: 58Ni+18
  - LET = 20.4 MeV/mg/cm2
- Two chips were irradiated:
  - No SEU detected after a fluence of 9,5·107 part/cm2
- 10 kHz refresh signal (SPIREFRESH)
- Equivalent expected limits for all channels in detector lifetime:
  - 1.3 SEU
  - 0.9 SEL



LHCb Upgrade Electronics

ICECALv3. A Full Custom design



IBias Block

Analog Ch

3-Voting FFs

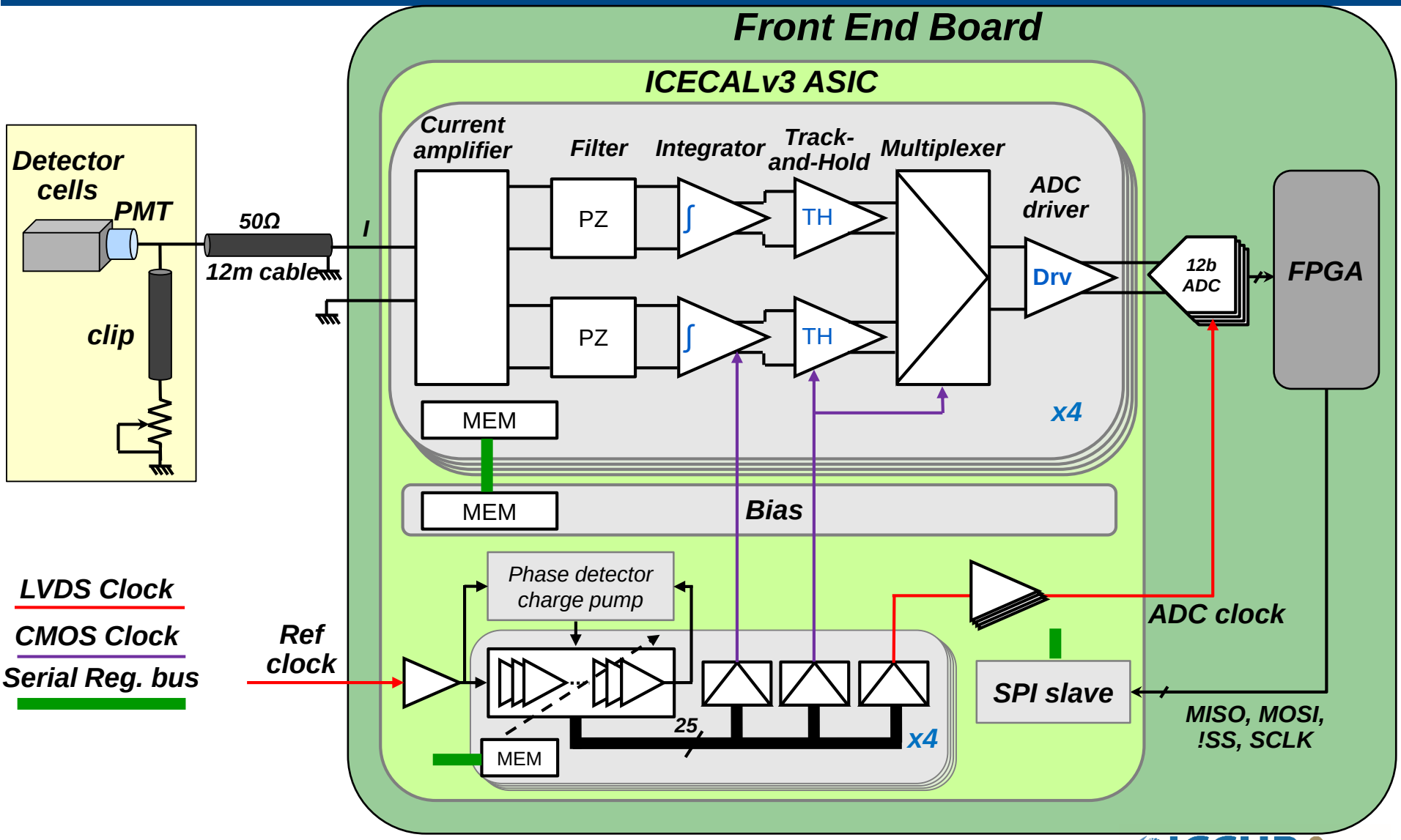
DLL + SPI

Die Area = 10.5 mm^2

Submitted: March 2014

ICCUB Institute of Cosmos Sciences
EXCELENCIA MARÍA DE MAEZTU

Backup: ICECALv3 architecture



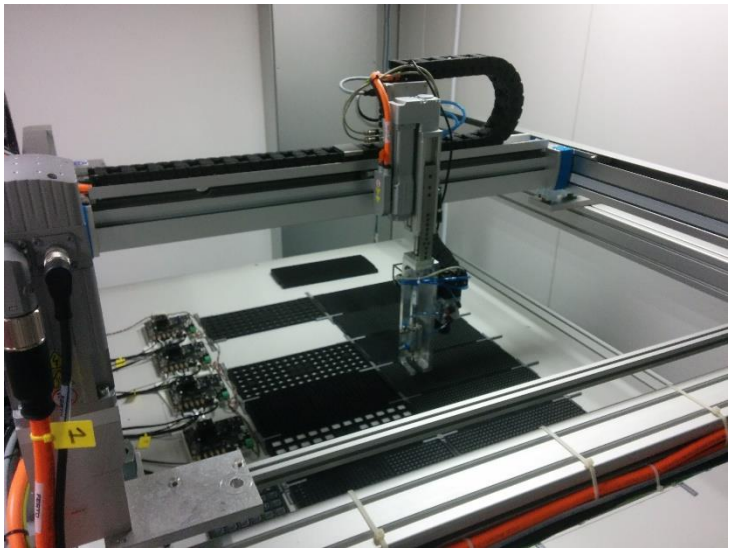
Dynamic range and version decision (I)

	v3.1	v3.2
Sensitility (fC/LSB)	4.54	9.05
Cint	14	8
Pedestal	311	311
Dynamic range (LSB)	3784	3784
1 LSB (MeV)	2.5	5
Dynamic range (GeV)	**9.5**	**19**
Noise (LSB)	1.21	1.06
Noise PS (LSB)	1.66	1.26
Noise (MeV)	3	5.3
Noise PS (MeV)	4.2	6.3
Equivalent noise from detector (LSB)	2.1 to 2.4	2.1 to 2.4
Noise PS+detector noise (LSB)	2.7 to 2.9	2.4 to 2.7
Noise PS+detector noise (MeV)	**6.5 to 7.2**	**8.0 to 8.6**

- Which ASIC version?
  - ICECALv3.1.
    - √ Lower noise
  - ICECALv3.2
    - √ Increased dynamic range
  - Mixed solution? For example:
    - Inner FE with ICECALv3.2
    - Outer FE with ICECALv3.1

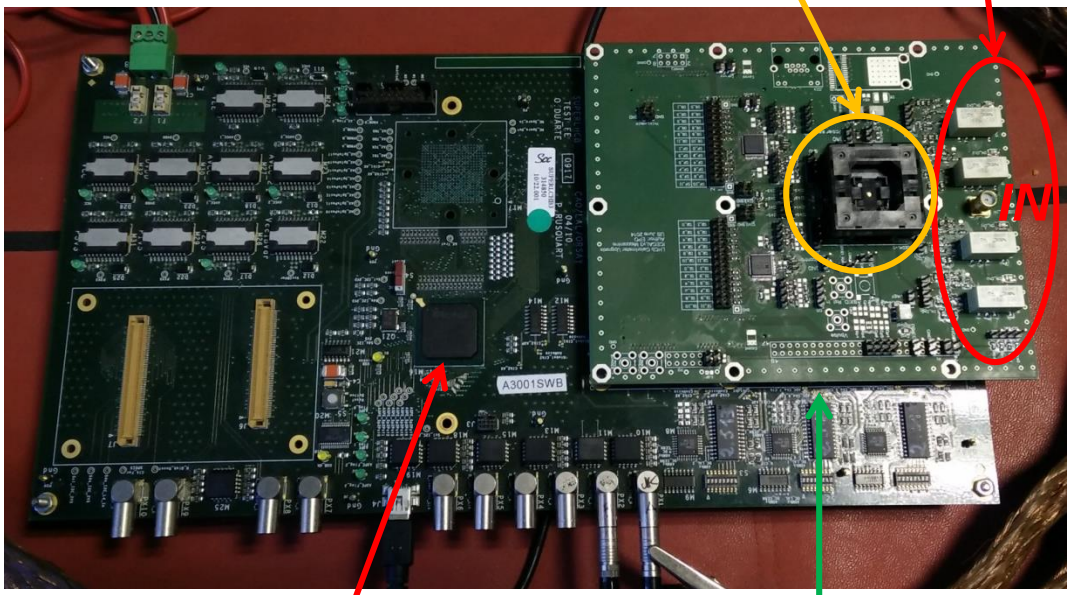
Production quality control

Robotic system



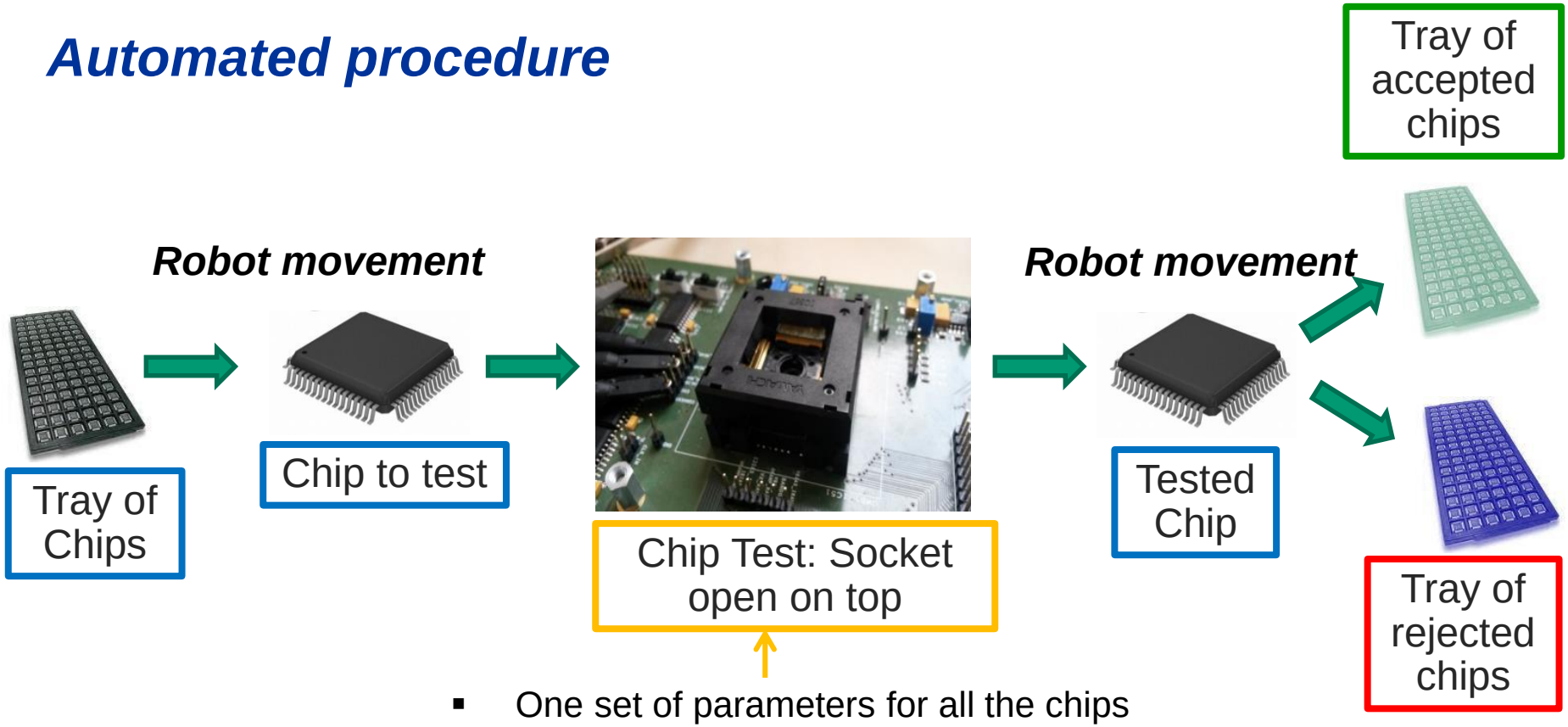
- Motorized horizontal gantry system to move the chips from tray to the test PCB and to final tray.
- Motorized stage in the vertical direction.
- Pneumatic suction.
- Pressure sensor.

FEB prototype (4 data channels)



Production quality control

Automated procedure



- One set of parameters for all the chips
- The optimal parameter set of values is obtained from a statistically reasonable amount of chips.
- 2 min < t < 5 min

Example: ASICs tested per robot run

Elements/Package	PACTA (Example)	ICECAL
Package	QFN32	QFN64
Size	6x6mm^2	9x9mm^2
Num Chips/Tray	490	260
Num Trays	14	12
Num Chips/Robot	6860	3120
Num Chips per test	4	1
Robot Movement + photo per test	~176s	~44s
Test QC Time per test	~65s	~300s
Test Robot+QC iteration	~240s	~344s
Complete Run Test	114h→~5 days	298h→~12 days
Chips Tested per day	~1440 chips/day	~252 chips/day