FEB Performance Tests

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for the LAL team

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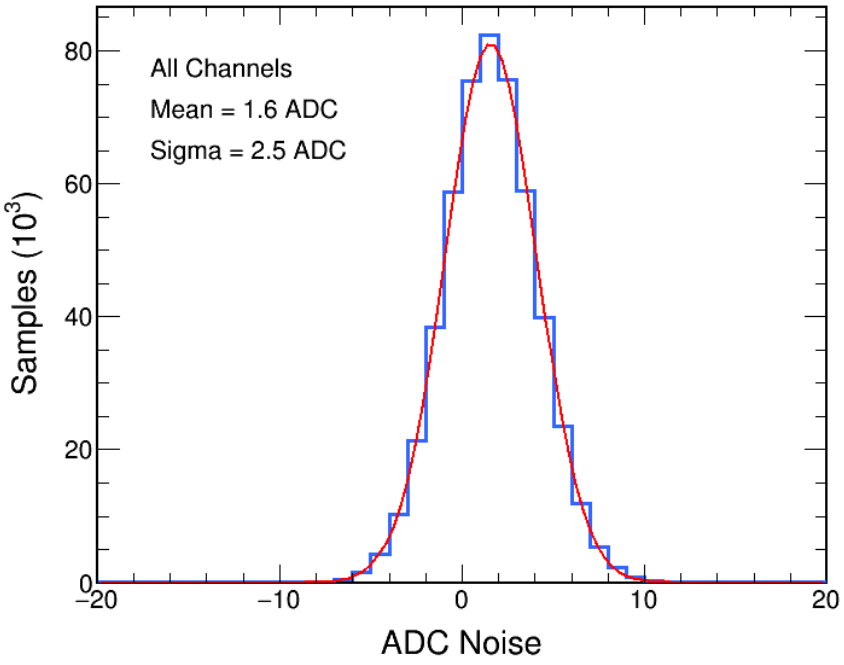
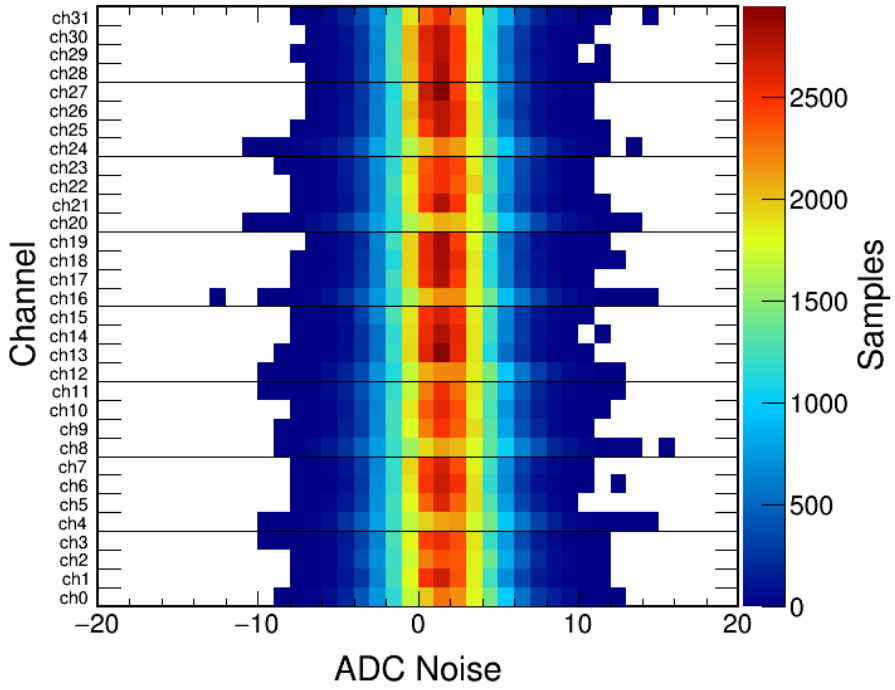
Outline

- General tests performed on the FEB:
  - Noise level and correlations
  - Linearity of integrated response
  - Cross-talk between channels
  - Time stability of the acquisition

Noise Level

- Acquisition was performed with no cables connected to the input signal
- Integrators were synchronized to match between events
- Bias due to pedestal subtraction: 1.6 ADC
- Noise width: 2.5 ADC*

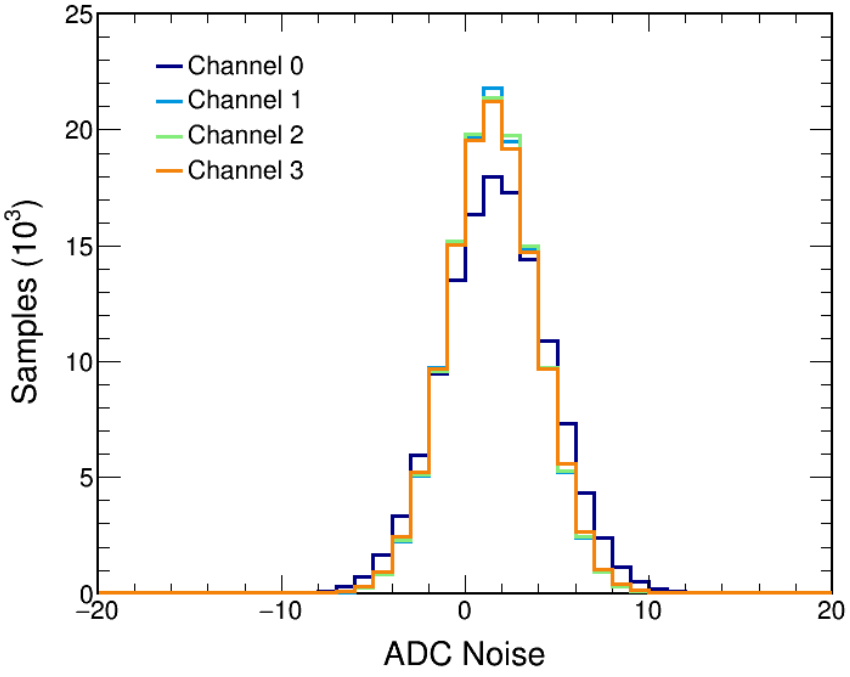


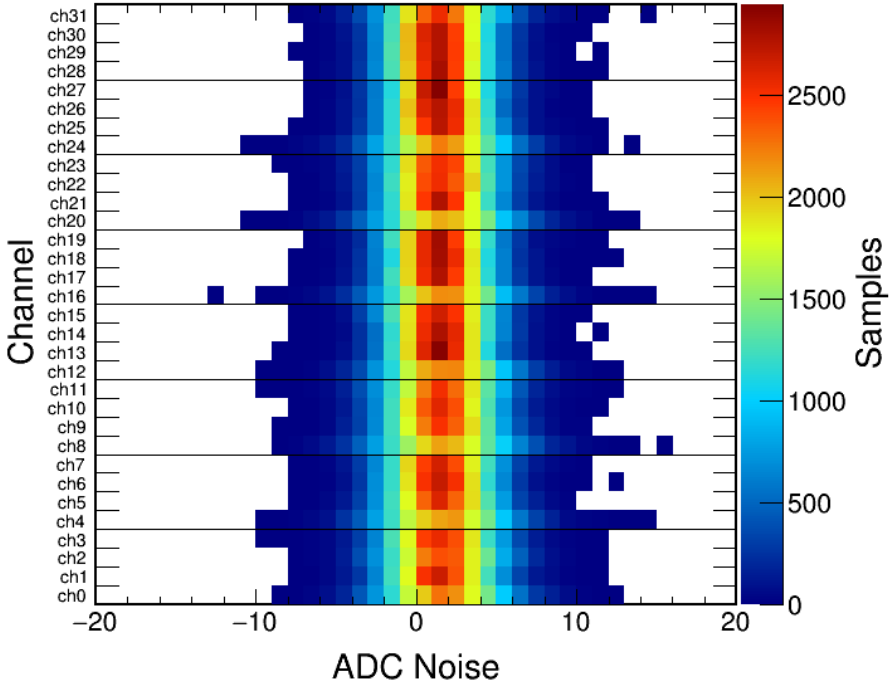


*1.8 ADC without pedestal subtraction

Noise Level

- Acquisition was performed with no cables connected to the input signal
- Integrators were synchronized to match between events
- Not all channels are equal
- Ch. 0 is noisier (2.9 ADC), while others are quieter (2.4 ADC)

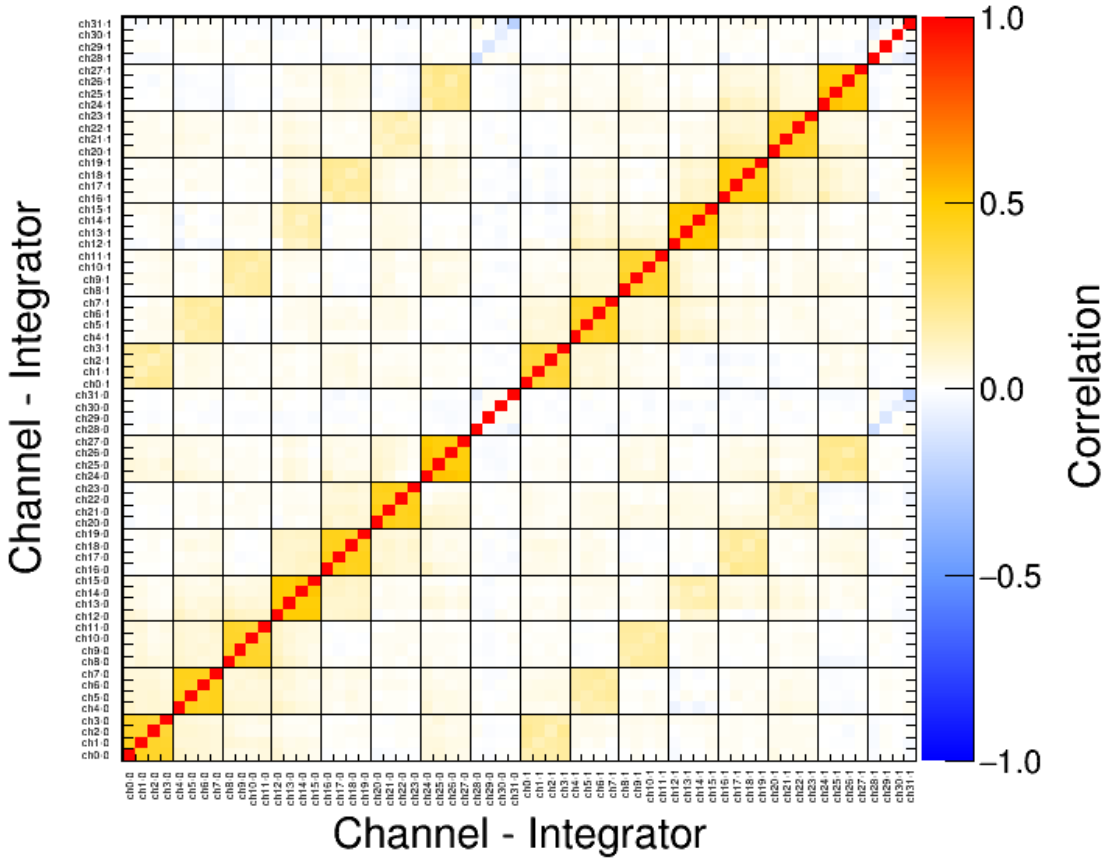




*1.8 ADC without pedestal subtraction

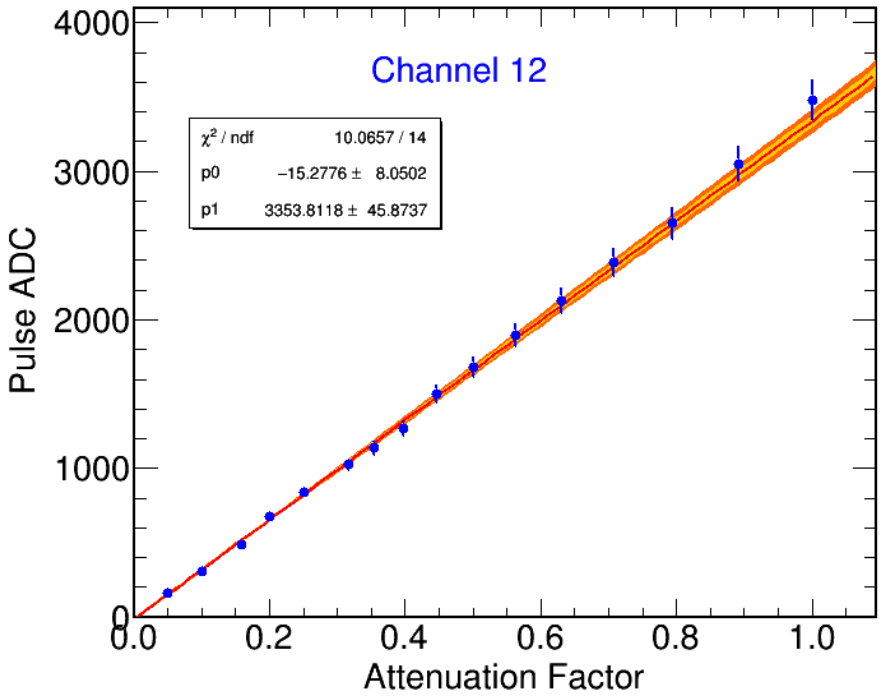
Correlations

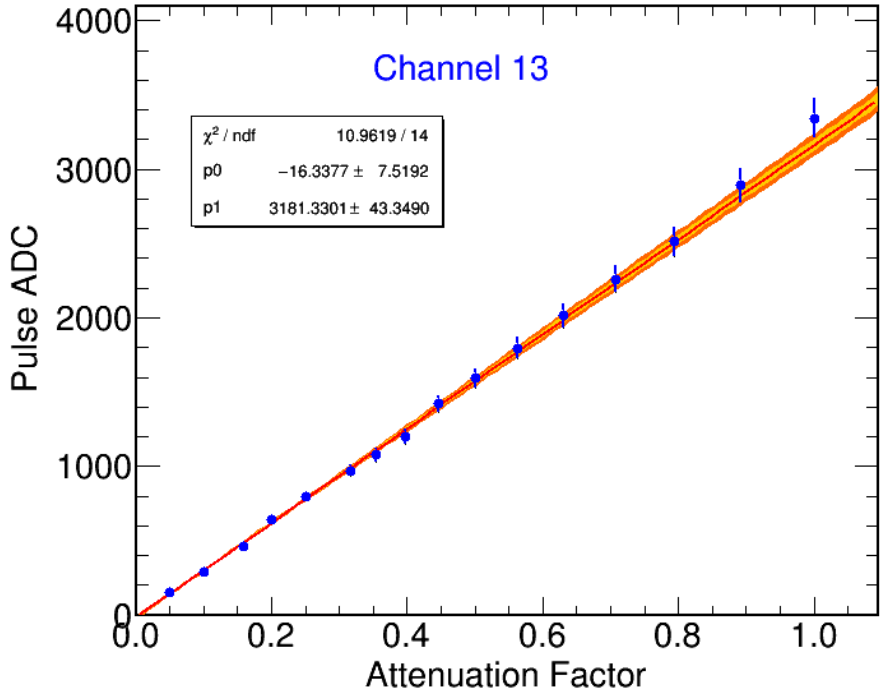
- Can also look at correlations between different channels and integrators
- Observe 45% correlation between channels in same chip and integrator
- Between integrators, correlation drops to 17%
- Correlation between channels in different chips is 3.6%
- Chip 7 has different behavior in this board



Linearity

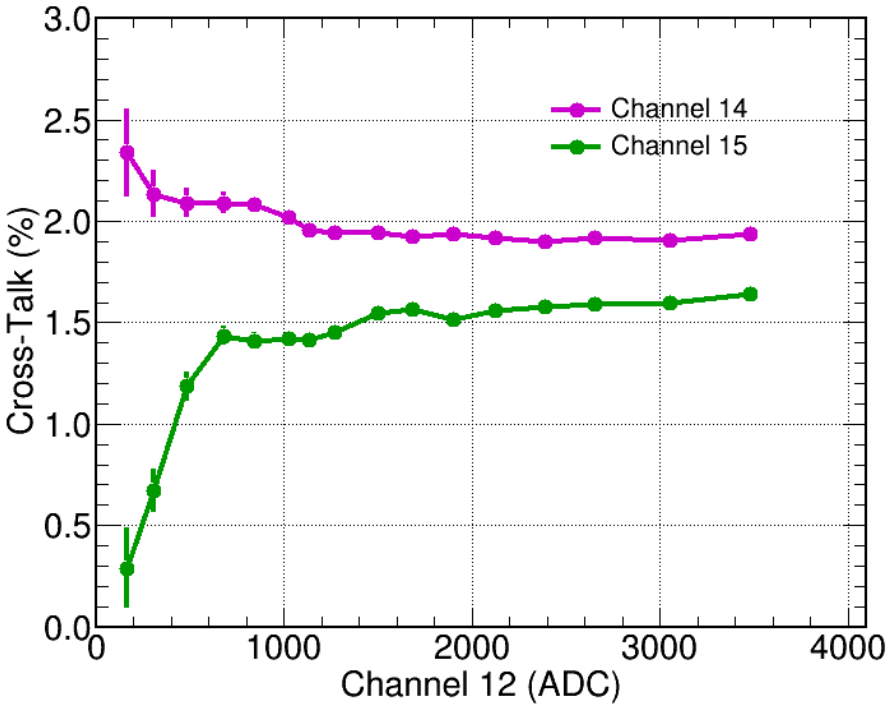
- Acquisition with pulses injected in channels 12 and 13 (chip 3)
- Channels 13 and 14 were not connected
- Used attenuators to control injected pulse size
- Maximum amplitude tuned to generate ~18 pC (4.5 fC/LSB)
- Measured attenuator precision to be at 4% level





Cross-Talk

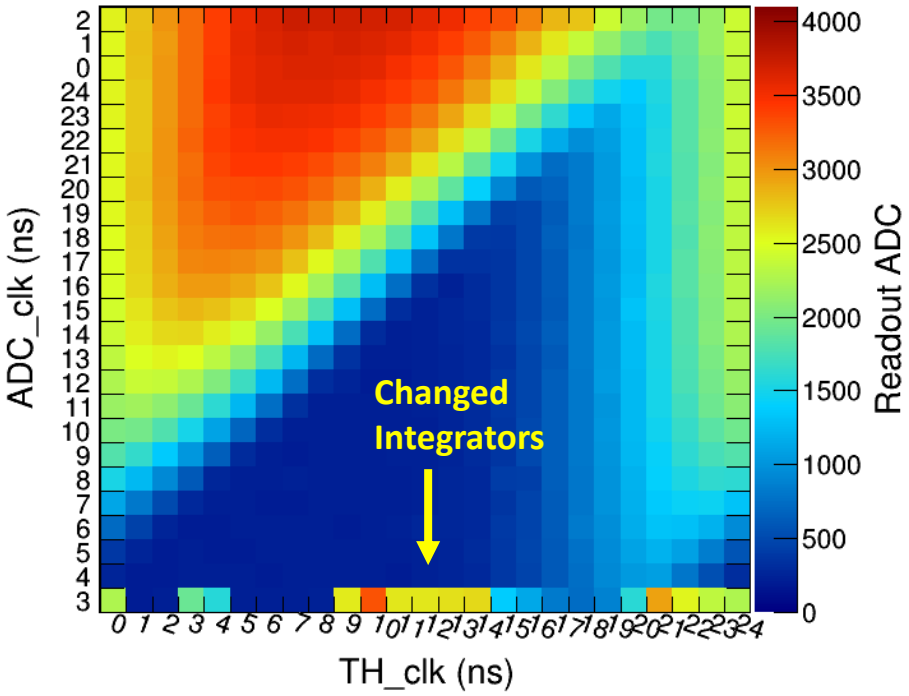
- Using same acquisition from linearity test, measure cross-talk in adjacent channels 14 and 15
- Setup is not ideal as cross-talk channels were not connected and pulses had been injected in two channels
- Preliminary tests with improved setup:
  - Single channel injected with pulse
  - 2 chs connected to 50Ω resistance
  - No significante cross-talk observed in those two channels
  - Unconnected channel sees cross-talk at ~1% level
  - Further tests needed with all channels connected and variable signal amplitude



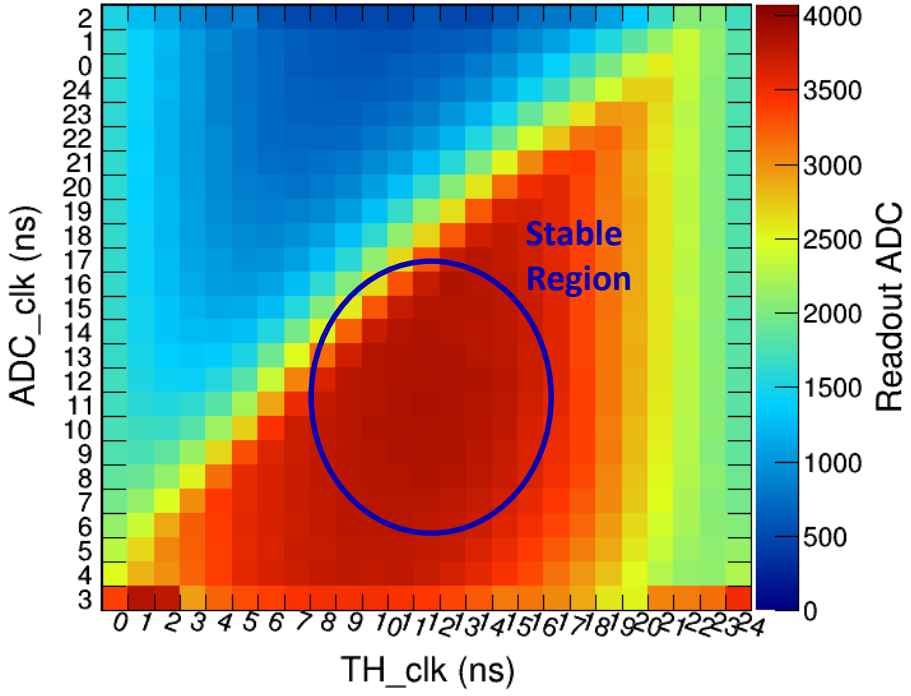
Time Stability

- Testing for stable range of clock phases for acquisition
  - Inject pulses at fixed amplitude
  - Vary TH (start integration) and ADC phases
  - Find range of phases within 1% of maximum readout

Sample 27

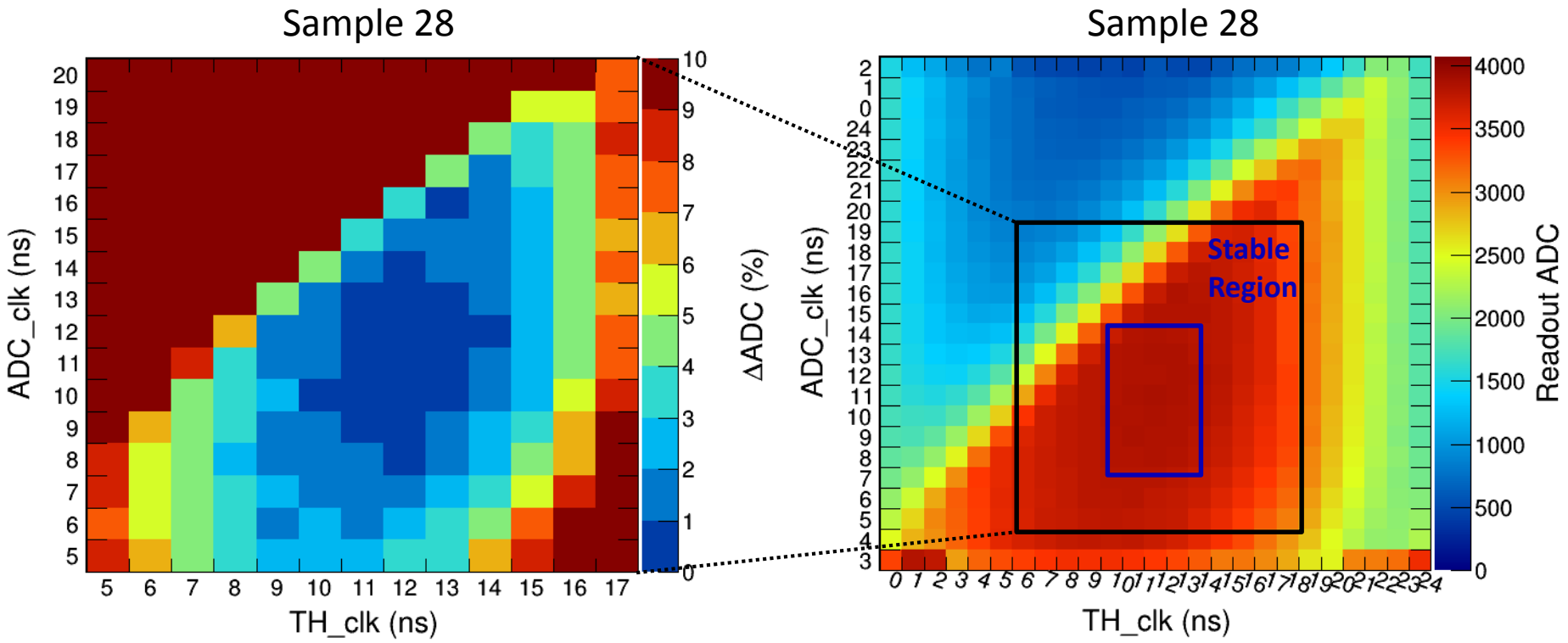


Sample 28



Time Stability

- Testing for stable range of clock phases for acquisition
  - Inject pulses at fixed amplitude
  - Vary TH (start integration) and ADC phases
  - Find range of phases within 1% of maximum readout
  - About 7ns stability in ADC clock



Conclusion

- Initial performance tests of the FEB show promising results
- Noise level a bit higher than expected, but reasonable
- Correlations mostly within chip
- Linearity demonstrated over full dynamic range
- Cross-talk level still under investigation, but below 2%
- Readout stable over 7ns in ADC clock

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