Production Readiness Review

Introduction

Electronics PRR

The LHCb calorimeter upgrade group

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Reminder of the LHCb calorimeters

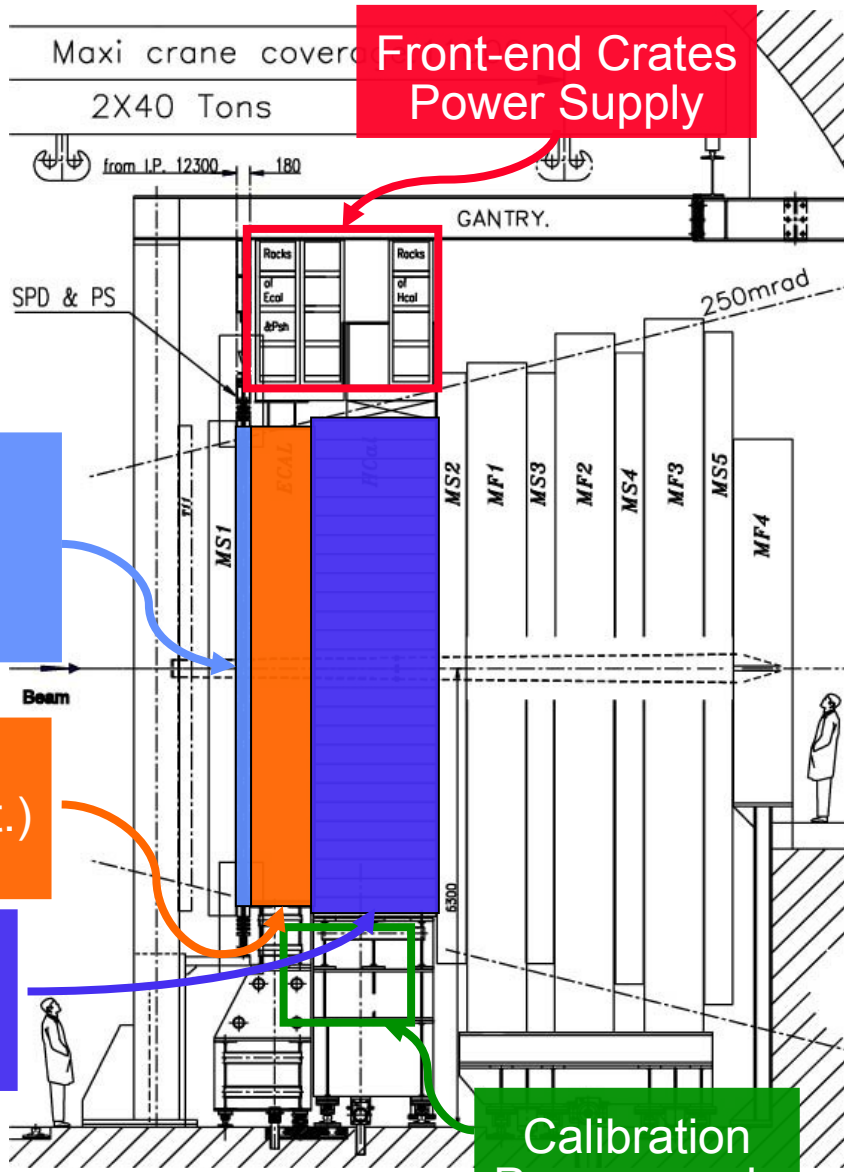
- The LHCb calorimeter system is based on the SPD/PS, ECAL and HCAL
- Requirements :
  - Energy/position measurements
  - Particle id for γ, electrons, hadrons
  - Present L0 trigger input
    - almost no spill-over
    - fast response

Scintillating Pad Det (SPD)
Preshower (PS)
Scint. Pad + Fibres+ MAPMT
6016 cells each

same electronics same crates

ECAL
Shashlik (Pb-scint.)
6016 cells

HCAL
Tiles (Iron-scint.)
1488 cells



Key points of the calorimeter upgrade

- New design of the Front-end electronics
  - The calorimeter data will be sent @ 40 MHz to the upgraded-HLT / PC-farm
  - Reduction of the PMT gain (factor 5) to reduce the integrated current
  - The calorimeter will provide the necessary information to make the LLT decision
- The SPD/PS system is removed
  - Not so important after L0 disappears
  - Particle identification is affected
  - Easier calibration of the ECAL/better resolution
- The module will degrade because of radiations (affects the innermost cells)
  - ECAL baseline:
    replacement of the most affected modules planned for LS3
  - HCAL should survive longer
    - Performances will not be in specs up to 50fb^{-1} (central region)
      - HCAL mainly used by L0
      - Not critical to lose the most internal cells after several tens of fb^{-1}
- Upgrade beam conditions have an impact on the performances
  - Pile-up → look for new cluster shapes (reconstruction)
  - Particle id. for photon and electrons → related to SPD/PS removal

Major developments

- Mainly concerns the electronics
  - New front-end electronics
    - 278 FEB
      - Prototypes of the analog and digital parts have been designed
      - FEB prototypes equipped with ICECAL have been tested intensively
        - Close to the final version (wait for latest consolidation proto.)
        - Integrate the final components (optical links, etc…)
    - 21 Control boards
      - Prototype has been tested and firmware developped
      - Final version reached
  - Electronics for the HV control, monitoring and calibration
    - Keep a large fraction of the present electronics
      - Modify 2 mezzanine boards
    - Design a GBT fanout (optical link → elinks)
- Firmware development (microcode) for the TELL40
  - Event building and distribution of the events to the farm
- Dismantling of the SPD/PS/Lead
- Reconstruction software for the calorimeter objects
- Replacement of the innermost modules of the ECAL during the LS3

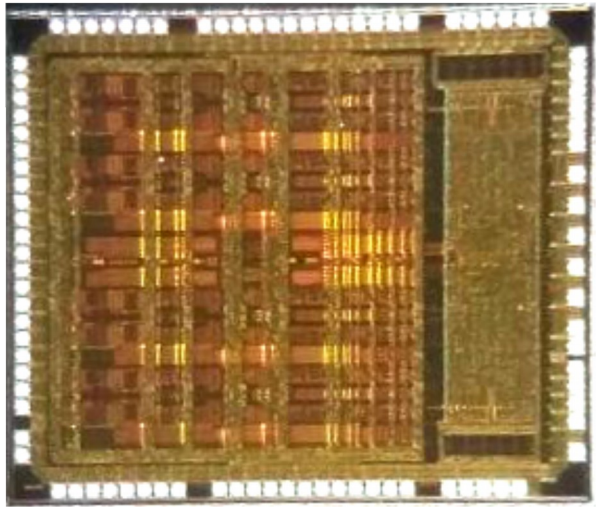
Work packages

- Analog electronics
  - Spain
- Front-end boards for the ECAL/HCAL (digital part)
  Control board (3CU)
  Readout (TELL40 calo specific code)
  - France
- HV/Calibration/Monitoring systems
  - Russia, Ukraine
- Installation/Dismantling/Commissioning
  - CERN, France, Russia, Spain
- Software for the reconstruction, identification
  - France, Russia, Spain

Analog electronics (I)

- Basic requirements

Parameter	Requirement
Energy range	$0 \leq E_T \leq 10$ GeV (ECAL)
Calibration/Resolution	4 fC/2.5 MeV per ADC count
Dynamic range	4096-256 = 3840 cnts: 12 bits
Noise	$\lesssim$ 1 ADC cnt (ENC $<$ 4 fC)
Termination	$50 \pm 5\ \Omega$
Baseline shift prevention	Dynamic pedestal subtraction
Max. peak current	4-5 mA over 50 Ω
Spill-over residue level	$\leq 1\%$
Non-linearity	$< 1\%$
Cross-talk	$< 0.5\%$
Timing	Individual (per channel)



ICECAL ASIC v3

- 2 competitive developments : COTS design and ASIC (ICECAL)
  - Choice of the technology in 2014 → ICECAL
- EDR and PRR of the ICECAL passed
- Several versions developed
  - Full integration of the time alignment of the channels in the chip
  - Integration of a pole-zero compensation
    - Reduction of the spill-over, better int. curve sampling
  - Analog gain is tunable (calo Et range flexibility)

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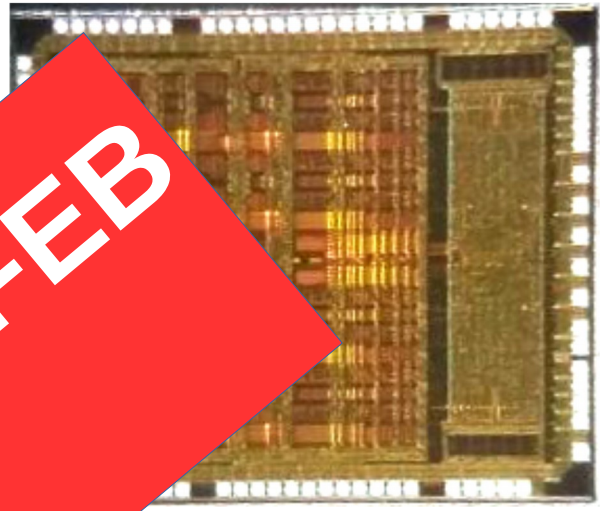

ICECAL ASIC v3

Analog chip of the FEB produced

- 2 competitive develo nd ASIC (ICECAL)
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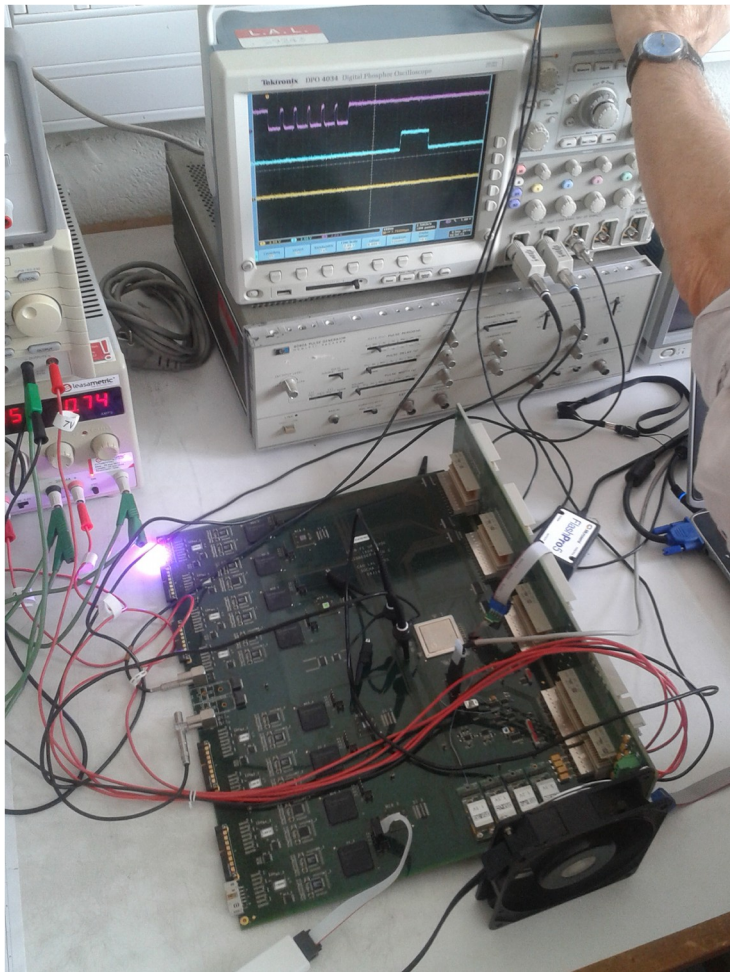
Front-end board

- 2 prototypes of the Front-end board exist
- First prototype
  - Realistic acquisition implemented
    - Used in real conditions (Module) with ICECAL
      - Test beams (see below)
    - But no GBT and only 8 channels

FEB proto 1

Front-end board

- 2 prototypes of the Front-end board exist
- First prototype
  - Realistic acquisition implemented
    - Used in real conditions (Module) with ICECAL
      - Test beams (see below)
    - But no GBT and only 8 channels
- A second prototype has been produced
  - See presentation of Christophe
- The acquisition has been tested
  - Data stream
  - Solw control
- Wait the final version: a few corrections wrt the present one



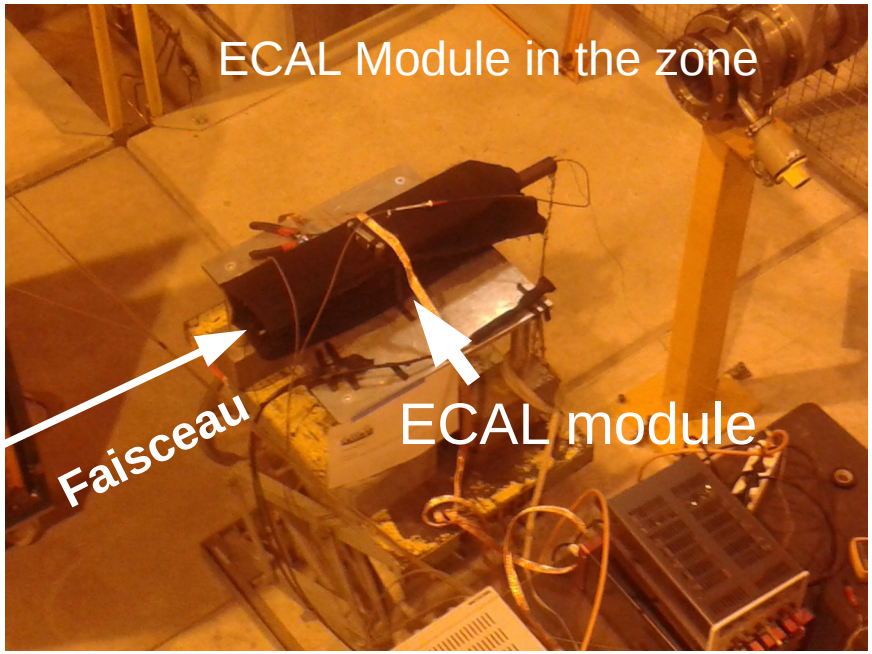
FEB proto 2

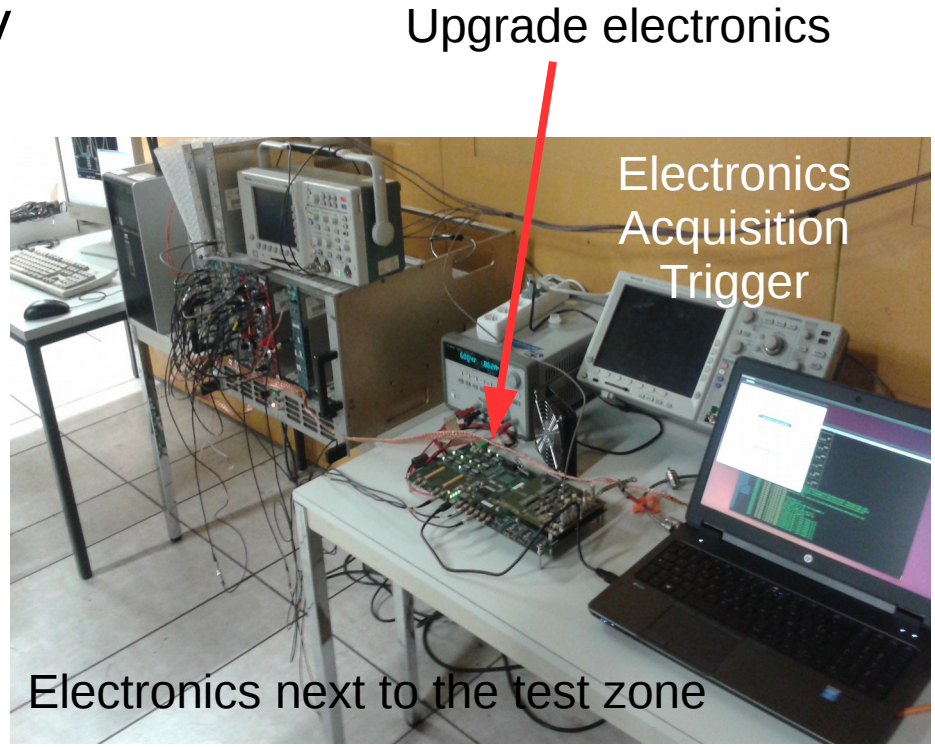
Front-end board

- FEB EDR passed last year
  - Based on a realistic FEB version
- Most of the components used are already certified.
  - ~10 components of the FEB have been tested in June/July with ICECAL at Louvain-La-Neuve
- Firmware of the FPGA is partially available
  - Simulations of the response of the firmware to injected ADC values
  - Part of the present code can be used
- Custom test bench software available
  - Used for the test benches, test beams and irradiation tests
- We hope to be able to start the production very soon
  - Tests will be shared between France and Spain (2 test benches)

Analog and Front-end board tests

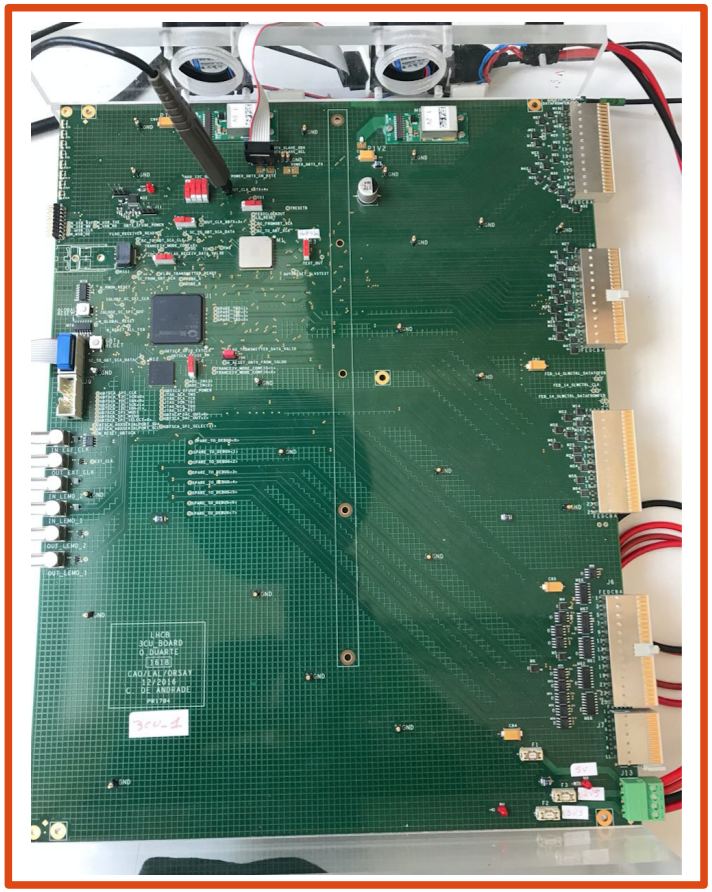
- The electronics has been tested during 2 test beams in 2014/2015
  - Electronics used
    - ICECAL (+ COTS design in 2014)
    - Front-end board prototype
  - Electrons from 20 to 120 GeV





Control board

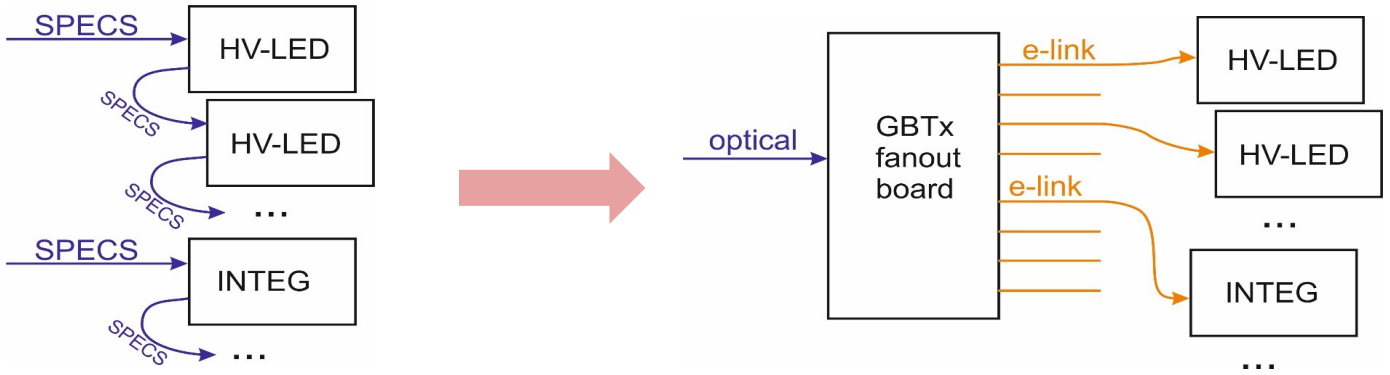
- The CTRL board performs a similar treatment as the VLDB board (CERN)
  - Mainly Slow control signal distribution
  - Add some functionalities
    - TFC – fast commands
    - Clock distribution



- A realistic prototype has been designed
  - Final components used
  - No modification is forseen before production

- The control board uses the same components as the FEB
  - CTRL board specific components have also been tested in June/July at Louvain-la-Neuve

- System mostly independent from data taking
- The components are
  - HV-LED boards (standalone)
  - INTEG boards (readout of the HCAL PMT current, standalone)
  - LEDTSB (LED calibration) installed in the FE crates
- Very modular system
  - Motherboards are kept
  - LEDTSB equipped with 2 mezzanines that need to be replaced
    - 12 Slow control board → move to the GBT-X/GBT-SCA



    - 12 Ctrl board → upgrade the FPGA generation (IGLOO2)
  - Need also to build a fanout board (12 copies including spares)

HV/Monitoring/Calibration for ECAL/HCAL

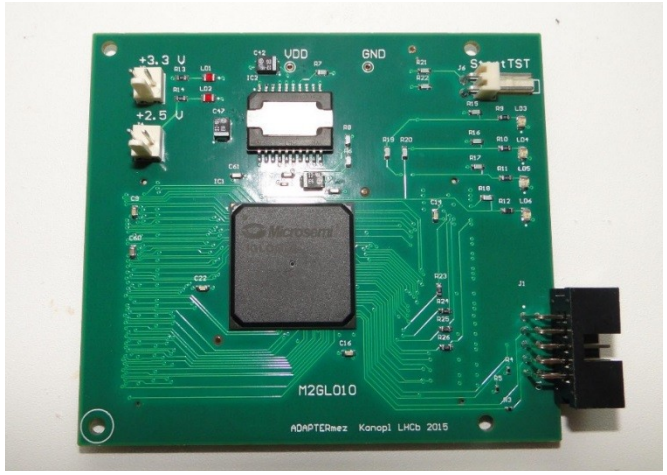
- Prototypes of
  - Ctrl mezzanine
  - GBT-SCA mezzanine

  have been produced

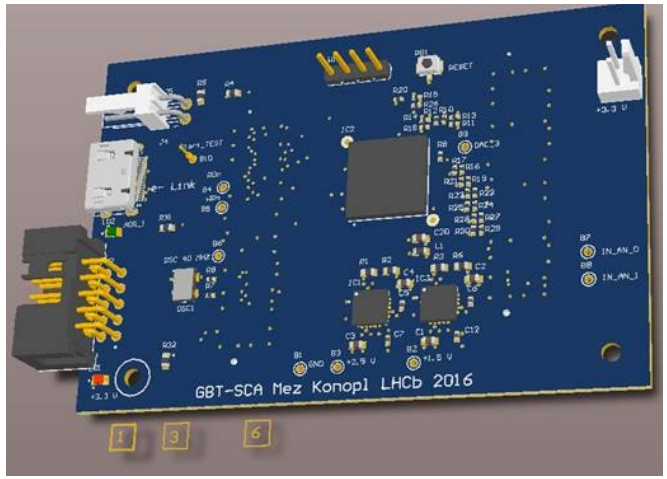
- ELMD prototypes of the ELMD boards have been produced
  - Close to the CERN VLDB board

- Hardware has been tested intensively

- See presentation by Yuri/Anatoli



New Control mezzanine



GBT-SCA mezzanine

Procurement of the components - Production

- Components bought for full production (all boards)
  - DC-DC converters
  - GBT-X
  - GBT-SCA
  - VT-T/R-x
  - … all the other components (except for the ICECAL ASIC) are commercial chips and are easily available

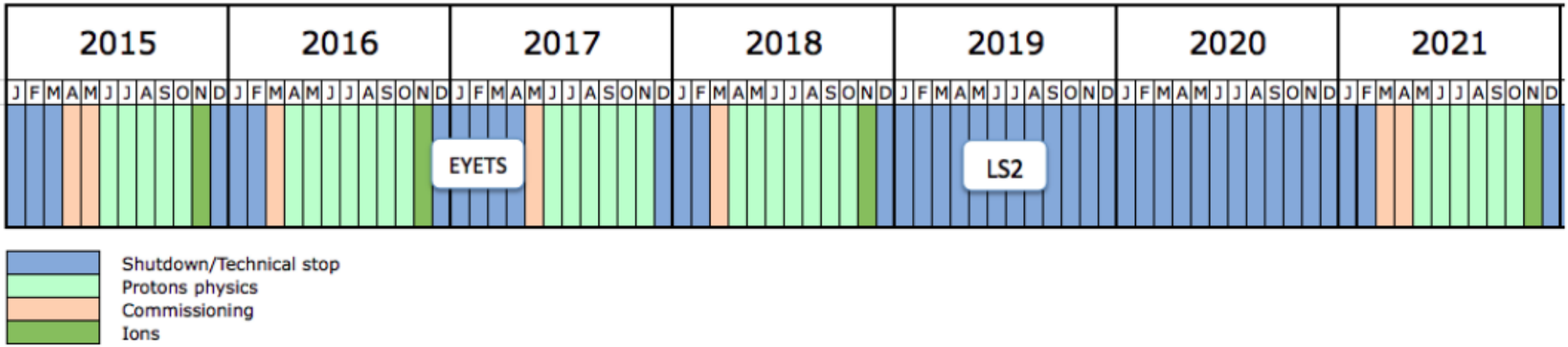
- Optical links, counting room
  - Definition of the optical path (number, patch panel, etc…)
    - Almost completed
  - First estimation of the number of TELL40/SOL40 (counting room)
    - Almost ready

- Dismantling
  - Manpower: essentially contributors to the installation of the SPD/PS
  - Definition of the necessary tooling in progress
    - Try to recuperate the tools used for the installation
  - Try to organize activities in parallel
  - No specific issue related to this activity

- TELL40 microcode
  - Data format specified
  - No fancy data compression necessary for the calo (widebus mode)

- Work on pile-up (cluster reconstruction)

Schedule - Conclusions



We do not expect significant issues or delays
The development is well-advanced and the critical decisions have been taken

Should be ready for installation at the end of 2018

Executive summary

- Analog electronics
  - EDR, PRR passed
  - Production completed
- Front-end boards for the ECAL/HCAL (digital part)
  - FEB EDR passed
  - Production should start as soon as possible
- Control board (3CU) - HV/Calibration/Monitoring systems
  - EDR passed
  - Schedule follows approximately FEB planning
- HV/Calib/monitoring
  - EDR passed
  - 2 mezzanines and a fanout GBT board to design
  - No specific problem
- Readout (TELL40 calo specific code)
  - Optical link path well defined (number of links, patch-panels, etc…)
  - Already an important activity on TELL40 microcode