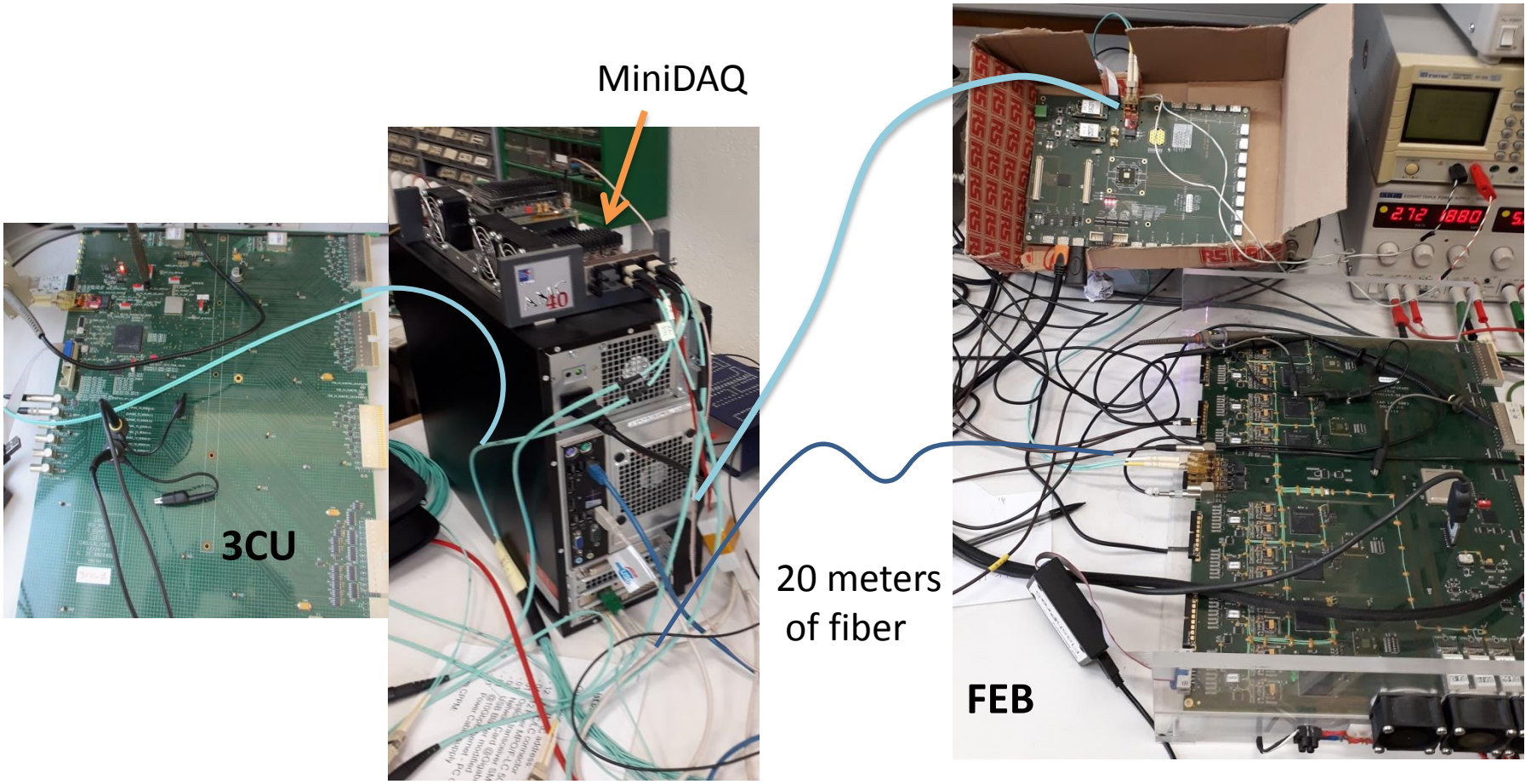
slow control and acquisition

The MiniDAQ environment

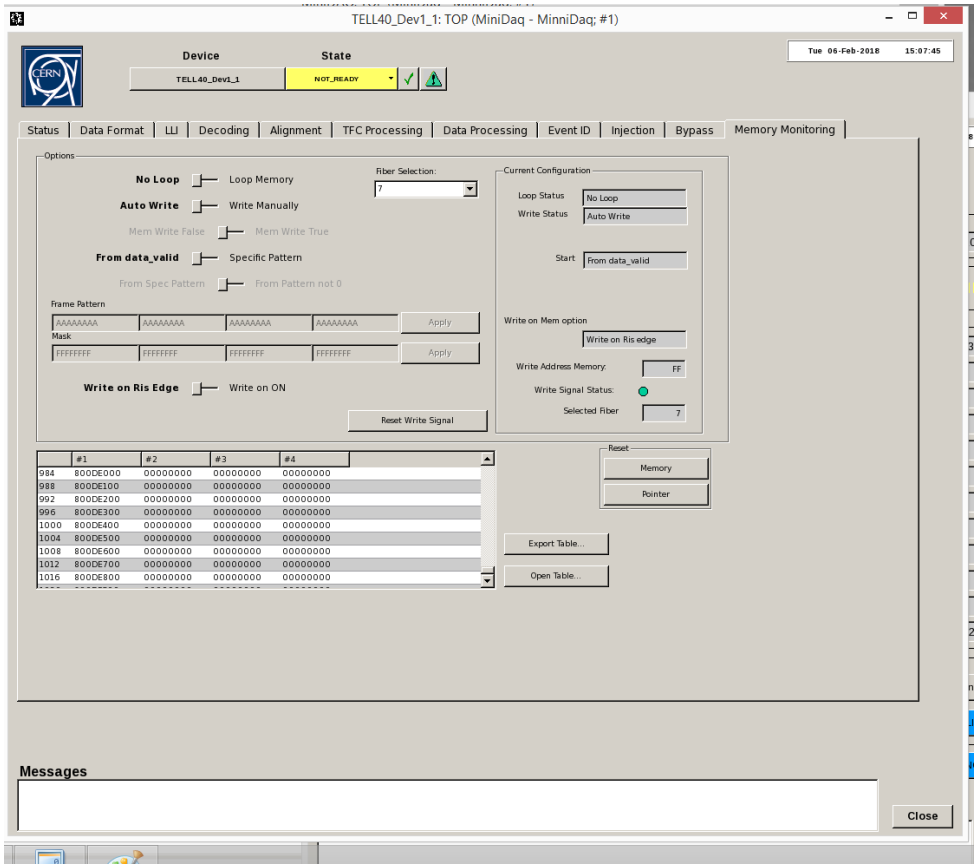


Configuration of the FEB

The FEB is configured by the USB with program in python and C++ libraries

The board should be initialized , The different elements (ICECAL, FE-PGA,SEQ-PGA) are configured by the SPI, and I2C , through commands sent by the USB

Test FE Data part

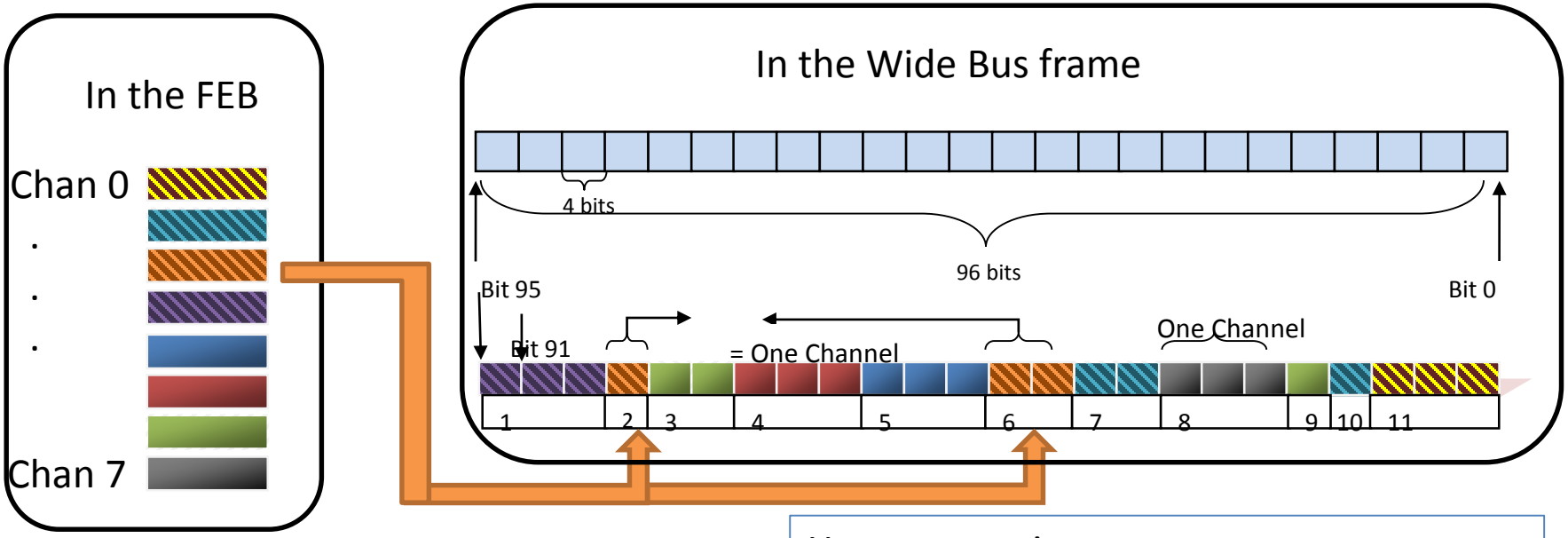


Test of the Data Frame received in the Memory Management :

- In fixed pattern mode (0xAA BB ..)
- Random pattern mode

Test BCID is OK
easy to check from the Memory Management panel

Data part more difficult to check
(see next slide)



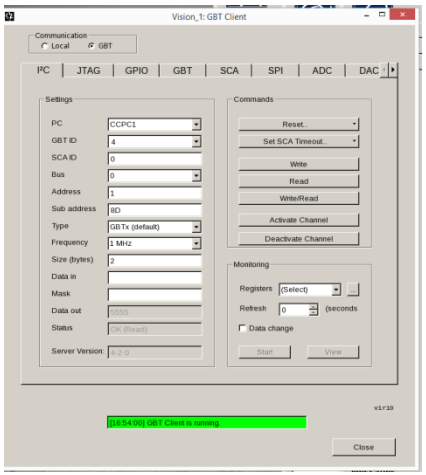
Specific data encoding of the FEB

How we test it :

1. Load FE injection Ram with specif pattern
2. Verification with a program to retrieve a specific pattern put in the data sent by the FEB in files written by the amc40_frgwriter of the miniDAQ

Test I2C communication with GBT-SCA of the FE

GBT Client



FEB

Read/write of some Register of the different Gbtx of the FEB

By optic fiber

By mini-HDMI to back end

Test SPI communication with GBT-SCA of the FE

CCP1
terminal

Spi_test line
command used

FEB

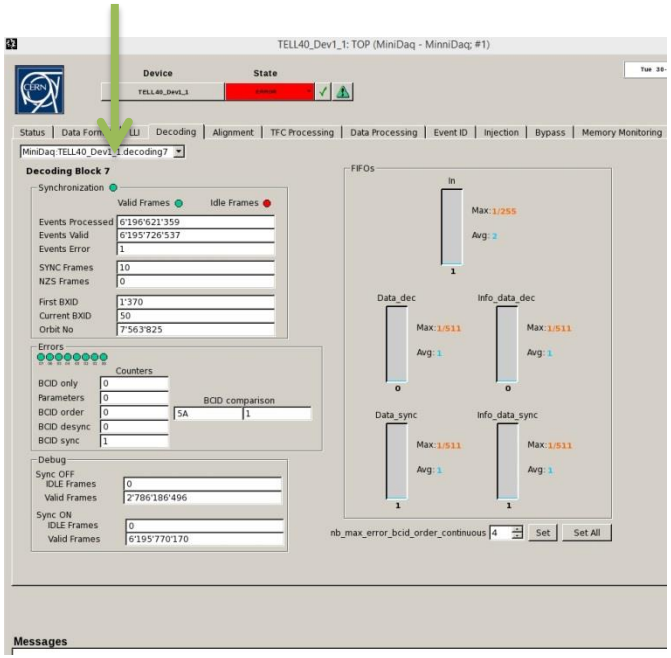
Read/write of some
Register of SPI different
Slave (ICECAL OK),
firrmware adaptations for
Fe_pga and Tri_Seq_pga

By optic fiber

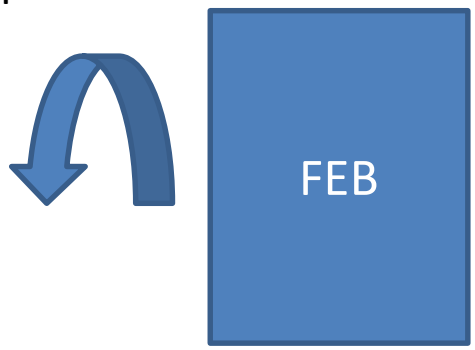
By mini-HDMI to back end

Test SyncFrame pattern to miniDAQ

Green led synchronized



Datas
Optic fiber 7



- a local command triggers 10 SyncFrames

SyncFrame = Configuration of the FEB to send the BCID under 12 bits with a fixed pattern after this.

- Commutation to normal datas with BCID under 8 bits after the 10 SyncFrames

⇒ The miniDAQ is synchronized !

⇒ But as we aren't synchronous with a TFC cmd the miniDAQ is in Error