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3CU
Calorimeter Control Card Unit

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Abstract

The project of the LHCb upgrade foresees a replacement of the whole acquisition system of the detector to allow a full readout at 40 MHz. The development of a new control board, called the 3CU for the electromagnetic and hadronic calorimeters was proposed. This board receives commands from the main LHCb control system and sends them through the backplane to the front-end boards. Each calorimeter crate is equipped with one unique 3CU plugged in the central slot which also provides the clock, slow controls, etc., to all the boards. This note gives a detailed description of the prototype of the 3CU board.

Contents

1 Introduction

For the purpose of the LHCb upgrade, it is foreseen to replace the electronics of the calorimeter. The calorimeter new acquisition system will be controlled by the so called 3CU board. It is responsible for sending and processing the information received though optical fibres from the main LHCb system to the front-end boards. A total of 23 control boards including spares are needed for both the electromagnetic and hadronic calorimeters. A complete description of this board can be found in the document. The note is is structured as follow, first a general description of the board will be present and it will be followed by a detailed description of the main blocks, functionalities and components of the board.

The LHCb operational master clock for data taking and the entire precise timing and synchronisation of the sub-detectors relies on the LHC bunch clock and the LHC orbit signal. The orbit signal marks each turn of the full LHC circulating bunch scheme (3563 steps). The S-ODIN receives directly these two clock from the RF-system of the LHC via an LHC Interface card located on the S-ODIN card. The LHC bunch clock is distributed to the FE and TELL40 readout boards with sufficiently low jitter (assumed for the moment to be O (10 ps)), and constant and reproducible phase. The S-ODIN card distributes the clock and the Fast Control commands to the SOL40 and TELL40 board, and the SOL40 board distribute the Clock and the Fast Control command to the 3CU board, as shown in Figure: 1. The calorimeter crate mechanics is a standard 9U VME-like frame.

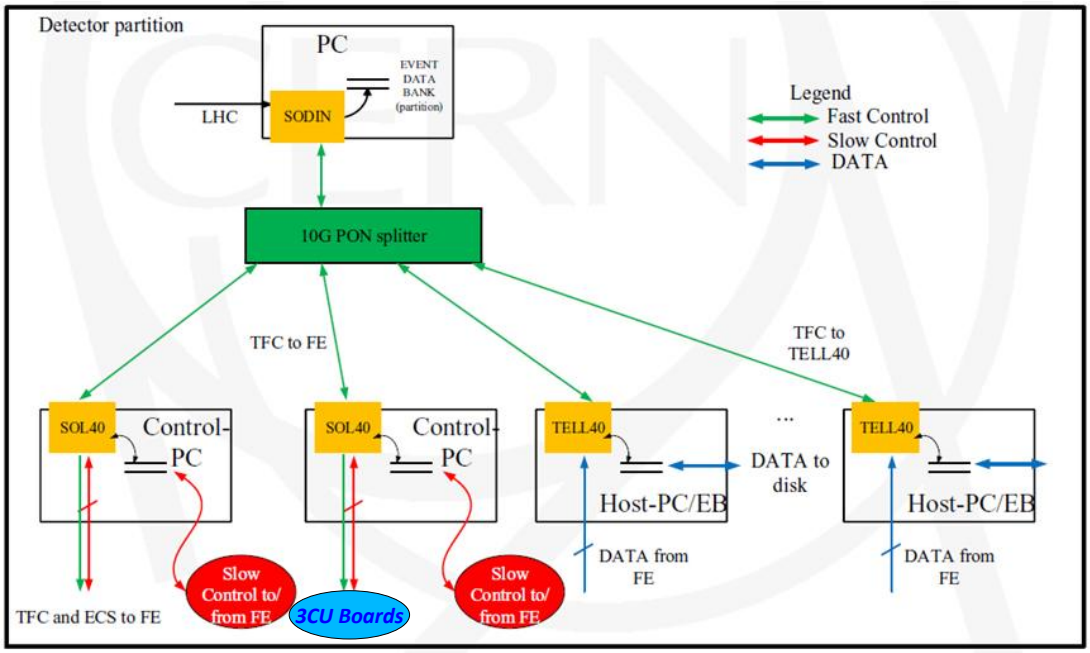

Figure 1: Architecture of the LHCb control system.

They have two custom backplanes mounted in the back. The lower one (3U backplane) provides the power supplies, the TFC commands and the clock distribution. The upper one (6U backplane) is dedicated for the exchange of signals between the boards (front- end boards and 3CU) inside the crate and with the other crates, see Figure: 2. A calorimeter front-end crate contains up to 16 front-end boards (FEB) which perform the acquisition

of the detector channels, and in the middle of the crate a reserved slot to the 3CU board. For the upgrade, we have been removed the validation board, that mean the space for these two card will be free.

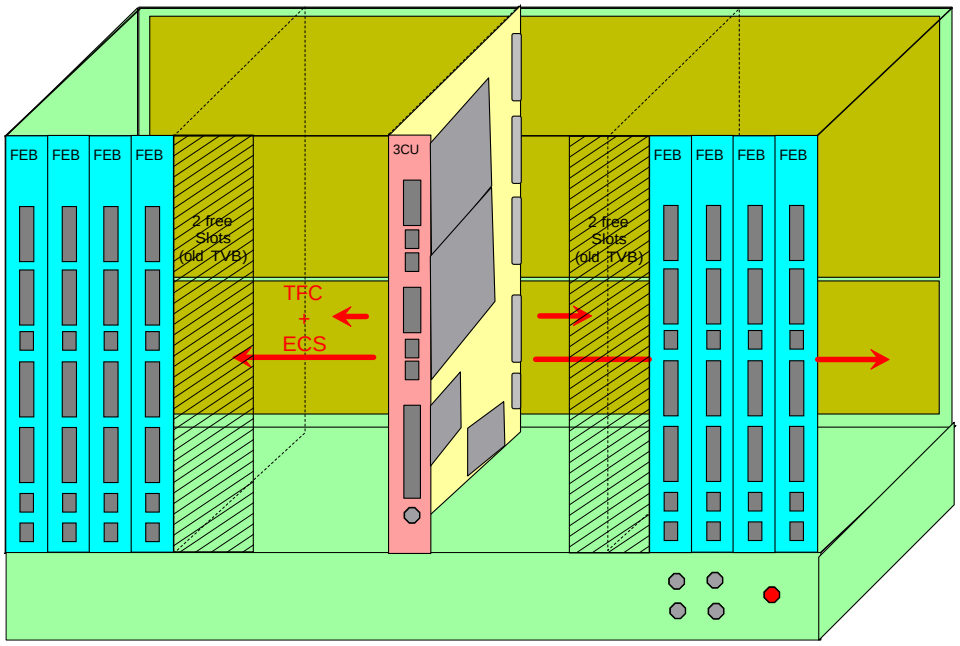

Figure 2: Schematic of the calorimeter crate.

2 General description

The main role of the 3CU is to receive the GBT frame through the optical link and to extract the information which is needed by the FEBs inside a same crate: the 40 MHz clock, the Time Fast Control (TFC) commands and Experiment Control System (ECS). Figure 3 shows a picture of the 3CU. The various parts of the board are clearly identified. The board contains :

- A Versatile Link Transceiver / Receiver (VTRx), for the reception and transmission to the SOL40 board.
- A radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links (GBTX).
- A GBT-SCA ASIC, part of the GBT chip-set, to distribute control and monitoring signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters.
- A Microsemi FPGA (IGLOO2 family) who is in charge of the processing on the 3CU.

Following the clock and TFC command (or from left to right on the picture), first the 3CU receives the clock and the TFC command through the optical transmitter (VTRx)

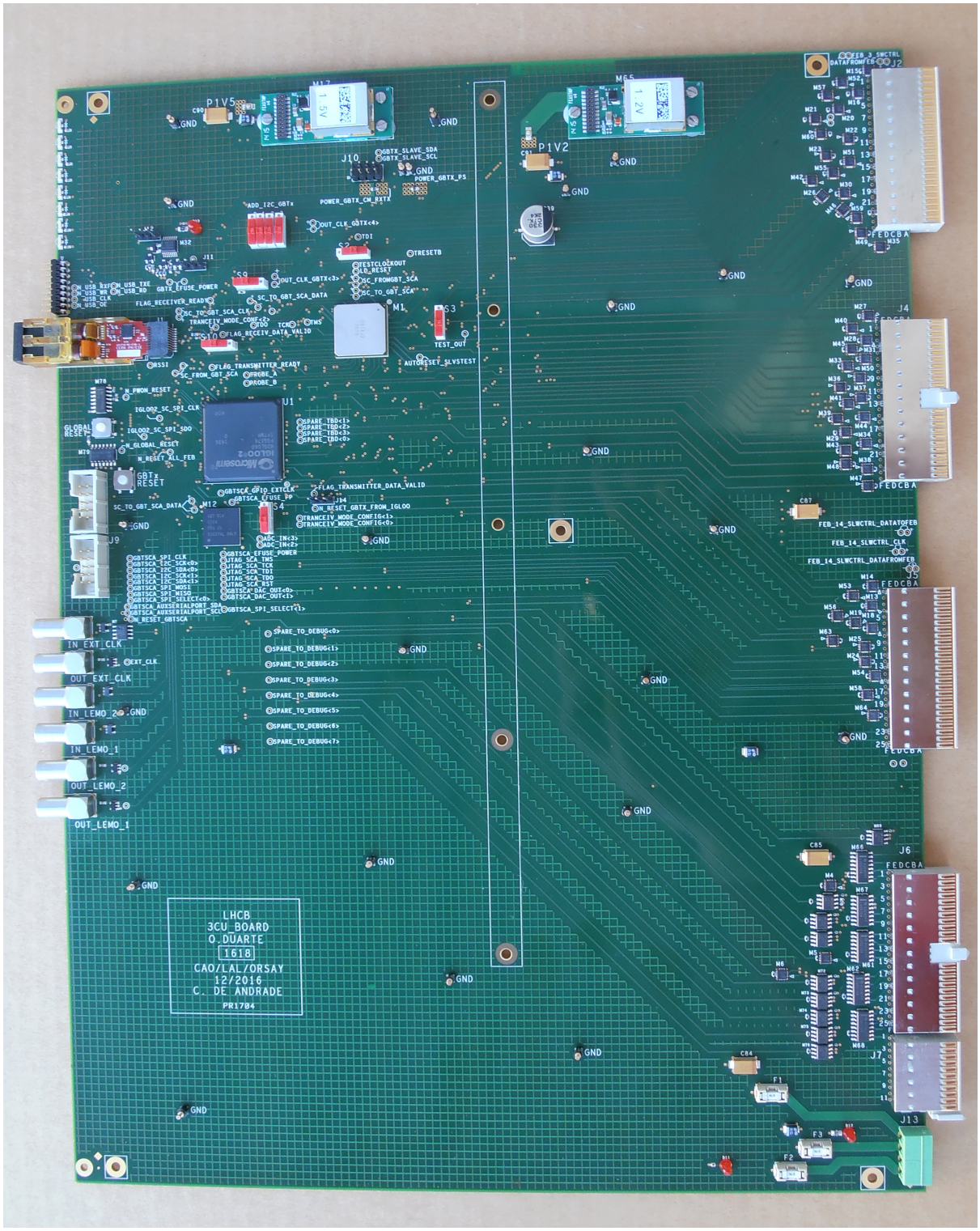

Figure 3: 3CU board.

and decoding inside the GBTX. After processing (inside IGLOO2), the board transmits through the 3U backplane these signals to all the FEB inside the same crate. The FEB are protected by delatchers which detect any current increase that could be due for example, to a Single Event Latchup (SEL). The 3CU board is in charge to monitor the delaching

status of all FEBs inside the same crate.
Most of the components that will be used on the 3CU are common to the FEB. A complete study of the radiation hardness of the components of the FEB can be found in Ref. [1].

3 Global architecture of the 3CU

Figure: 4 displays a picture of the global architecture of the 3CU board. In this section is presented a detailed of description of the path of commands on the board as well as the different blocks functionalities. The main blocs of the board are:

- The Versatile Transceiver (VTRx), a bi-directional module composed of both optical transmitter and receiver and a GBTX chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links. Logically the link provides three distinct data paths for Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information. In practice, the three logical paths do not need to be physically separated and are merged on a single optical link.

- The GBT-SCA ASIC, its purpose is to distribute control and monitoring signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters. It provides various user-configurable interfaces (I2C, SPI, GPIO used on the 3CU board).

- The Microsemi IGLOO2 family FPGA. It is mainly in charge of the processing of the TFC command and the control of the 3CU board.

- One USB interface mezzanine for the debugging of the 3CU card. This mezzanine is not radiation tolerant and will be used only for the debugging of the board.

3.1 Clock tree

The GBT receive the master clock through the optical link and it has 8 output programmable clock in SLVS (Scalable Low Voltage Standard) standard. We will used 4 among 8 clock output of the GBT to distribute the clock to all the FEB inside the same crate. Figure: 5 shows a picture of the clock tree on 3CU. We buffered and split the clock before transmit to all FEB through 6U backplane in LVDS standard. From the 3CU, the LHC clock is distributed individually towards all slots through point to point connection. With the clock tree of the 3CU, we can adjust if its necessary independently half crate FEBs and FPGA clock. Moreover for the debugging, we can used an external clock.

3.2 GBT - frame format

The 120-bit "GBT frame format", sketched in Figure: 6, is transmitted during a single LHC bunch crossing interval (25 ns), resulting in a line rate of 4.8 Gb/s. A complete description of the GBT system can be found in Ref: [2]. Four bits are used for the frame Header (H) and 32 are used for Forward Error Correction (FEC). This leaves a total of 84 bits for data transmission corresponding to a user bandwidth of 3.36 Gb/s. Of the 84-bits, 4 are always reserved for Slow Control information (Internal Control (IC) and External

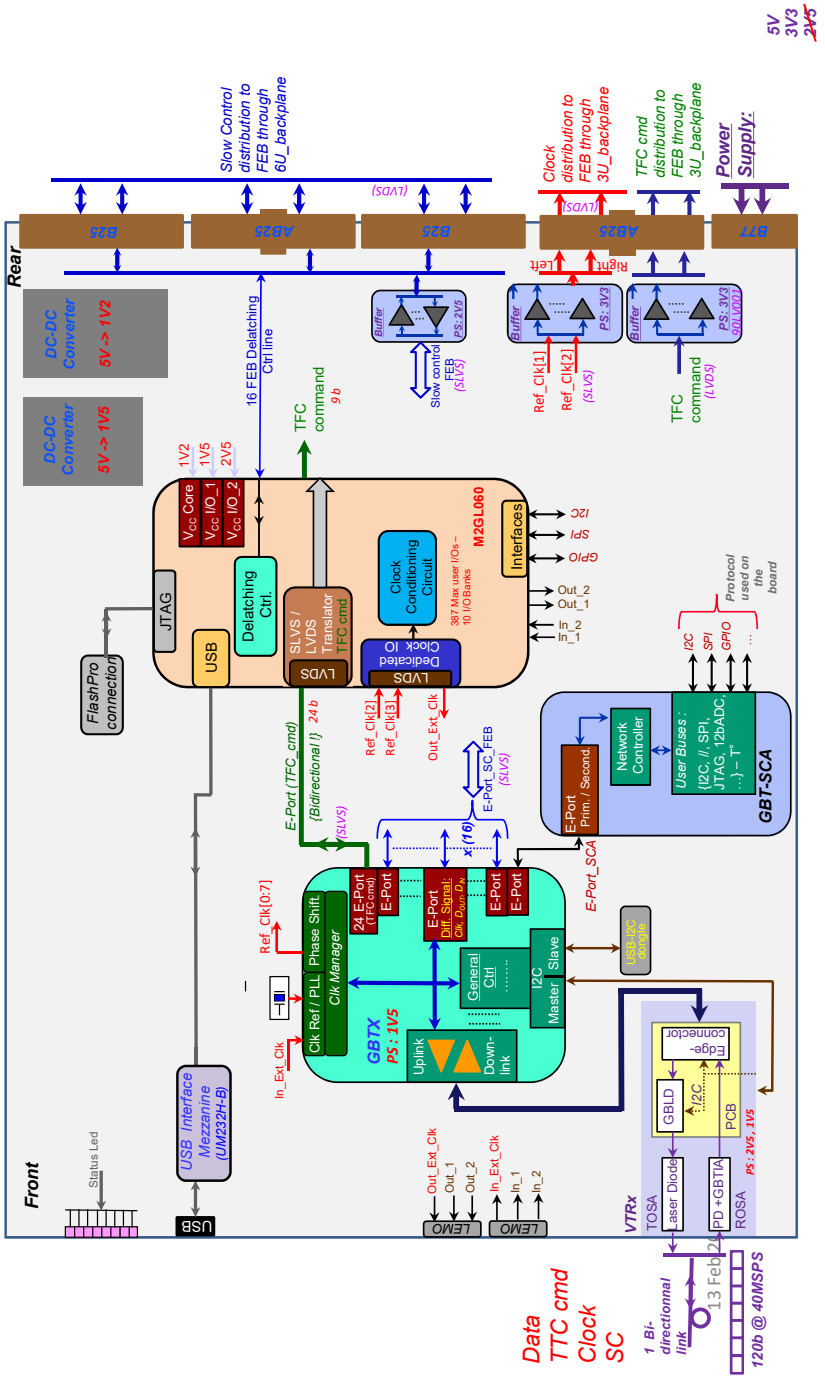

Figure 4: Global architecture of the 3CU.

Control (EC) fields), leaving 80-bits for user Data (D) transmission. The "D" and EC fields use is not pre-assigned and can be used indistinguishably for Data Acquisition (DAQ), Timing Trigger & Control (TTC) and Experiment Control (EC) applications.

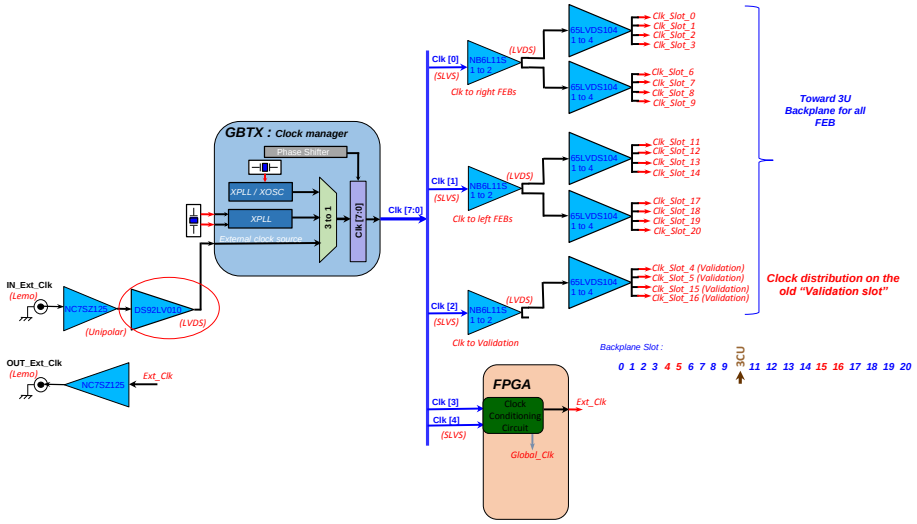

Figure 5: Clock tree distribution.

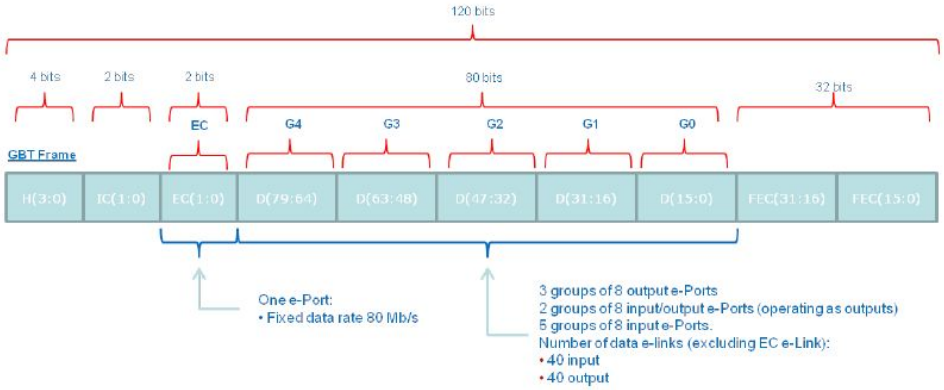

Figure 6: GBT frame.

3.3 TFC/ECS interface to the front-end

Rapid and synchronous controls are provided by the GBT link. Every 25 ns a frame is sent to every front-end device of the detector. A detailed description of the encoding of the TFC commands can be found in Ref [3], [4]. The link also provides the local 40 MHz used by the 3CU, that will distribute it to the front-end boards. The structure of the frame is show in Table: 1. To be able to accomodate the requirements of the various sub-detectors, the bandwidth available in the GBT for transmitting the ECS and the TFC is large. In the case of the calorimeter the following commands will be kept and sent to the FEB: The BX reset (1 bit), FE reset (1 bit), an or of Header only (1 bit) and BX veto (1 bit), Calibration (1 bit), Snapshot (1 bit), Synch (1 bit).

47... 25	23	21	19	17... 11	9	7	5	3	1
BXID(11..,0)	Reserve	Synch	Snapshot	Calibration Type (3...0)	BX Veto	NZS mode	Header Only	FE Reset	BXID Reset

Table 1: TFC frame.

3.4 FPGA

We used a Microsemi IGLOO2 family Flash based FPGA (it will retain the configuration data even after power down). We have integrated on the 3CU a FPGA (M2GL060) with 387 users IOs, 1826 K bits of RAM and 56520 logic elements, this is the medium- high of the size of the FPGA family matrix. This FPGA is mainly in charge of the processing of the TFC command from the GBT and monitoring of the delatching control line from the FEBs through the 6U backplane.

3.5 Slow control

The GBT communication is totally transparent to the slow control protocol. The GBT encodes slow control packets in the counting room, carries it on the optic fibres interlaced with the rest of the traffic, and it delivers the SCA packets unmodified to the GBT-SCA in the embedded system. The GBT-SCA ASIC [5] is a part of the GBT chip-set, has the purpose to distribute control and monitoring signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters. Inside the GBT frame, a 4-bit slow control field is dedicated to the execution of routine and control operations that do not necessarily require precise timing. Two bits are reserved for the Internal Control (IC) of the GBTX itself while the other two implement a fixed bandwidth port for an external slow control (EC) port.

The GBTX is connected to the GBT-SCA through a dedicated E-Port. With the SCA integrated on the 3CU board we have the possibility to use the several interfaces:

- I2C master serial bus;
- SPI master serial bus;
- JTAG master serial bus;
- PIA (Parallel Interface Adapter), 32 General Purpose digital I/O lines.

The 3CU is also in charge of transmitting the slow control to the 16 FEB through the backplane.

3.6 Fault

The FEBs are protected by delatchers of type MAX869 which detect any current increase that could be due, for example, to a Single Event Latchup (SEL). If such a situation occurs the current is switched off (during a few ms) and on again. The delatching is controlled by the 3CU. The 16 lines of all the FEBs of the 16 slots in the crate are connected to 16 pins of the IGLO2 FPGA which records any fault transition on those lines into its status register. The status register may be regularly checked in order to verify that no FEB has had a SEL and if yes the corresponding FEB may be reloaded through ECS. An other functionality of the fault system is to pull down the same line at the delatcher

and this will switch the current until the line is released. The delatchers that see the line pulled down will switch off the current until the line is released. The line may be maintained down to have a prolonged stop of a board. The mechanism would be used in case of problems with the electronics and is triggered by a ECS command and the writing in a 3CU register through ECS.

3.7 Power supplies

Inside the calorimeter crate we have four power supplies available: +7V[1], +5V, +3.3 V and +2.5V. As shown on Figures: 7 and 8, on the 3CU board we need: +5V, +3.3 V, +2.5V, +1.5V, +1.2V. We obtain the first three directly from the 3U backplane, and to build the last two we used a radiation and magnetic field tolerant DC/DC converter module from CERN.

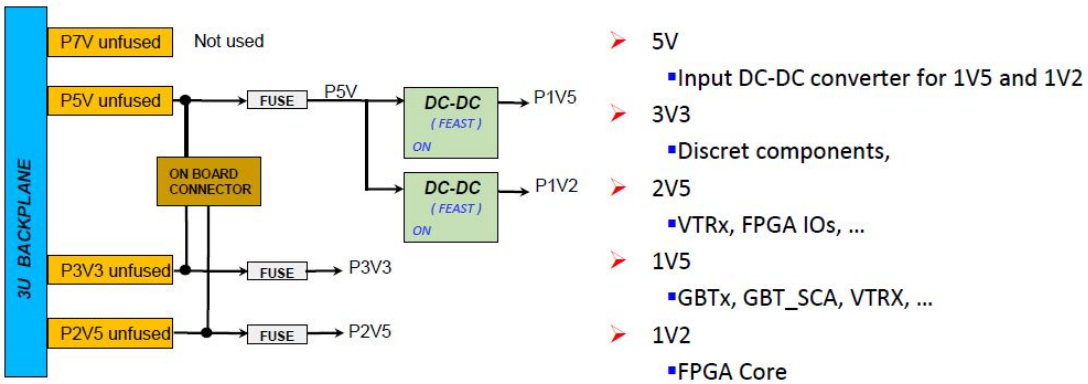

Figure 7: Power tree.

[1]Tests on the FEB prototype indicated that +6V is enough at this point, it will therefore be used as default in the future.

3.8 Backplane connections

The 3CU card is connected to the 3U and 6U backplane through two 2mm Hard Metric connector (125 and 55 points) for the 3U backplane and three 2mm Hard Metric connector (of 125 points) for the 6U backplane see Figure: 9.

3U Backplane connections: The 55 points connectors is dedicated to the power supply distribution, while the 125 points distribute the clock to all FEBs (differential point to point connection dark blue), the TFC command (differential point to point connection light blue).

6U Backplane connections: The three 125 points connector are used to :

- Transmit the Slow Control information to all the FEB (3 point to point differentials pairs between each FEB and the 3CU light blue surrounded by red).
- Read the 8 bits of crate Id from the backplane (red).
- Control and command the delatching line (point to point connection between each FEB and 3CU.

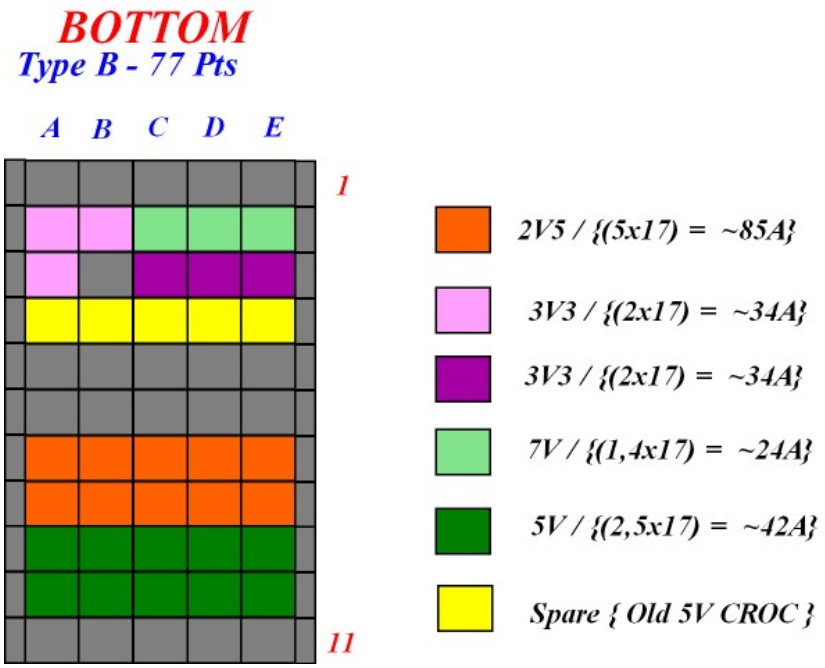

Figure 8: Backplane - Power supply.

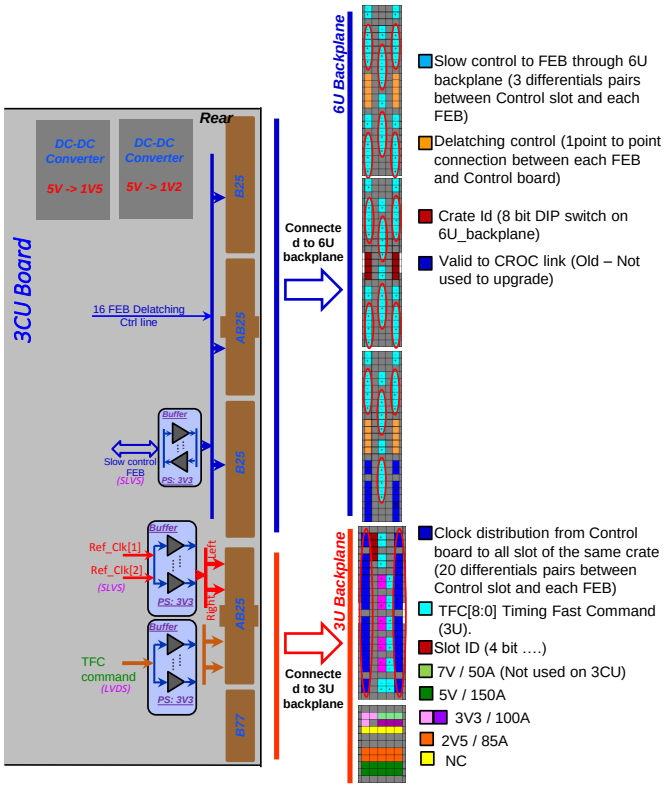

Figure 9: Rear connections of the 3CU.

References

[1] The LHCb Collaboration, The A-team , *FEB*, "Reference-Number".

[2] CERN, CERN people, *GBTX Manual"*, "Reference-Number".

[3] LHCb collaboration, K. Wyllie et al. , *Electronics architecture of the LHCb Upgrade*, LHCb-PUB-2011-001.

[4] LHCb collaboration, F. Alessio et al. , *System-level specifications of the timing and fast control system of the LHCb upgrade*, "LHCb-PUB-2012-001".

[5] CERN, S. Bonacini et al. , *GBT-SA User manual, the slow control adapter basic for the GBT system"*, "Reference-Number".