3CU (Calorimeter Crate Controller for the Upgrade) Production Readiness Review

Introduction

- Short reminder (TFC system, Calorimeter crate)

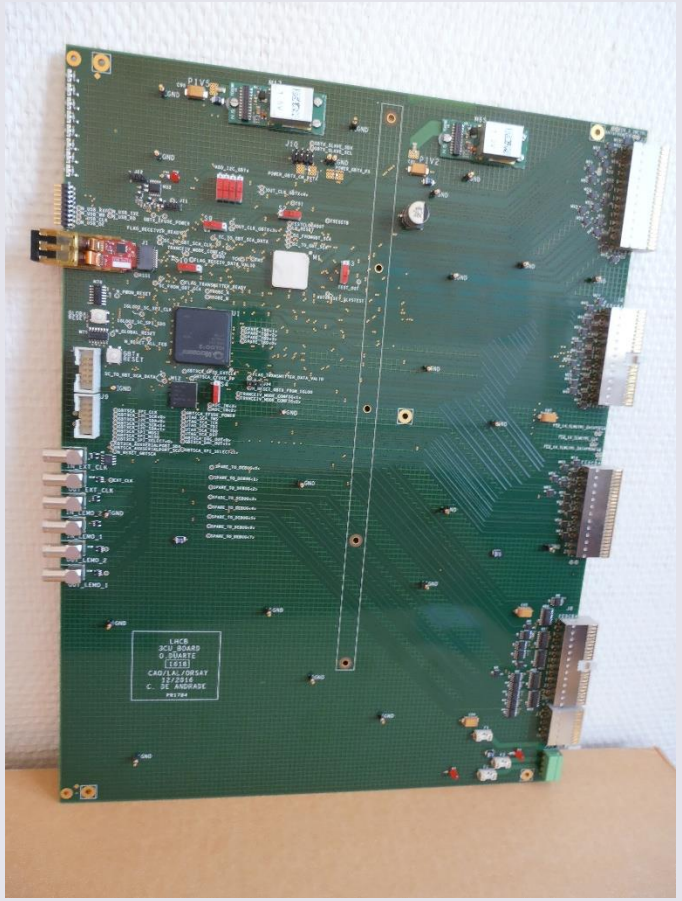
General description

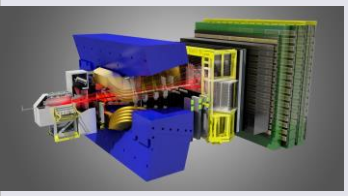
- Main role - main part of the board - overview

Architecture

- Global architecture - clock tree - GBT frame format - Slow Control - Delatching control - IGLOO2 FPGA - Power supplies and power tree - Rear connections - Fimware architecture

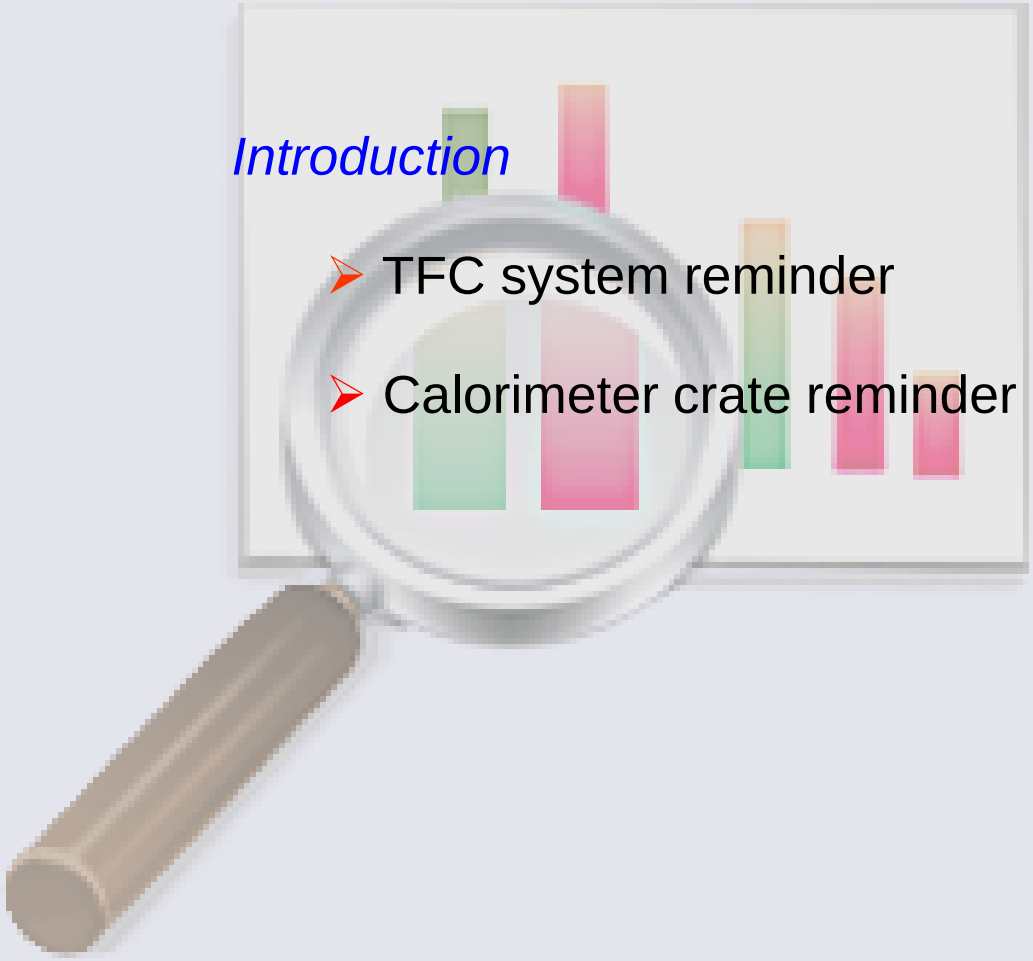
Conclusion





On behalf of the Orsay group

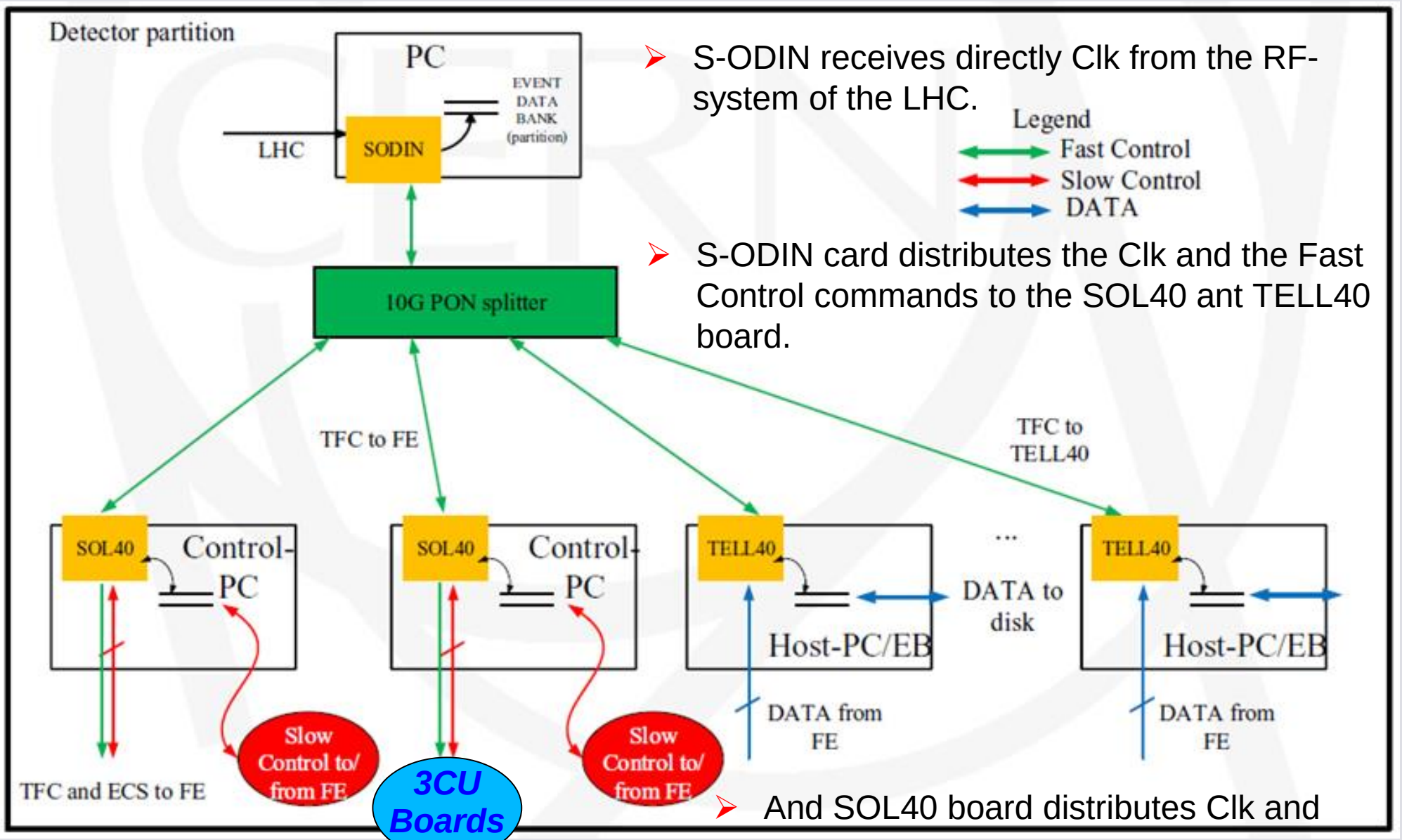
PRR 3CU board



Introduction

- TFC system reminder
- Calorimeter crate reminder

Introduction : TFC system reminder

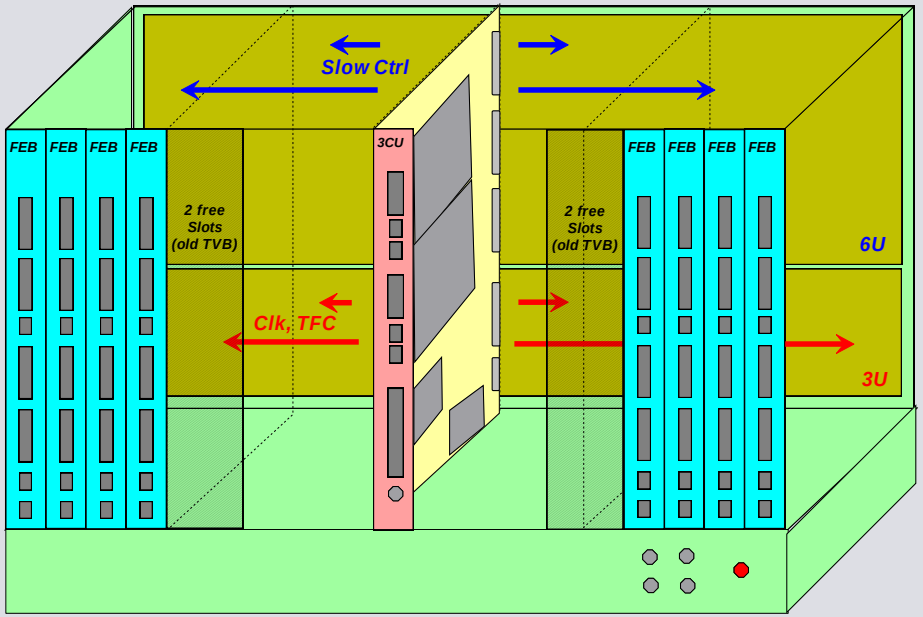


- S-ODIN receives directly Clk from the RF-system of the LHC.
- S-ODIN card distributes the Clk and the Fast Control commands to the SOL40 ant TELL40 board.
- And SOL40 board distributes Clk and Fast Control command to the 3CU board.

F. Alessio Schematic

Introduction : Calorimeter crate reminder

- **Front-end crate** with same backplanes and power supply
  - 3U ⇨ power supply, clock distribution, …
  - 6U ⇨ links between boards inside the same crate.
  - New Front-end board with optical link DAQ and LLT.
  - New Control Board (3CU).
  - Remove TVB.



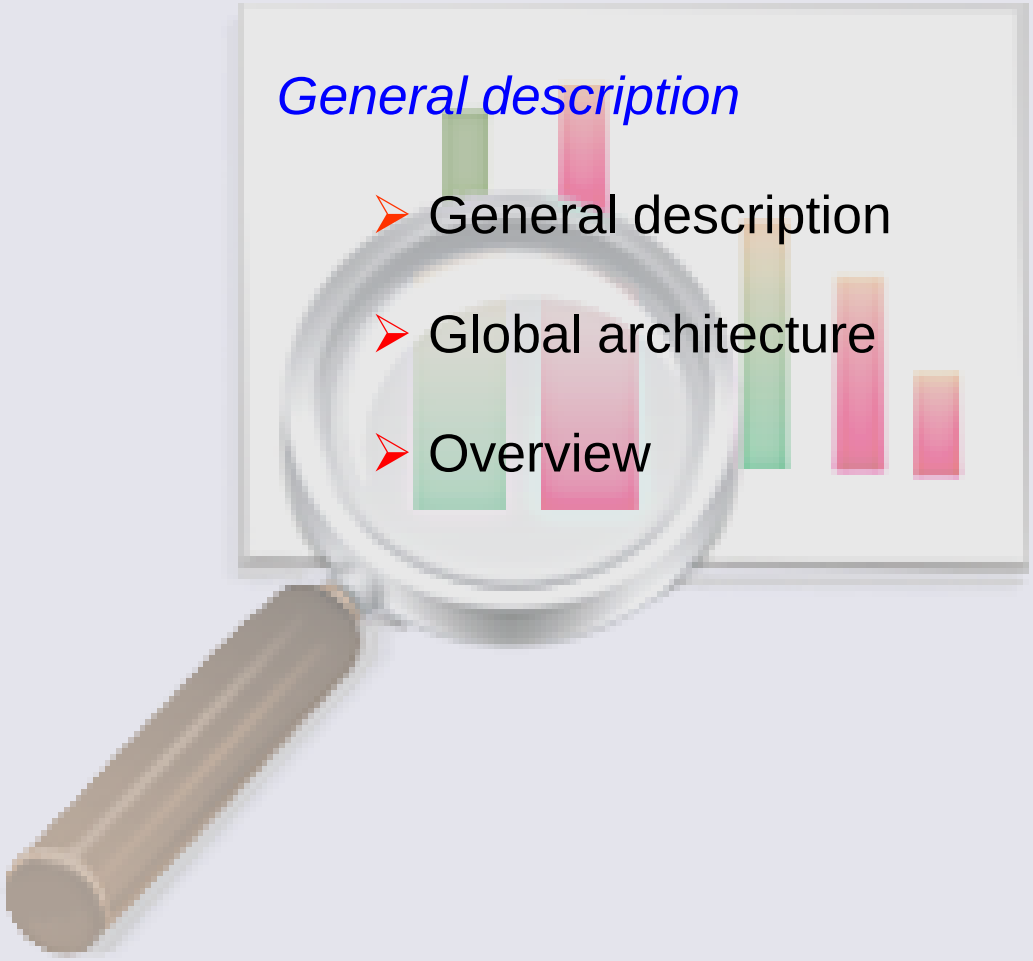
- Calorimeter crate controller **board (3CU)**

Ensure signal distribution inside Front-end crate

  - Clock distribution from the 3CU to all front-end board inside the same crate through 3U backplane.
  - Slow control through 6U backplane
  - Fast command (BxId Reset, FE Reset, …) through 3U backplane

- Crate Power supply
  - Reused Marathon equipment

PRR 3CU board



General description

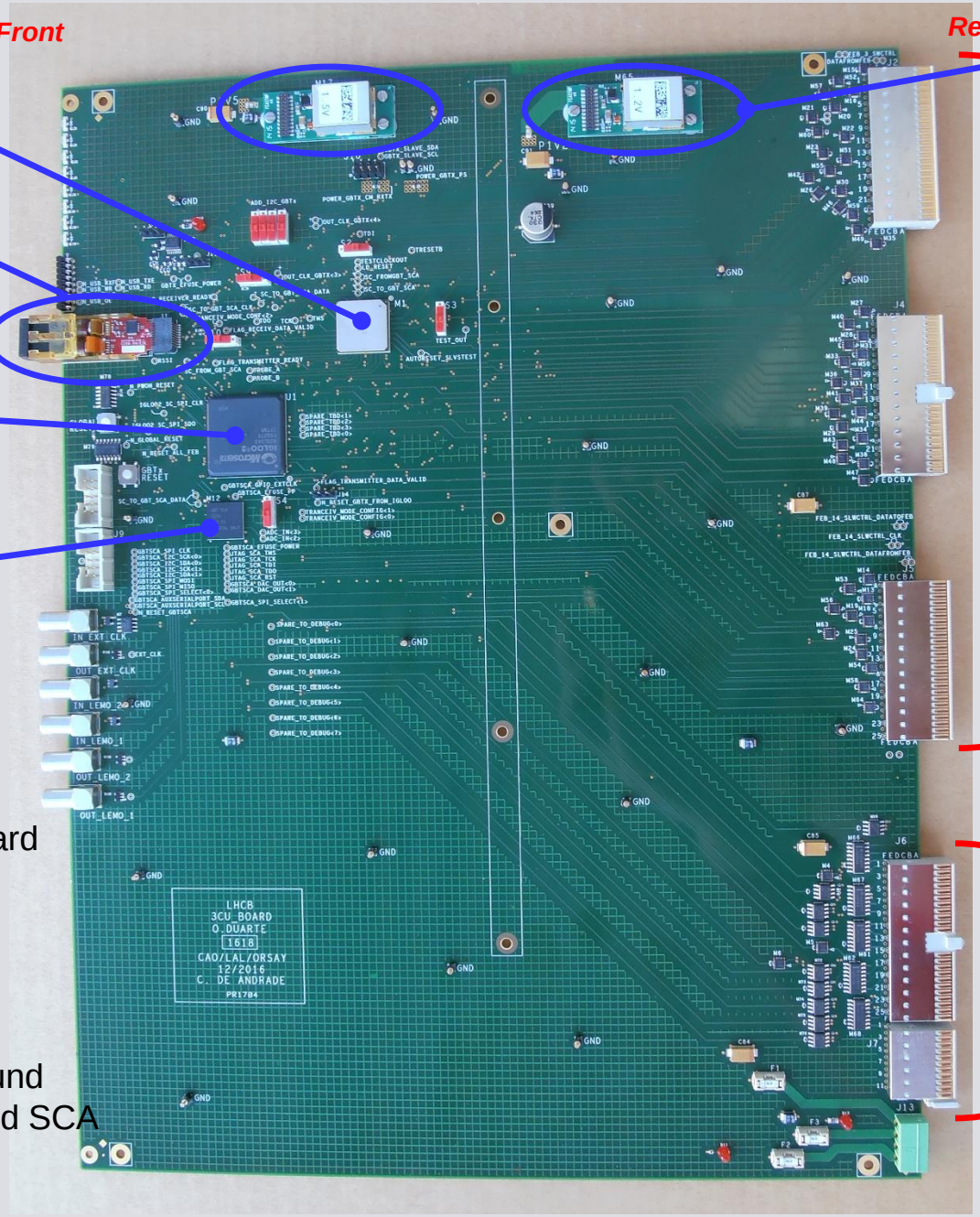
- General description
- Global architecture
- Overview

3CU : General description

- 3CU main role:
  - Receive the GBT frame through the optical link.
  - Extract the information needed by the FEBs (inside the same crate)
    - 40 Mhz Clock
    - Time Fast Control (TFC) commands
    - Experiment Control System (ECS)

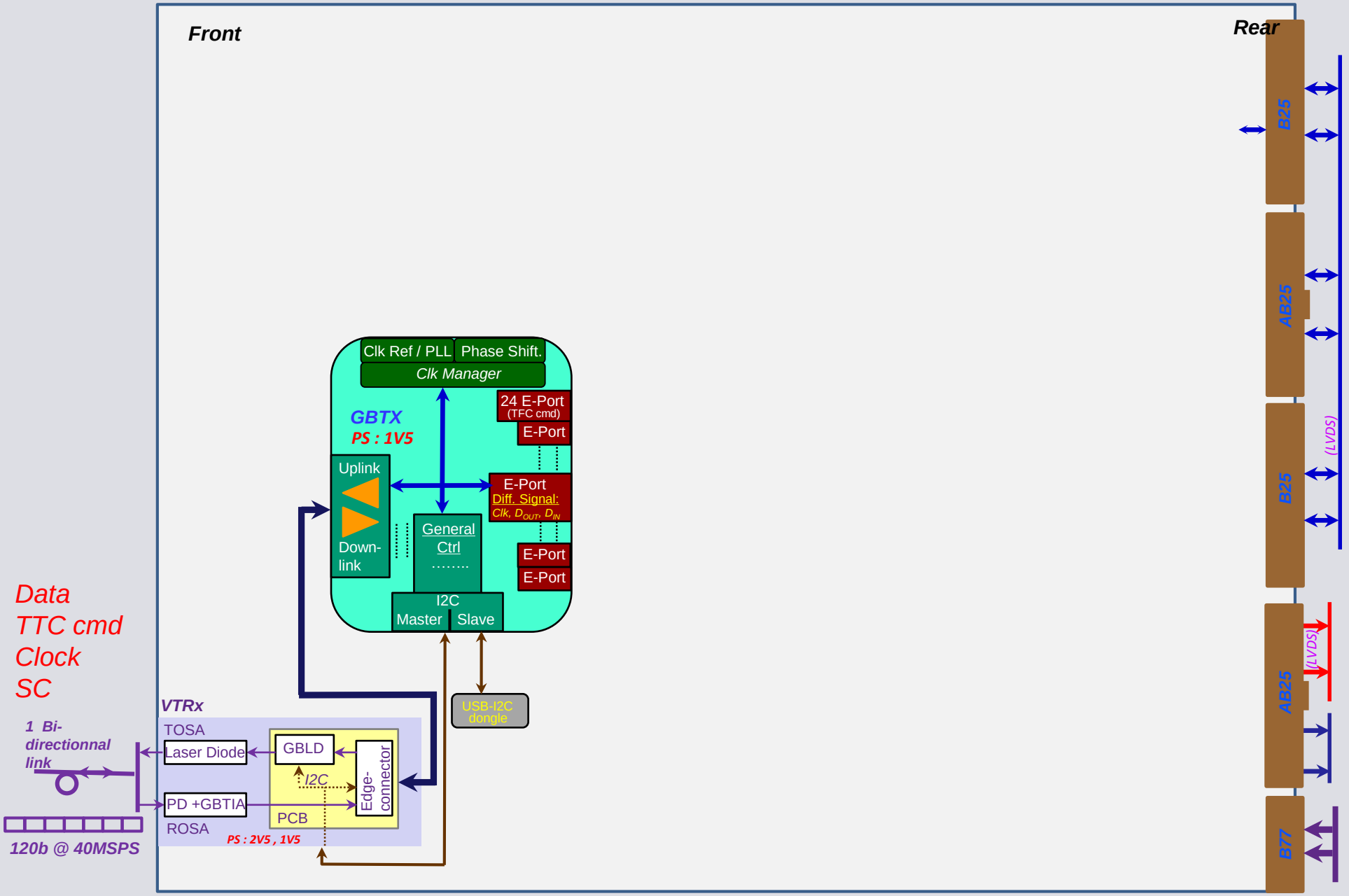
- Main part of the board:
  - A Versatile Transceiver (VTRx), a bi-directional module composed of both optical transmitter and receiver.
  - A GBTx chip that can be used to implement multipurpose high speed bidirectional optical link.
  - A GBT-SCA ASIC, part of GBT chip-set to distribute the Slow Control (SC) information on the board.
  - A Microsemi FPGA (IGLOO2), in charge of the processing on the 3CU.

General description: overview

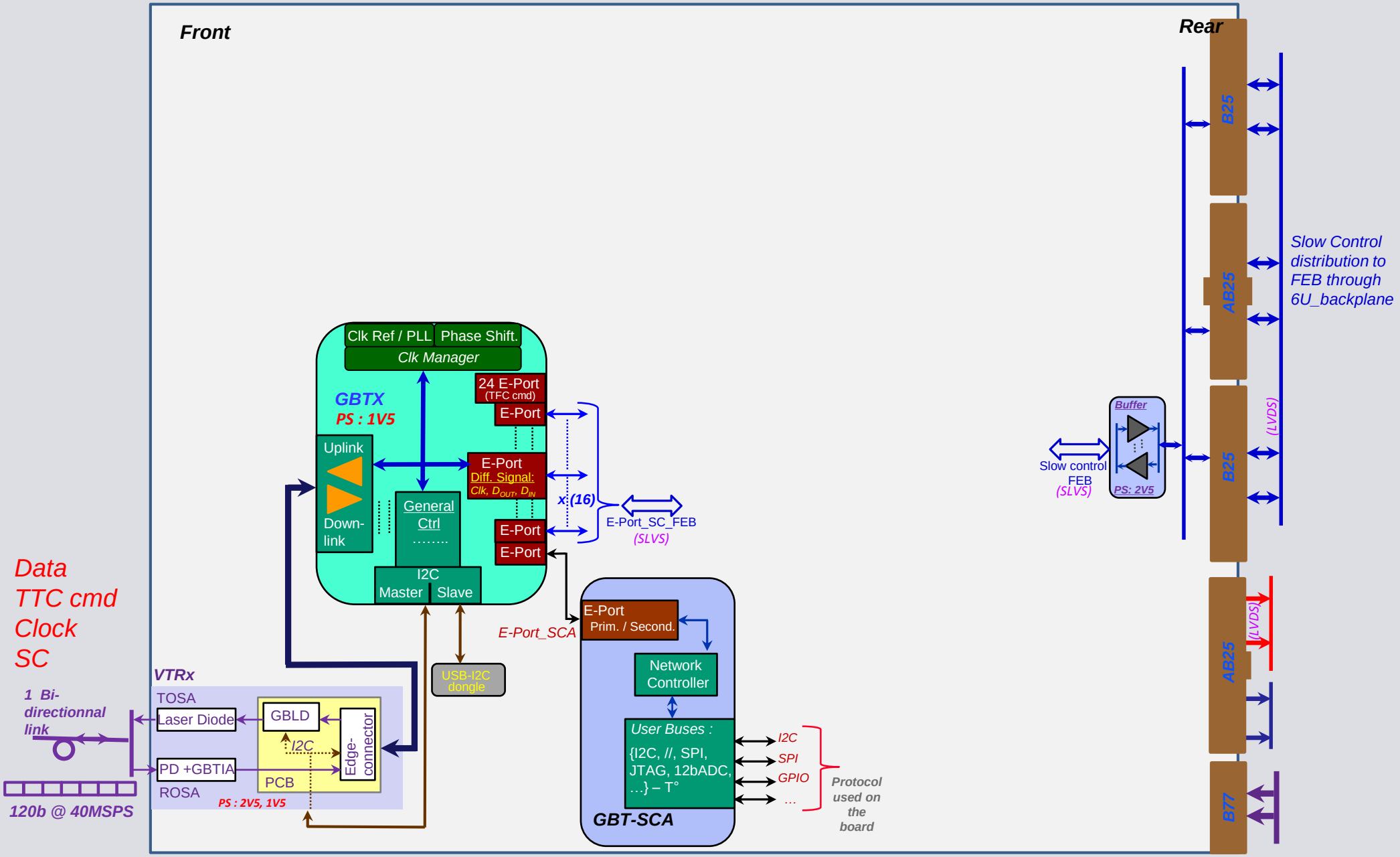


- 3CU board:
  - 9U / 280 mm VME board
  - Thickness 2.4 mm
  - Components 999 / Connections 5115
  - 12 layers
  - Routing very tight around IGLOO2 and GBTx and SCA

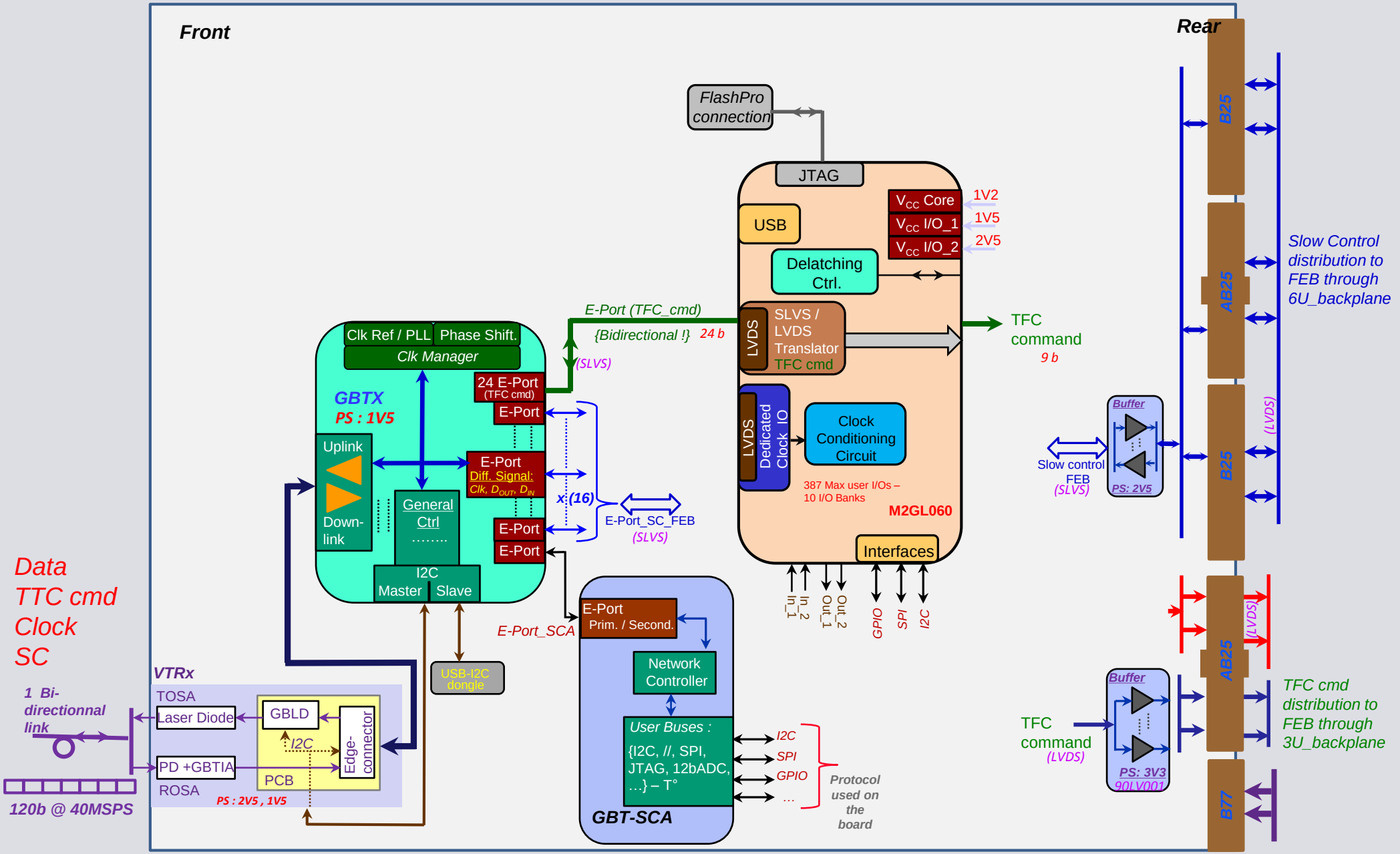
3CU Board : Global architecture



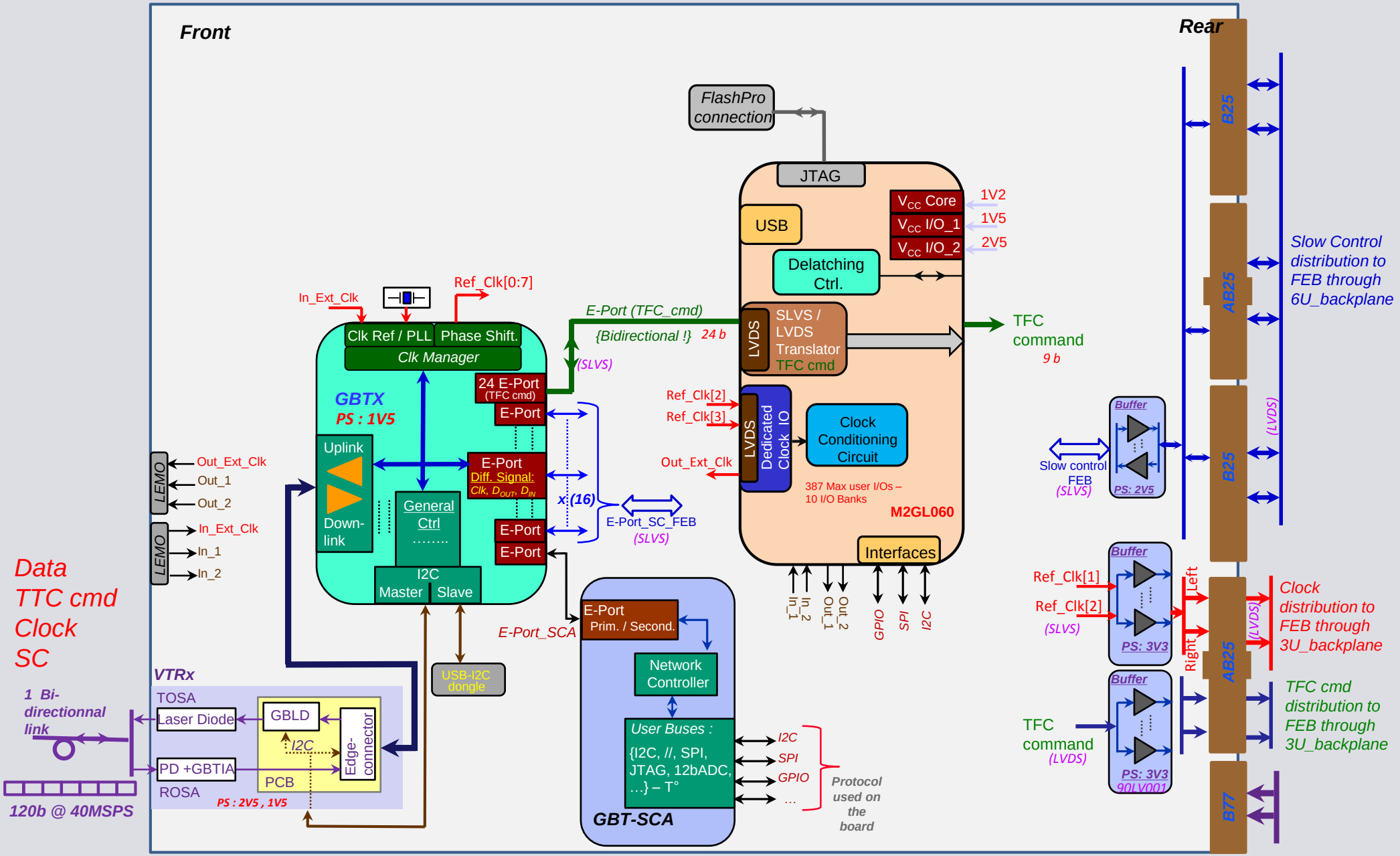
3CU Board : Global architecture



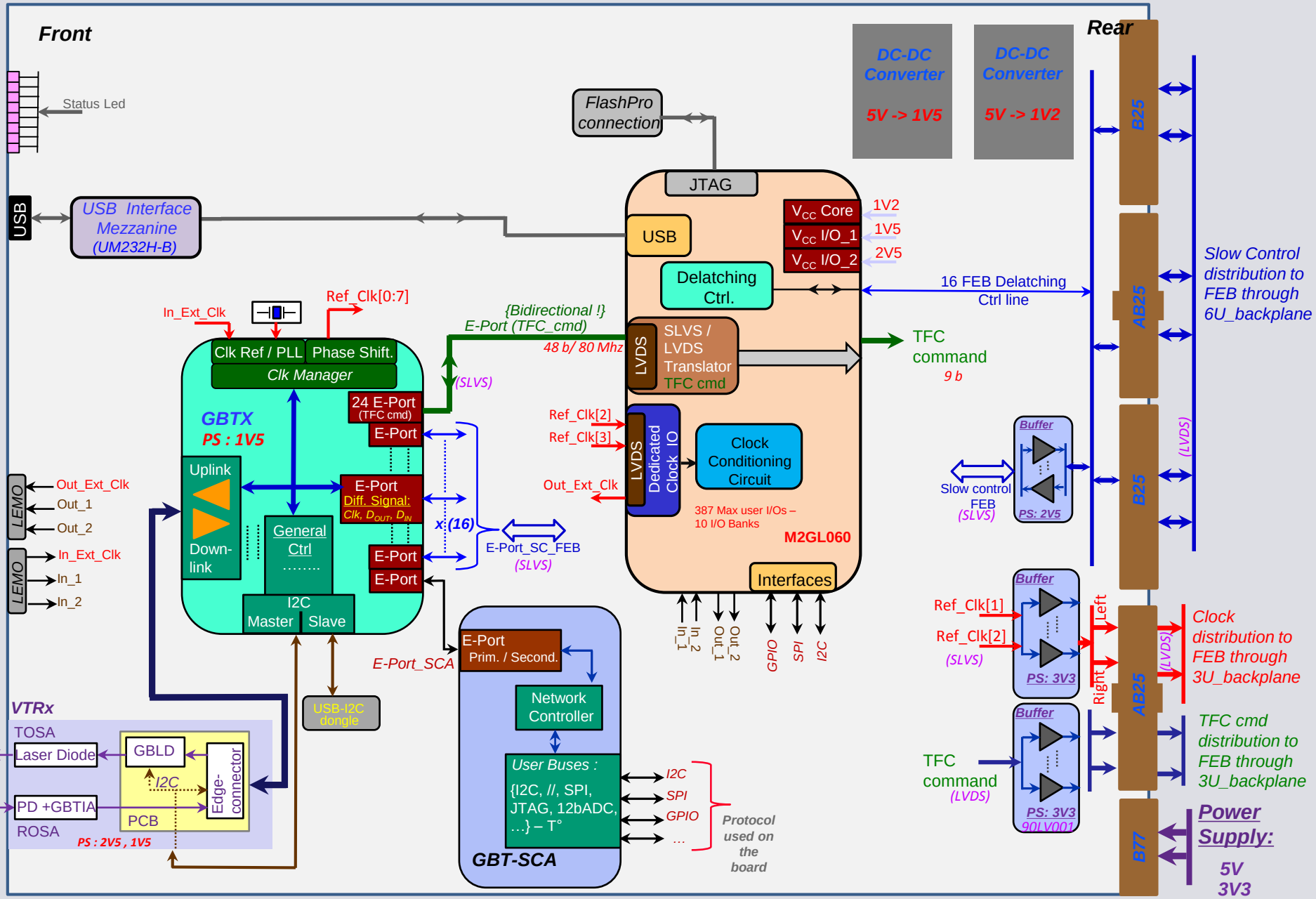
3CU Board : Global architecture



3CU Board : Global architecture



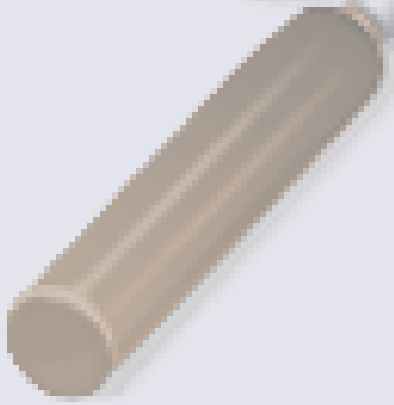
3CU Board : Global architecture



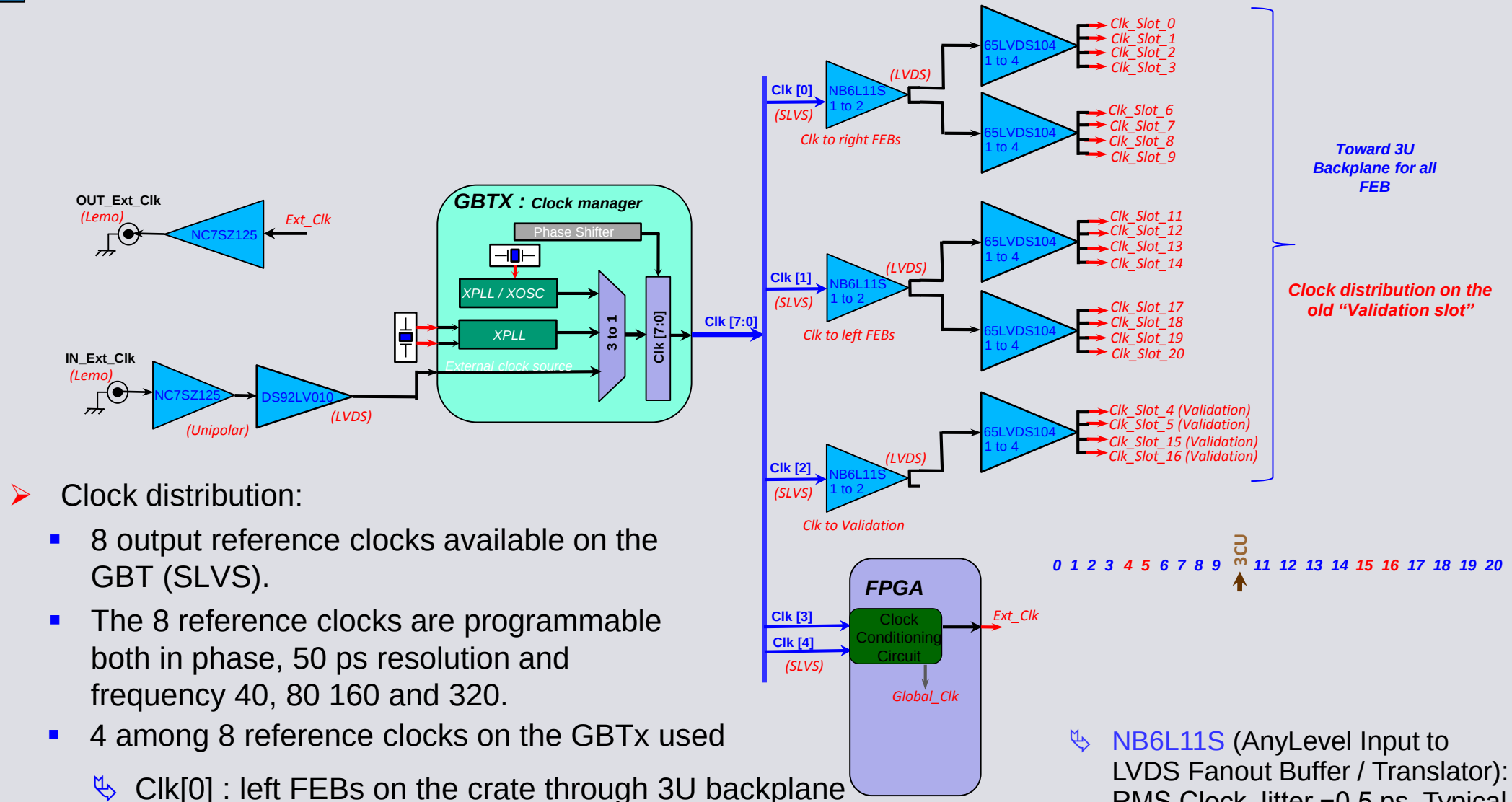
PRR 3CU board

Architecture of the board

- Clock tree
- GBT frame
- Slow control
- Delatching control
- IGLOO2 FPGA
- Power supplies and power tree
- Rear connections
- Firmware architecture



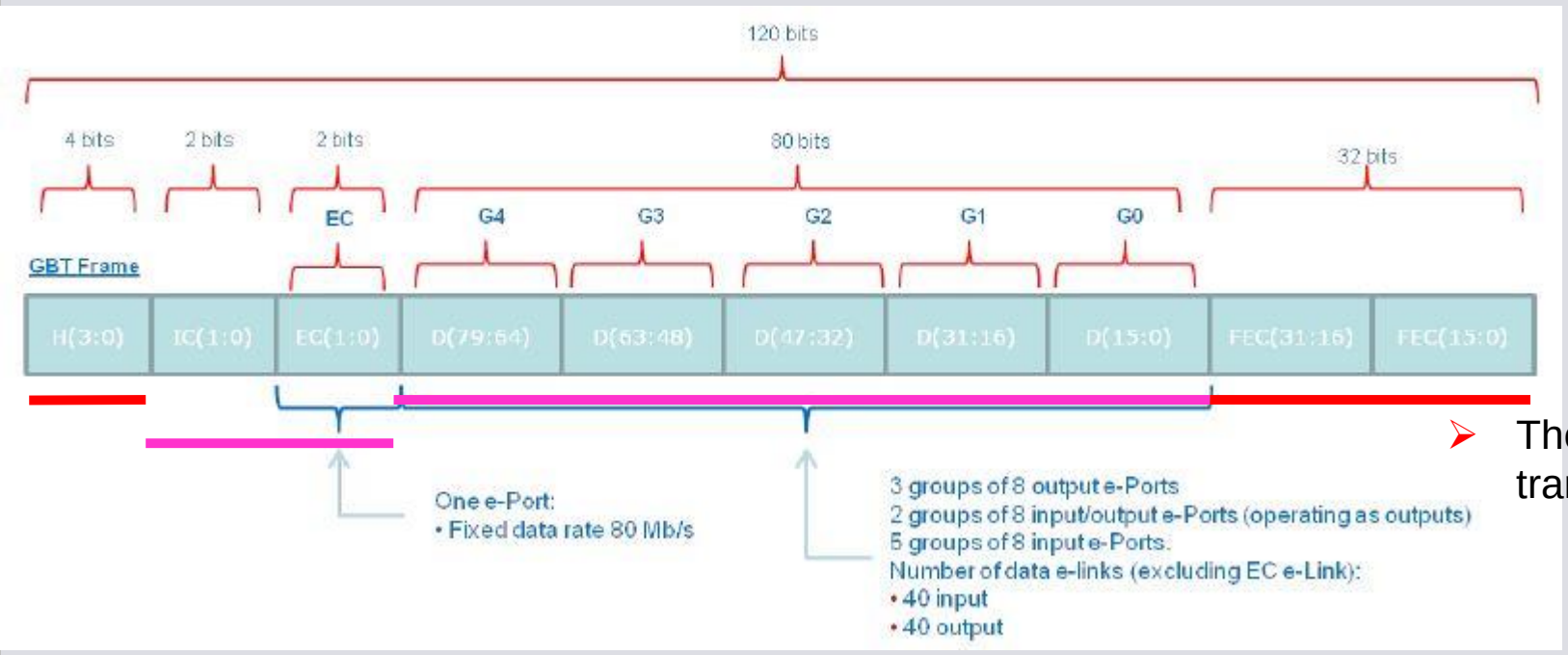
3CU Board : Clock tree



- Clock distribution:
  - 8 output reference clocks available on the GBT (SLVS).
  - The 8 reference clocks are programmable both in phase, 50 ps resolution and frequency 40, 80 160 and 320.
  - 4 among 8 reference clocks on the GBTx used
    - Clk[0] : left FEBs on the crate through 3U backplane
    - Clk[1] : right FEBs on the crate through 3U backplane
    - Clk[2] : Spare (Old validation slot)
    - Clk[3], Clk[4] : IGLOO2 Clock input (one should be enough !)

- NB6L11S (AnyLevel Input to LVDS Fanout Buffer / Translator): RMS Clock Jitter −0.5 ps, Typical
- SN65LVDS104 (1:4 LVDS Clock Fanout Buffer) : already used on the CROC for the clk distribution

3CU Board : GBT frame

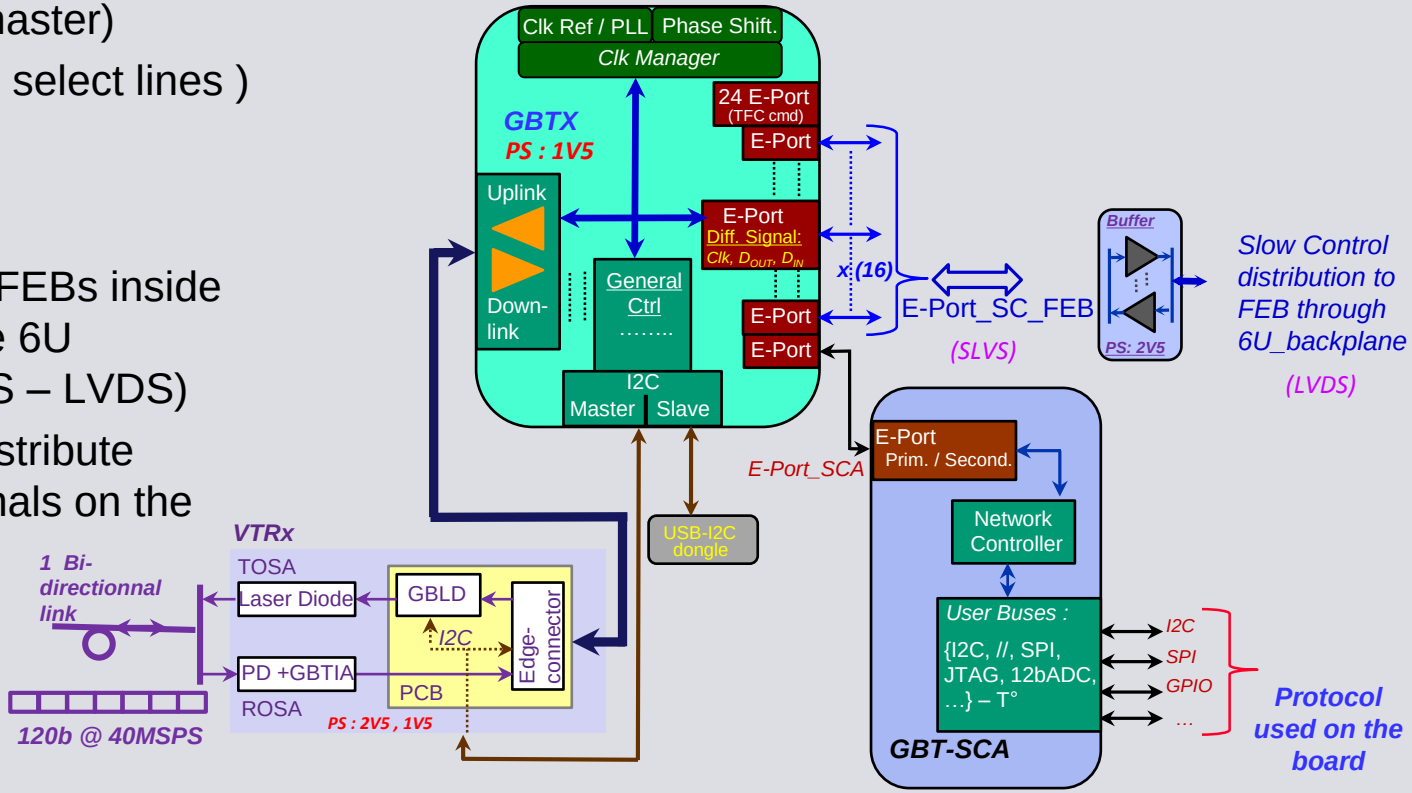


- The 120-bit “GBT frame” is transmitted every 25 ns

- GBT frame format:
  - 4 bits for the frame Header
  - 32 for the FEC (Forward Error Correction)
  - This leaves 84 bit for data transmission
    - 4 bit for Slow Control information Internal Control (IC) and External Control (EC) field
    - 80 bit for user Data (D) transmission
    - “D” and “EC” fields is not pre-assigned and can be used indistinctly for Data Acquisition (DAQ), Timing Trigger & Control (TTC) and Experiment Control (EC) application
- 3CU extract and process (if necessary) the TTC and EC to transmit them through backplane to the FEBs.

3CU Board : Slow Control (SC)

- GBT encodes SC packets in the counting room
- Transmit through optical fiber SC information interlaced with the rest of the traffic (DAQ, TTC, …)
- Delivers the SCA packet unmodified to the GBT-SCA
- GBT-SCA provides various user-configurable interfaces capable to perform simultaneous operations
  - I2C (16 independent I2C master)
  - SPI (with 8 individual slave select lines)
  - GPIO (32 digital IO lines)
- 3CU board
  - Transmit the SC to the 16 FEBs inside the same crate through the 6U backplane (translator SLVS – LVDS)
  - Integrate a GBT-SCA to distribute control and monitoring signals on the 3CU

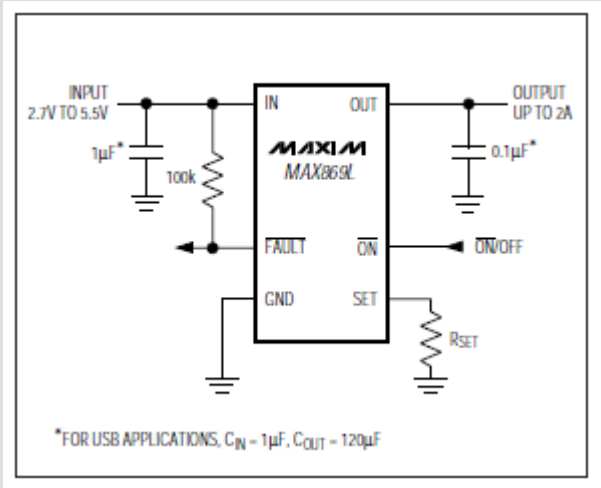


3CU Board : FEBs delatching control

- Each FEBs inside the crate are protected by delatchers (2A, Current-Limited switch) of type MAX 869
  - If Single Event Latchup (SEL) occurs the MAX869 switch OFF (during few ms) the FEB and ON again
  - The delatching is controlled by the 3CU one connection between each FEB and 3CU, 16 lines off the backplane)

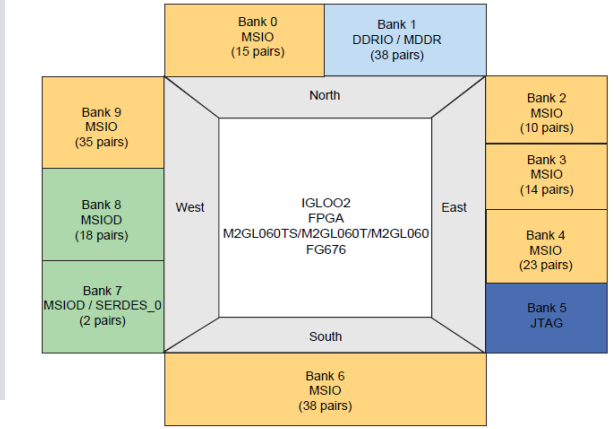
- On the 3CU
  - Each delatching control line is connected to the IGLOO2 (status register)
  - Status register regularly checked by the system, and if it necessary the FEB may be reloaded by ECS.

- Reused the same system of the CROC board with the IGLOO2



3CU Board : IGLOO2 FPGA

- Flexible IOs structure
  - Mixed voltages VCC_{IO_BANK} (1.2, 1.5, 1.8, 2.5, 3.3V)
  - Multistandard IOs



IGLOO2 FPGA Family

More Resources in Low Density Devices

Overview | Product Tables | Documentation | Design Resources | Ordering

Product Family

	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL060	M2GL090	M2GL150
Logic/DSP	Maximum Logic Elements (4LUT + DFF)*	6,060	12,084	27,696	56,340	56520	86,316	146,124
	Math Blocks (18x18)	11	22	34	72	72	84	240
	PLLs and CCCs	2						8
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FICs)	1			2			2
	Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (K Bytes)	128	256				512	
	LSRAM 18K Blocks	10	21	31	69	69	109	236
	uSRAM1K Blocks	11	22	34	72	72	112	240
	eSRAM (K Bytes)	64						
	Total RAM (K bits)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1x18			2x36	1x18	1x18	2x36
	SERDES Lanes	0	4		8	4	4	16
	PCIe End Points	0	1			2		4
User I/Os	MSIO (3.3V)	115	123	157	139	271	309	292
	MSIOD (2.5V)	28	40	40	62	40	40	106
	DDRIO (2.5V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), Automotive(T1/T2)*	C,I,T1,T2	C,I,M,T1,T2	C,I,M,T1,T2	C,I,M,T1,T2	C,I,M,T1,T2	C,I,M,T1,T2	C,I,M

* Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 Fabric UG for details

* Automotive grade is available only in VF256, VF400, FG484 and FG676 packages

Supported I/O Standards

SmartFusion2/IGLOO2 devices support the different I/O stan
standards can be configured using Libero SoC. Refer to the
Table 5-1 lists all the I/O standards supported for single-ende

Notes:

1. For M2GL060-FG676 device, SERDES block is not available in bank 7.

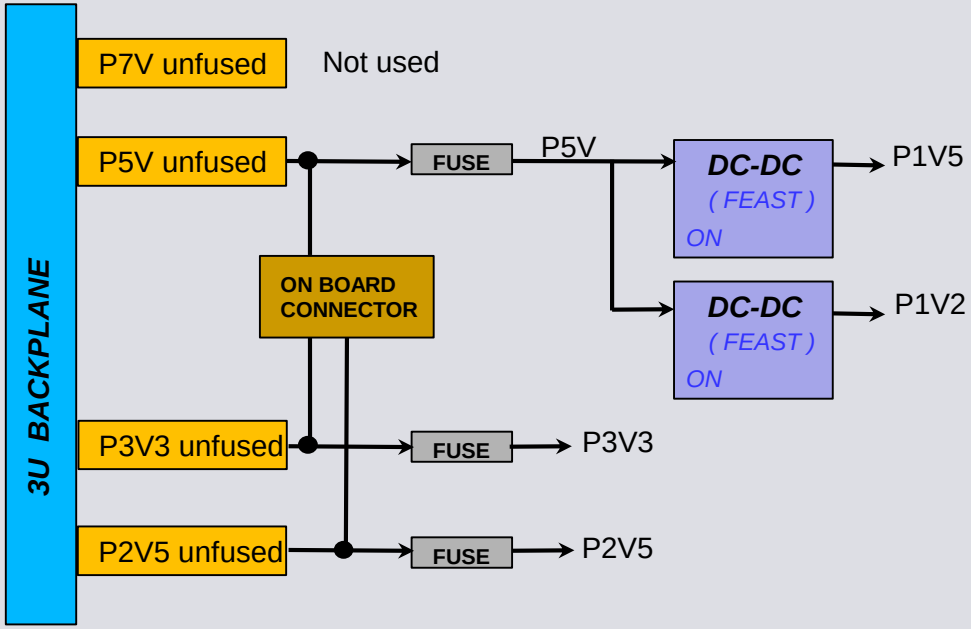
***Figure 4* • IGLOO2 M2GL060TS/ M2GL060T/M2GL060-FG676 I/O Bank Locations**

***Table 5-1* • Supported I/O Standards**

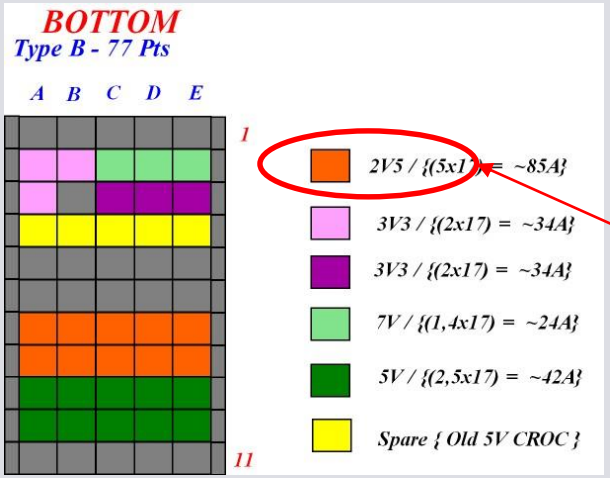
I/O Standards	Single-ended	Differential	MSIO (Max 3.3 V)	MSIOD (Max 2.5 V)	DDRIO (Max 2.5 V)
LVTTL	Yes	–	Yes	–	–
PCI	Yes	–	Yes	–	–
LVPECL (input only)	–	Yes	Yes	–	–
LVDS33	–	Yes	Yes	–	–
LVCMOS33	Yes	–	Yes	–	–
LVCMOS25	Yes	–	Yes	Yes	Yes
LVCMOS18	Yes	–	Yes	Yes	Yes
LVCMOS15	Yes	–	Yes	Yes	Yes
LVCMOS12	Yes	–	Yes	Yes	Yes
SSTL2I	Yes	Yes	Yes	Yes	Yes (DDR1)
SSTL2II	Yes	Yes	Yes	–	Yes (DDR1)
SSTL18I	Yes	Yes	–	–	Yes (DDR2)
SSTL18II	Yes	Yes	–	–	Yes (DDR2)
SSTL15I (only for I/Os used by MDDR/FDDR)	Yes	Yes	–	–	Yes (DDR3)
SSTL15II (only for I/Os used by MDDR/FDDR)	Yes	Yes	–	–	Yes (DDR3)
HSTLI	Yes	Yes	–	–	Yes
HSTLII	Yes	Yes	–	–	Yes
LVDS	–	Yes	Yes	Yes	–
RSDS	–	Yes	Yes	Yes	–
Mini LVDS	–	Yes	Yes	Yes	–
BUSLVDS	–	Yes	Yes	Yes (input only)	–
MLVDS	–	Yes	Yes	Yes (input only)	–
SUBLVDS (output only)	–	Yes	Yes	Yes	–

Note: For I/O pin names and bank assignments for different device packages, refer to the SmartFusion2/IGLOO2 Pin Descriptions document.

Power supplies and power tree

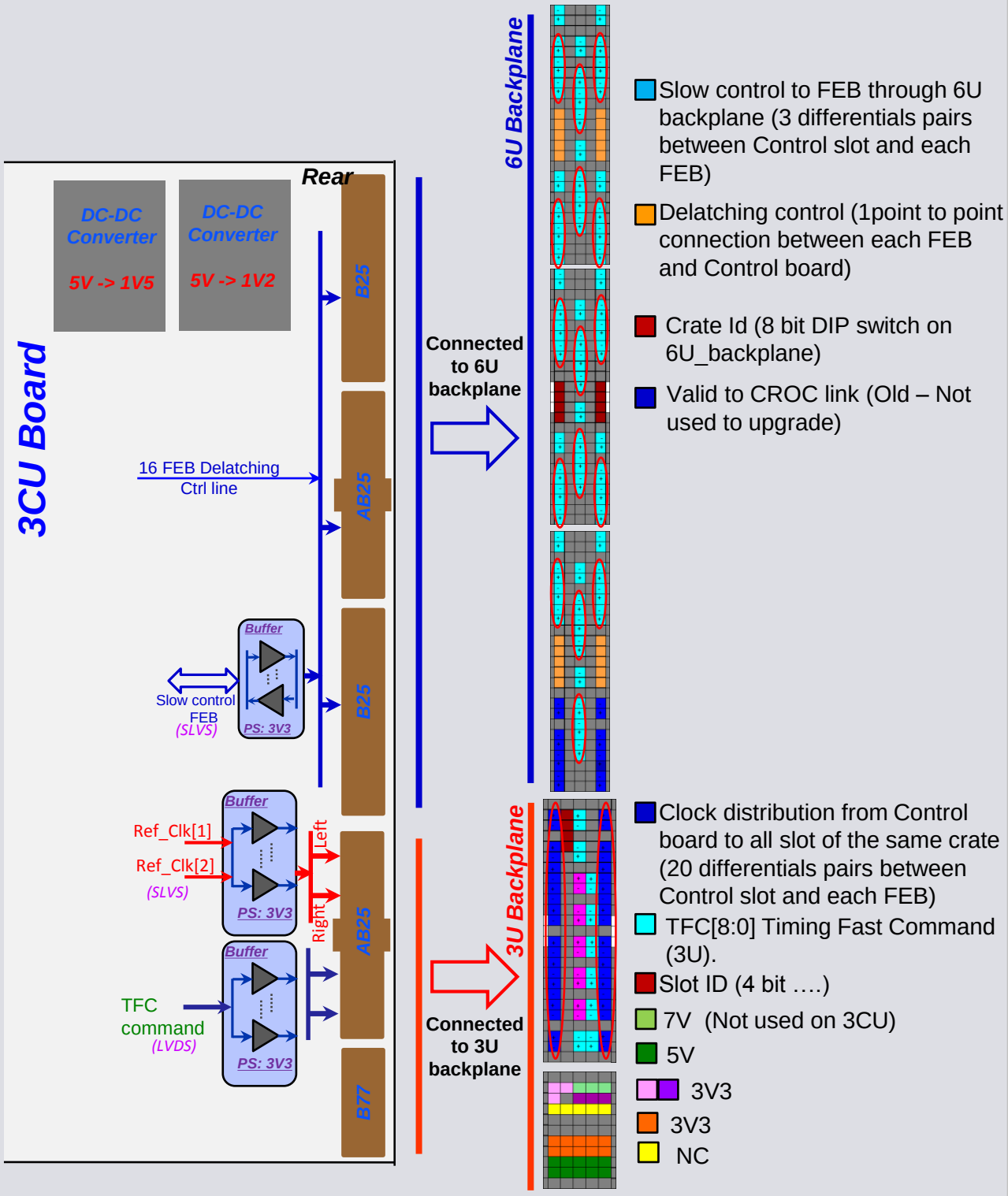


- 3CU power supplies needed
  - 5V
    - Input DC-DC converter for 1V5 and 1V2
  - 3V3
    - Discret components,
  - 2V5
    - VTRx, FPGA IOs, …
  - 1V5
    - GBTx, GBT_SCA, VTRX, …
  - 1V2
    - FPGA Core
- Crate power supplies available:
  - 7V, 5V, 3,3V, and 2,5V
  - 7V must be decrease at 6V
- Modification to the compatibility with the LEDTSB design
  - Move the 2.5V to 3.3V and use diodes to generate the 2.5V.

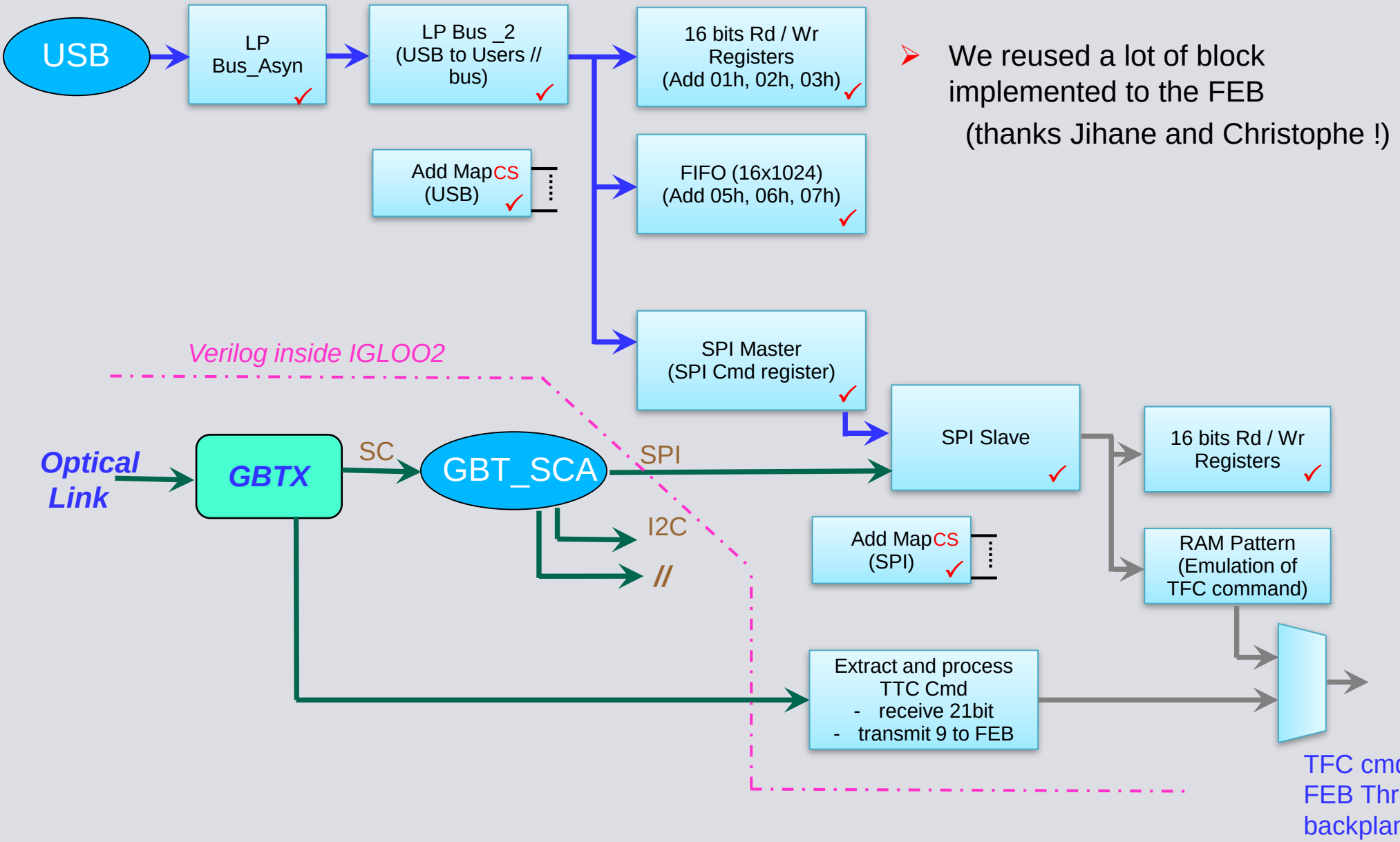


3CU Board : rear connection with 3U and 6U Backplane

- 6U Backplane connections
  - Transmit SC to all the FEBs
  - Crate Id
  - Delatching control line
- 3U Backplane connections
  - Power supply distribution
  - Clock distribution
  - TFC command distribution



Firmware architecture (IGLOO 2)

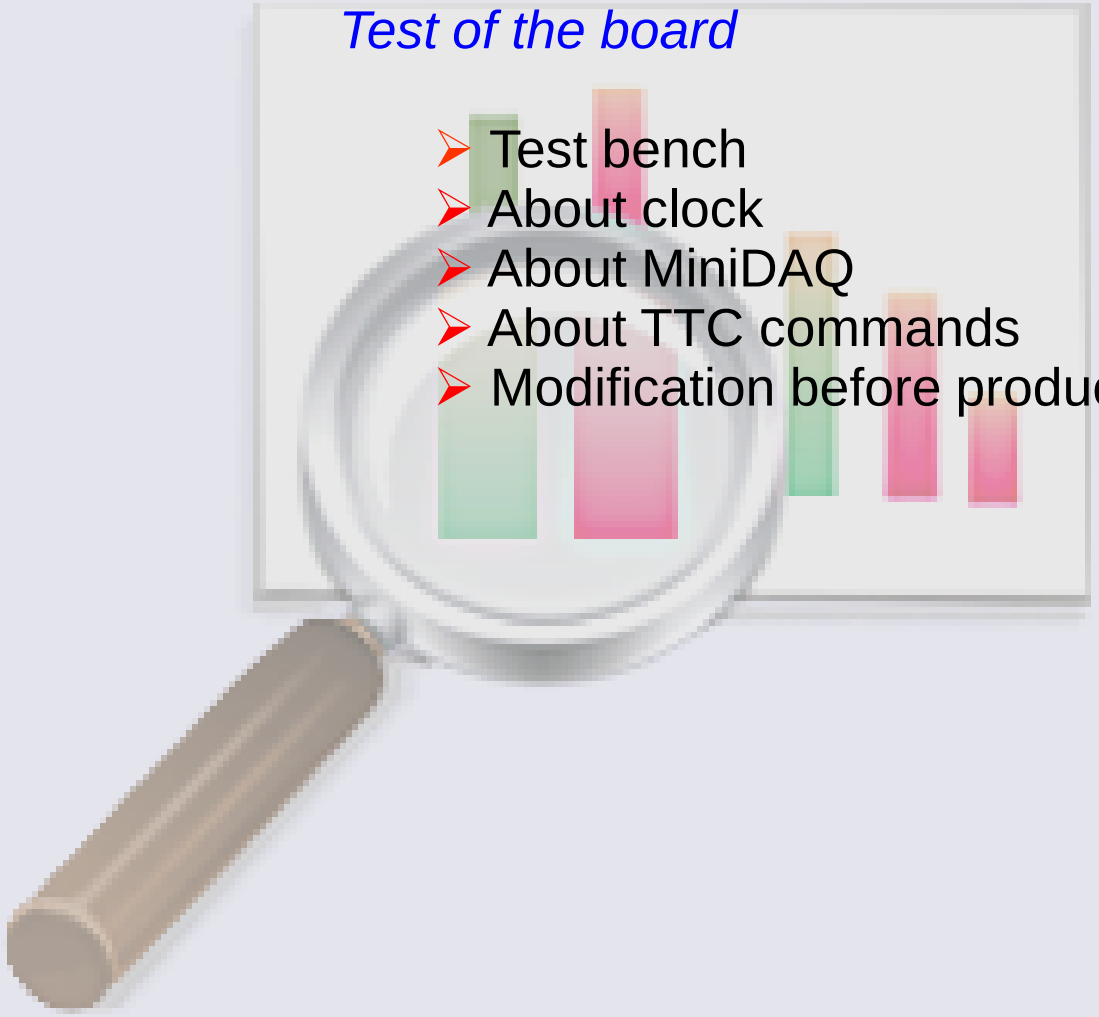


- We reused a lot of block implemented to the FEB
  (thanks Jihane and Christophe !)

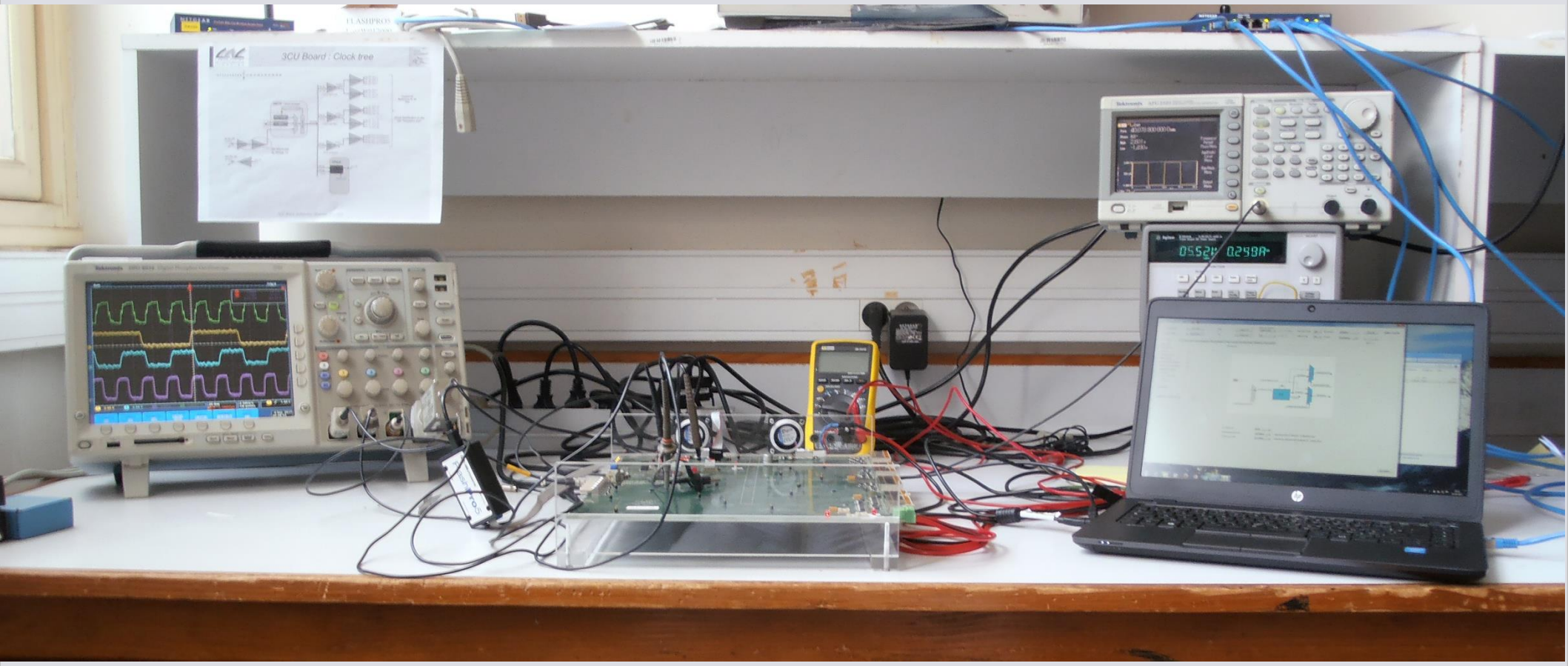
PRR 3CU board

Test of the board

- Test bench
- About clock
- About MiniDAQ
- About TTC commands
- Modification before production



3CU Test Bench



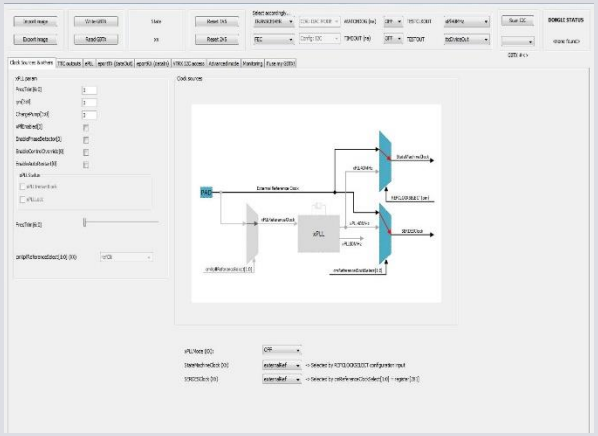
- Two 3CU board prototype available
  - Optical link from MiniDAQ
  - External clock generator
  - USB interface
  - Power supply, oscilloscope , …

Test status about clock and MiniDAQ

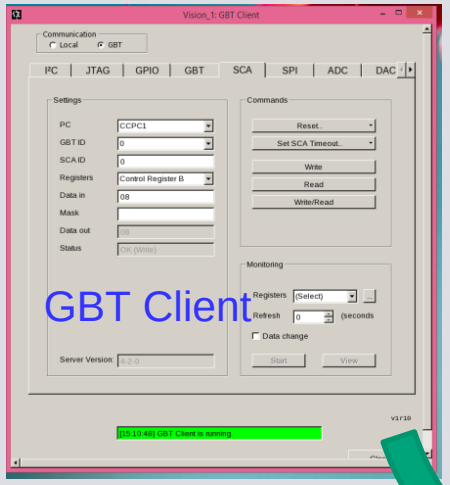
- About clock
  - ✓ The 3CU board works in master Clock

    Without optical links and With GBTx configuration by dongle (I2C) from CERN
  - ✓ The 3CU board works with the Clock locked on the optical fiber

    With optical links (from MiniDAQ) and with GBTx configuration by dongle (I2C) from CERN
  - To do The test of the Clock distribution through backplane to FEB is to do.

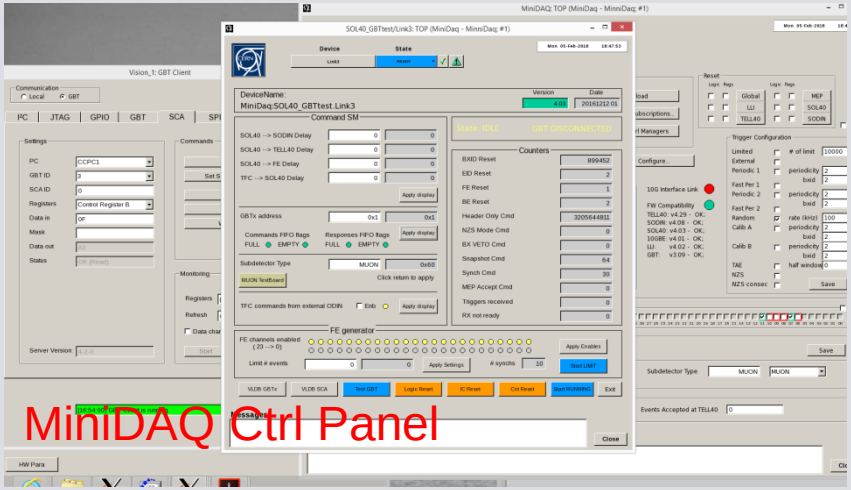


- About MiniDAQ (Optical link between MiniDAQ and 3CU board only)
  - ✓ The MiniDaq (GBT Client) read the fourth Ctrl register inside the GBT_SCA.



By optical link

Test status about TTC command



By optical link

- About MiniDAQ and TTC command
  - The “Start_Run” command generate a Synch. Pulse in the frame
  - Extract a Synch pulse from the frame (inside IGLOO2 FPGA)
  - Transmit to FEB through backplane

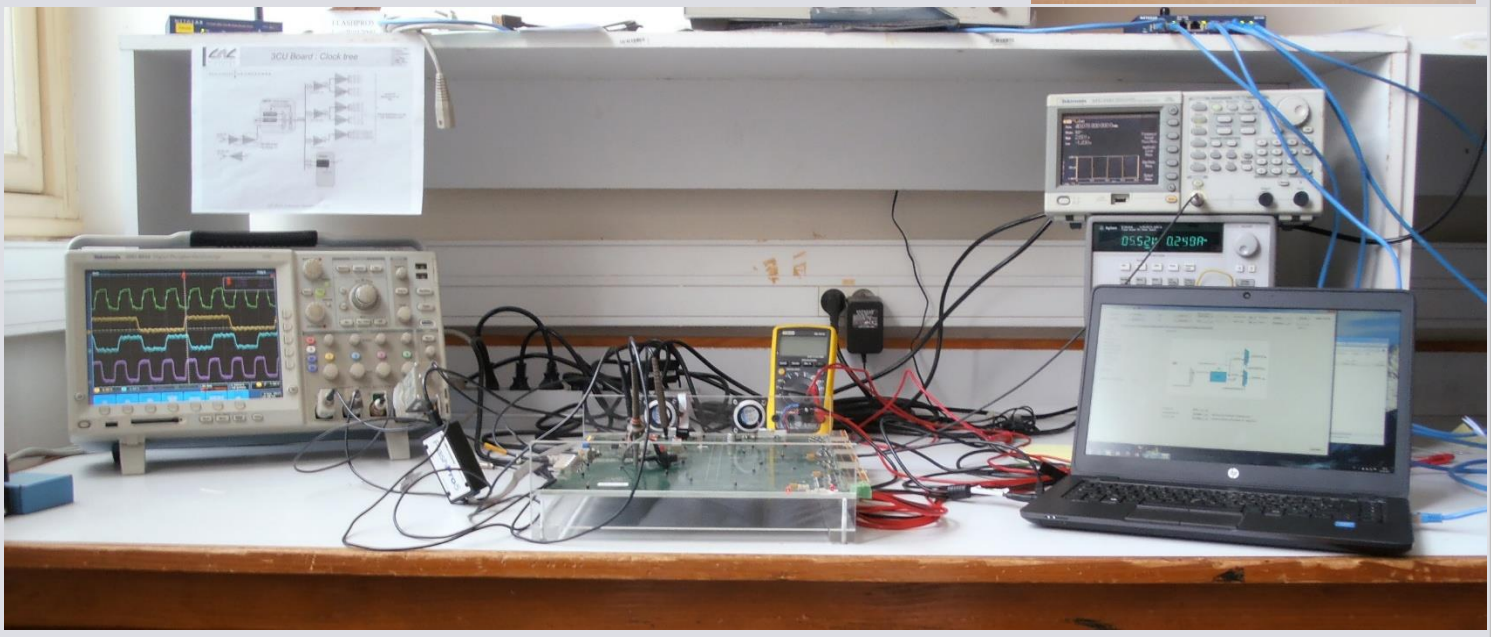
In progress

Modifications and test before production

- 30 boards will be produced (including spares)
- Wire modification
  - Grounding of DC-DC converter (schematic mistake !)
  - Add decoupling capacitor on several discret footprints
  - Remove switch to command the GBTx configuration, the configuration will be from the FPGA (Triple Voting Rregister).
  - Change the power supply : to move the 2.5V to 3.3V and use diodes to generate the 2.5 V. 2 Amps diode available
- Standalone tests
  - Extract the TTC command from a frame *In progress*
  - Transmit Rd/Wr from the GBTx (3CU) to GBT_SCA (3CU)
- 3CU board in the crate with FEB
  - Transmit the Clock through backplane to all FEBs inside the same crate (At the moment the clock is present on the rear connector of the 3CU board)
  - Transmit the TTC command through backplane to all FEBs inside the same crate
  - Transmit Rd/Wr from the GBTx (3CU) to GBT_SCA (FEB) through backplane

Conclusion

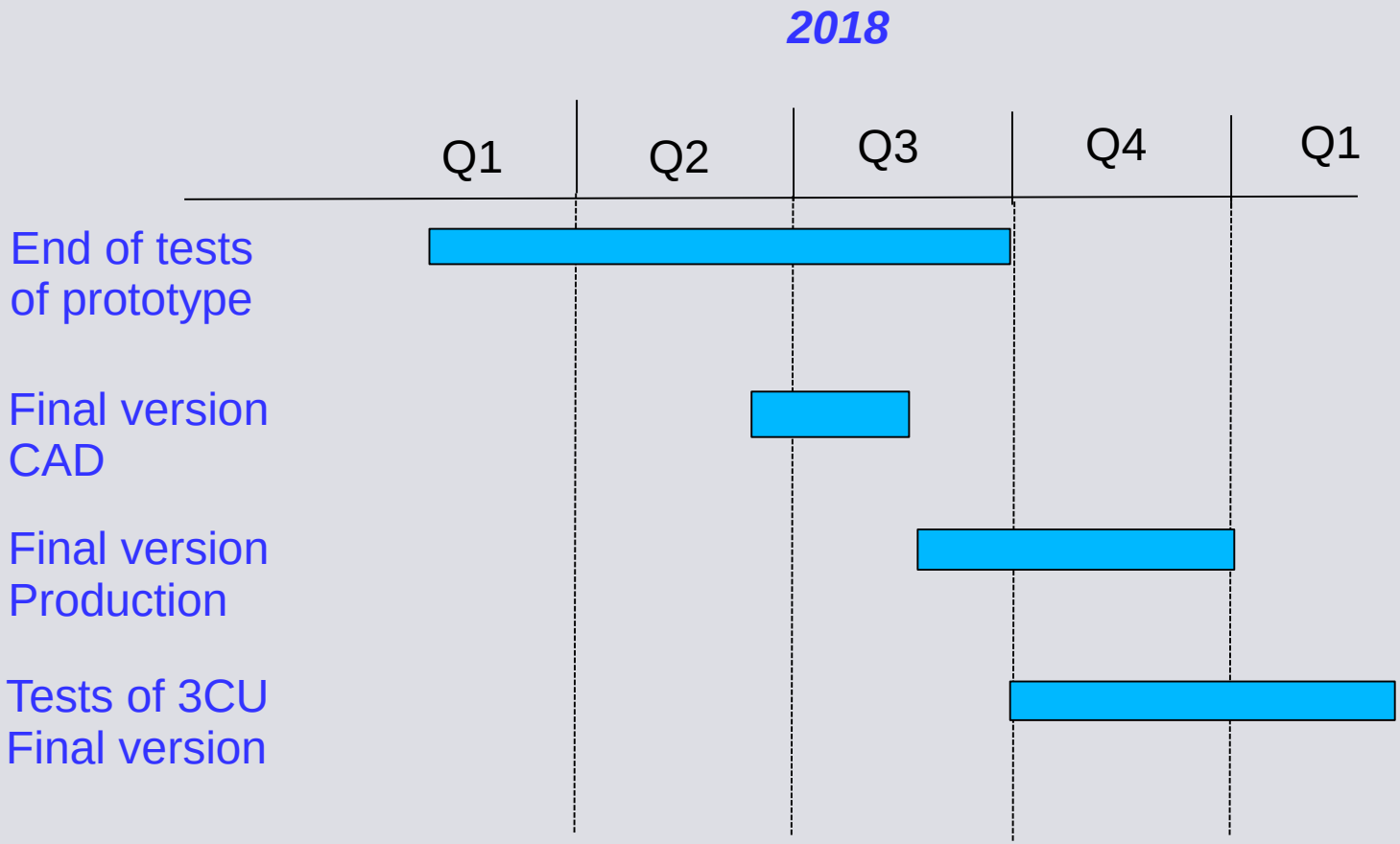
- Two 3CU prototype boards available and under test
- No major corrections for the final version
- There are still some tests to do before production (test with FEB inside the same crate)
- The 3CU documentation is available and up to date



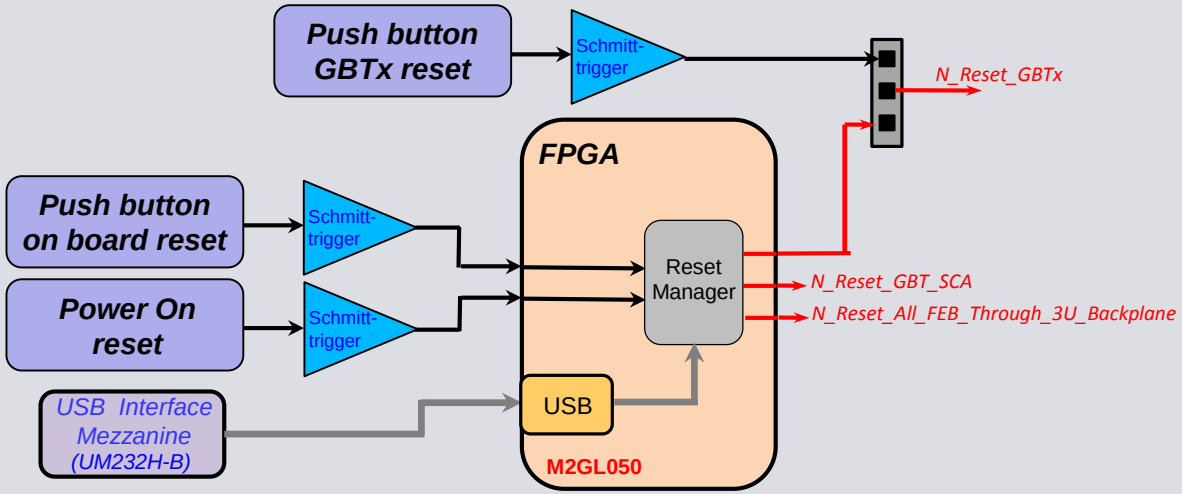
Thank you

SPARES

Production Schedule

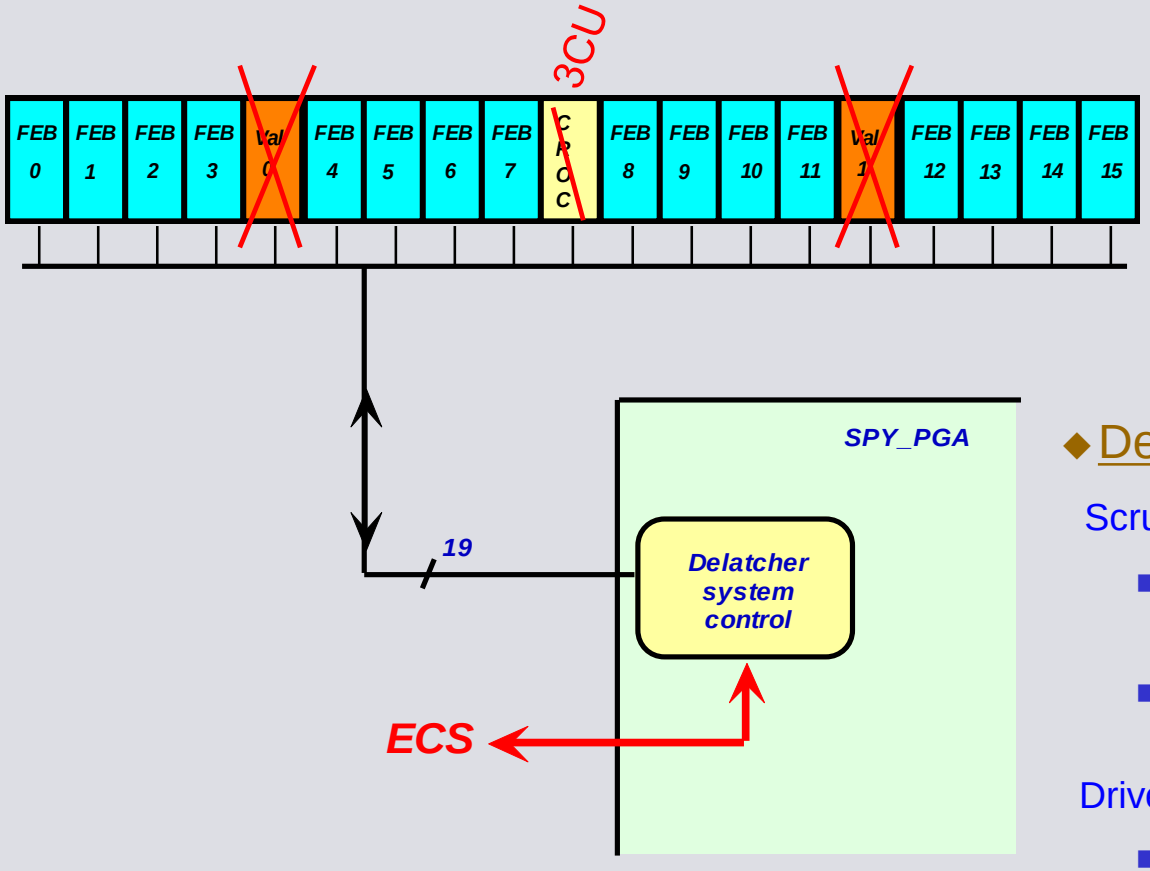


3CU Board : Reset tree



3CU Delatching

- Same as the CROC …



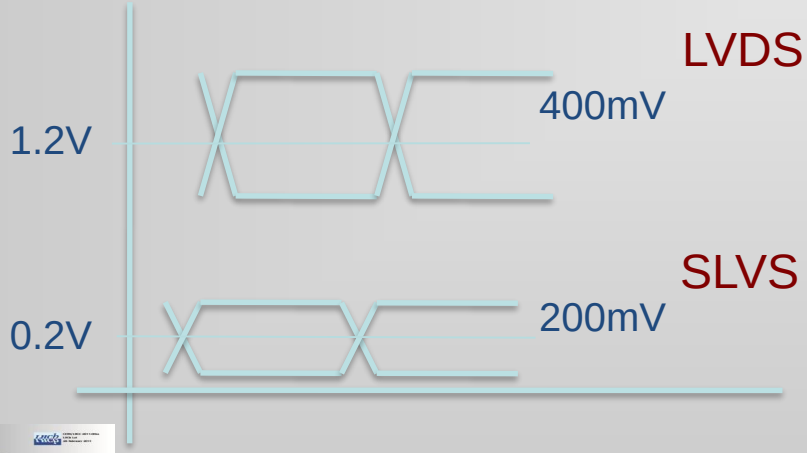
- Delatcher

  Scrutinize mode
  - Scrutinize the state (ON or OFF) off all board inside crate
  - Storage delatching of FEB or Validation board (FEBn = OFF).

  Drive mode
  - Switching ON or OFF of FEB or Validation (FEBn= ON or OFF).

SLVS standard

- SLVS (Scalable Low Voltage Standard)
  - JEDEC standard: JESD8-13
  - Differential voltage based signaling protocol.
    - Voltage levels compatible with deep submicron processes.
    - Typical link length runs of 30cm over PCB at 1Gbps.
    - Low Power, Low EMI
  - Application in data links for Flat Panel displays in mobile devices.
    - Mobile Pixel Link, MPL-2 (National semi.)



SLVS specifications brief
2 mA Differential max
Line impedance: 100 Ohm
Signal: +- 200 mV
Common mode ref voltage: 0.2V