CALO slow control electronics upgrade – Production Readiness Review report for the HV, LED Monitoring and Cs Calibration systems

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Production Readiness Review report for HV, LED Monitoring and Cs Calibration systems

Outline

- Introduction
- Radiation hardness consideration.
- Development and design validation with prototype testing
  - Control Mezzanines (adapterMez_010-HV, adapterMez_025-LED) – for replacement HV control, CS calibration control and LED monitoring system mezzanines
    - Firmware design,
    - Setup for making functional tests and validation FPGA firmware.
  - ECS interface mezzanines (scaHV_Mez02, scaLED_Mez02) - for replacement the SPECS mezzanine by new mezzanines based on GBT-SCA ASIC
    - Setup for making functional tests and validation GBT-SCA mezzanines
  - "E-Link Distributor Mezzanine"- [ELDM] card based on GBTx ASIC.
    - Board architecture and installation consideration
- Prototype production and mass production readiness
- Planning of the post production tests
- Conclusion
- References

Introduction

The upgrade project of the LHCb CALO slow control electronics is described in reference [1].
The EDR of the CALO slow control electronics took place on 21 February 2017.
There are two reasons of the motivation for the HV, Cs Calibration and LED Monitoring electronics upgrade :

- First is replace the electronic parts more sensitive to irradiation by new ones with same functionality, but equipped with new radiation tolerant components. Microsemi IGLOO2 FPGAs and CERN ASICs developed for GBT project will be used in upgraded electronics.
- Second reason is replace the currently used SPECS system (interface card between front-end and ECS system) by new one based on the CERN GBT architecture.

❑ **Important note: Upgrade of the base electronics parts is not foreseen!**
❑ **Functionality of the new mezzanines should be absolutely the same as for current ones**

The CALO HV, LED monitoring and Cs calibration systems include about 140 Control and SPECS mezzanines. New E-Link distributor card should be designed too, because the SPECS system with a daisy chain architecture is changed to a star topology of the GBT system.

The CALO slow control electronics upgrade of the HV and Cs monitoring systems includes replacement of two mezzanines on each motherboard of the HV and Cs subsystems:

- Existing Control mezzanine (based on ACTEL ProAsicPlus series) is replaced by a new HV Control mezzanine named – “adapterMez_010-HV” based on IGLOO2 FPGA
- SPECS mezzanine card will be replaced by a “scaHV_Mez02” interface card based on GBT-SCA ASIC

LHCb Calorimeters

Introduction *continued*

PCB design of the Control mezzanine for HV and Cs monitoring Systems is identical, the only difference is in firmware. Gbt-SCA Mezzanine card is the same for both systems too.

Production quantity [In total 108 mezzanine cards]:

- HV Control Mezzanine - “adapterMez_01-HV” – 54 (46 + 8 spares)
- Interface GbtSCA Mezzanine – “scaHV_Mez02” - 54 (46 + 8 spares)

The calorimeter LED monitoring system upgrade includes replacement of the two mezzanines on each LEDTSB motherboard installed into the frontend crates:

- Control Mezzanine named - “adapterMez_025-LED”
- Interface to ECS Mezzanine named - “scaLED_Mez02”

Communication of the DCS computer to several slow control electronic boards is performed through the optical links with subsequent conversion to electrical links, as defined in the GBT project. This architecture is required the distribution of the transmitted data from one optical line to several copper e-Links.
The E-Link Distributor Mezzanine – [ELDM] card has been designed to meet this requirement .
The ELDM card is based on the GBTx ASIC. Most of the distributor cards will be mounted standalone nearby the HV-LED & INTEGrator motherboards, few of them will be inserted into the FE crates. The design of the ELDM card is very similar to the VLDB board developed at CERN.

Production quantity [in total 36 mezzanines]:

- LEDTSB Control Mezzanine “adapterMez_025-LED” – 12 (10 + 2 spares) boards
- LEDTSB interface to ECS Mezzanine “scaLED_Mez02”– 12 (10 + 2 spares) boards
- e-Link distributor ELDM card “eLink_Mez” – 12 (10 +2 spare) pcs

Summary: five types of mezzanines have to be designed; in total of 144 cards will be produced installed and commissioned

Radiation hardness consideration.

Radiation environment for CALO on-detector electronics:

In many LHCb presentations [2] the maximal expected TID dose at the electronics location for the post-upgrade period (50 fb-1) is about 5 krad. This result is in a good agreement with analysis of the LHCb Radiation and background group (see Matthias thesis [3]).

We payed attention to a radiation-tolerant design of the calorimeter slow control electronics by using the radiation-hardening techniques:

1. The radiation-tolerant components were chosen:

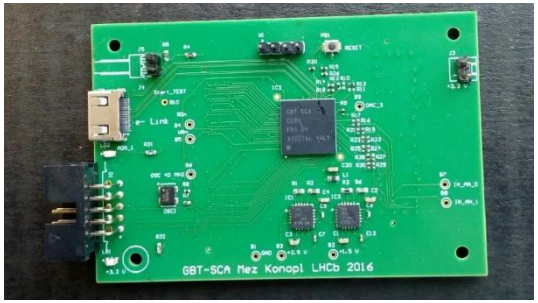
1. MicroSemi IGLOO2 FPGAs
2. CERN voltage regulator LHC4913
   ["Radiation performance of the L4913 voltage regulator", IEEE Xplore Conference: Radiation Effects Data Workshop, 2002 IEEE]
3. Texas Instruments Linear Regulator TPS74201 tested by ATLAS up to 80 krad (1.5*10^12 protons/cm^2, E=230 MeV)

2. The TMR (Triple Modular Redundancy) technics will be used for improving tolerance of the IGLOO2 FPGA logic to radiation environment.

Conclusion: Radiation hardness of the selected components is few times higher than the expected TID dose at the electronics location.

HV slow control electronics design and production readiness

Upgrade has been done for two types of the mezzanine. Prototypes were designed, produced and tested with CALO HV system.



Control Logic replaced by "HV Control Mezzanine"

SPECS replaced by "HV GBT-SCA Mezzanine"

Reminder: HV_LED_DAC board Specification.

Readout of the control voltages is performed by two ADCs. The DCU-ADC (on SPECS mezzanine board) digitizes the HV control signals, and VFC-ADC (on the mother board) reads out the LED intensity control signals.

Outputs

- 200 control signals for the CW bases [HV DC-DC converter] in range from 0 to 5 V with 12 bit precision.
- 8 connectors for distribution 16 LED intensity signals in range from 0 V to +5 V with 12 bit precision and powering LED-PIN boards.
- 8 outputs of the stabilized LV and +100 V power supplies for feeding the 8 groups of the CW bases.

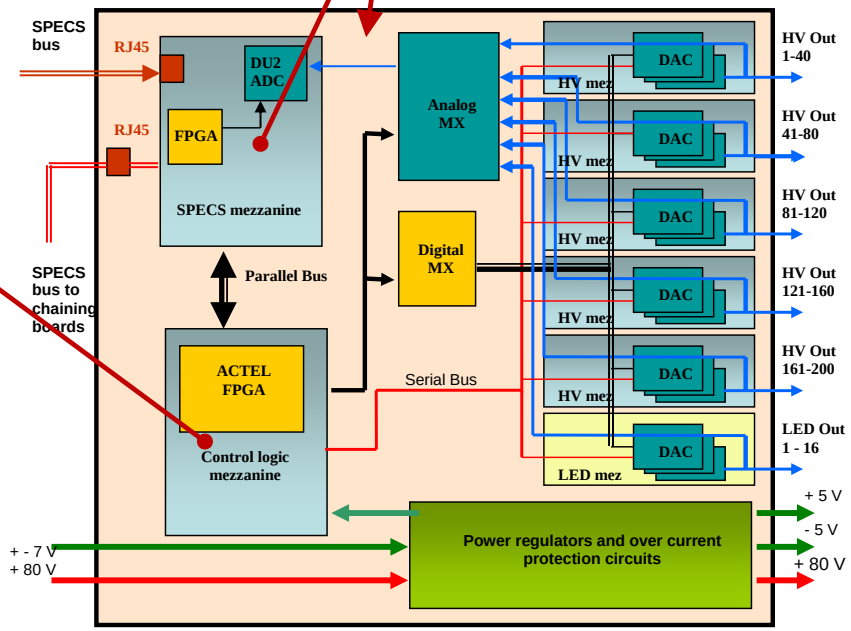
Voltages for CW base power:

1) +5.8 V, -5.8 V protected by fuses;
2) +100 V protected by relays.

Voltages for LED-PIN board:

1) +15 V for LED driver;
2) -30 V, +5.8 V, -5.8 V for PIN diode amplifier.

Main unit of the CALO HV & LED intensity control system is the HV_LED_DAC motherboard.

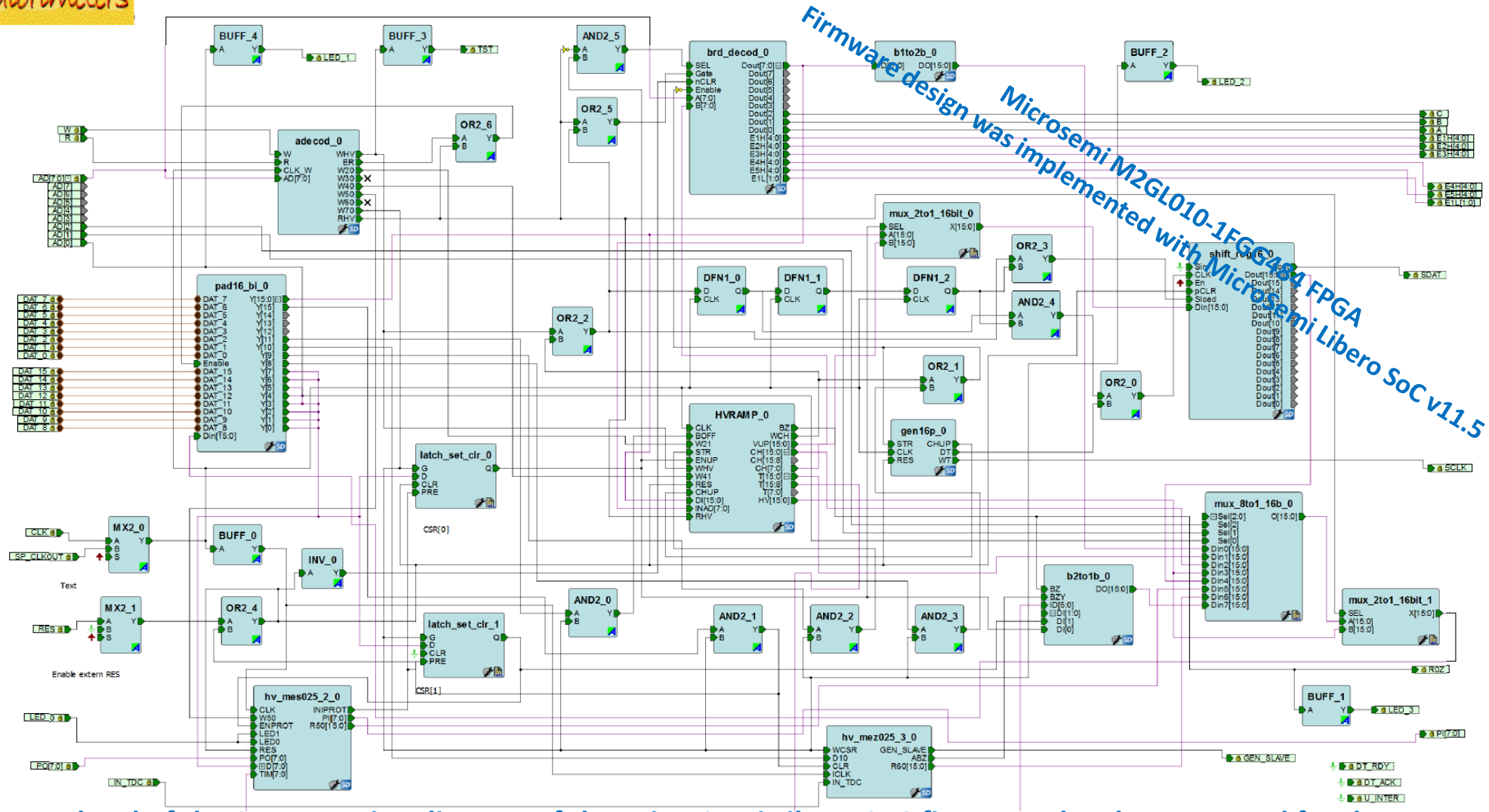


Block diagram of the HV & LED intensity control and power supply distribution board (HV_LED_DAC).

Status of HV Control Mezzanine design and test

- HV Control Mezzanine named – “adapterMez_010-HV” card is used for two applications: HV-LED control system and Cs calibration system
- This mezzanine is equipped with two active radiation tolerant components
  - Microsemi M2GL010 – 1FGG484 FPGA
  - CERN voltage regulator LHC4913
- PCB has been designed, two prototype boards produced, assembled and passed electrical tests
- Firmware for the HV-LED control application has been re-designed, simulated and uploaded into FPGA
- Extensive tests of the new HV Control Mezzanines were performed on the existing test-bench equipped with SPECS interfacing apparatus. The prototype cards have been passed all functional tests developed for mass production checking of the HV-LED motherboards in the past
- Testing of the Control mezzanine with the Cs calibration application is done too. The mezzanine passed all electrical tests with a 8 channels integrator - INTEG board. The FPGA firmware has been re-designed , simulated and uploaded. The prototype card was tested with SPECS system and passed all tests .

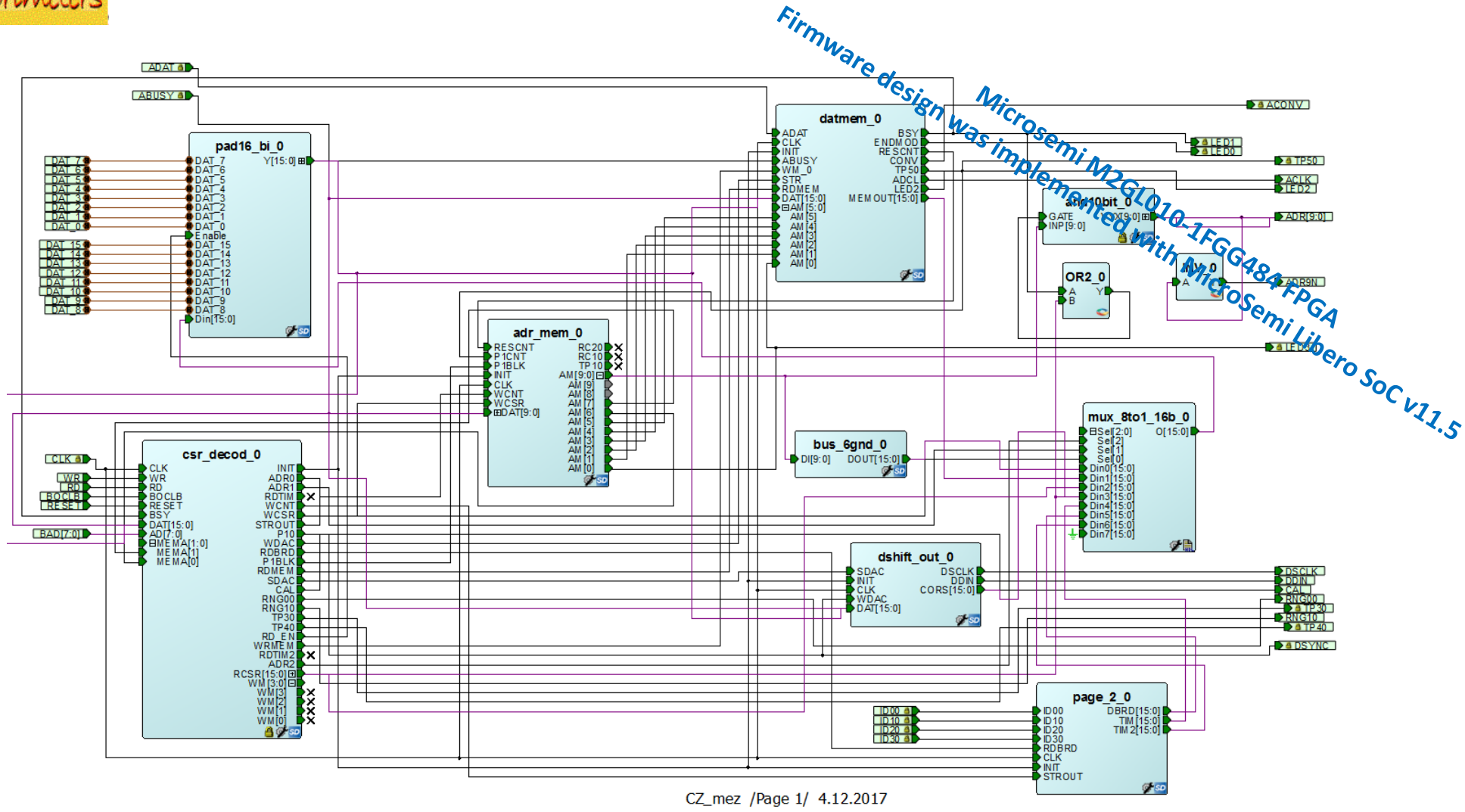
Illustration: Firmware of the "HV Control Mezzanine" FPGA



Top level of the Smart Design diagram of the MicroSemi Libero SoC firmware development tool for the HV-LED intensity control FPGA project.

At the moment The TMR (Triple Modular Redundancy) technics realized for a few registers. Optimization will be continued.

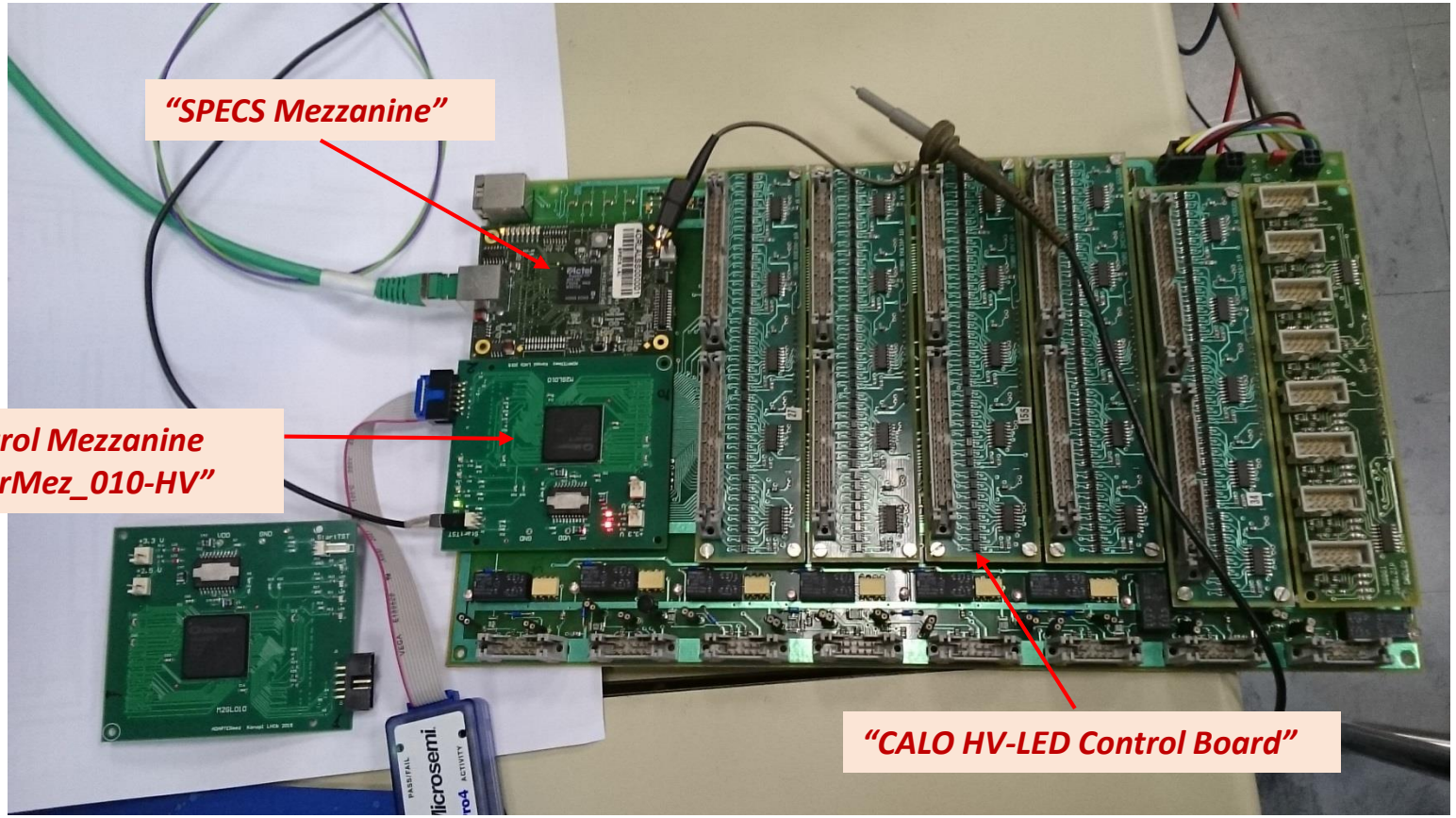
Illustration: Firmware of the Cs monitoring Control Mezzanine FPGA



Top level of the Smart Design diagram for the Cs monitoring control FPGA project.

Firmware optimization will be continued.

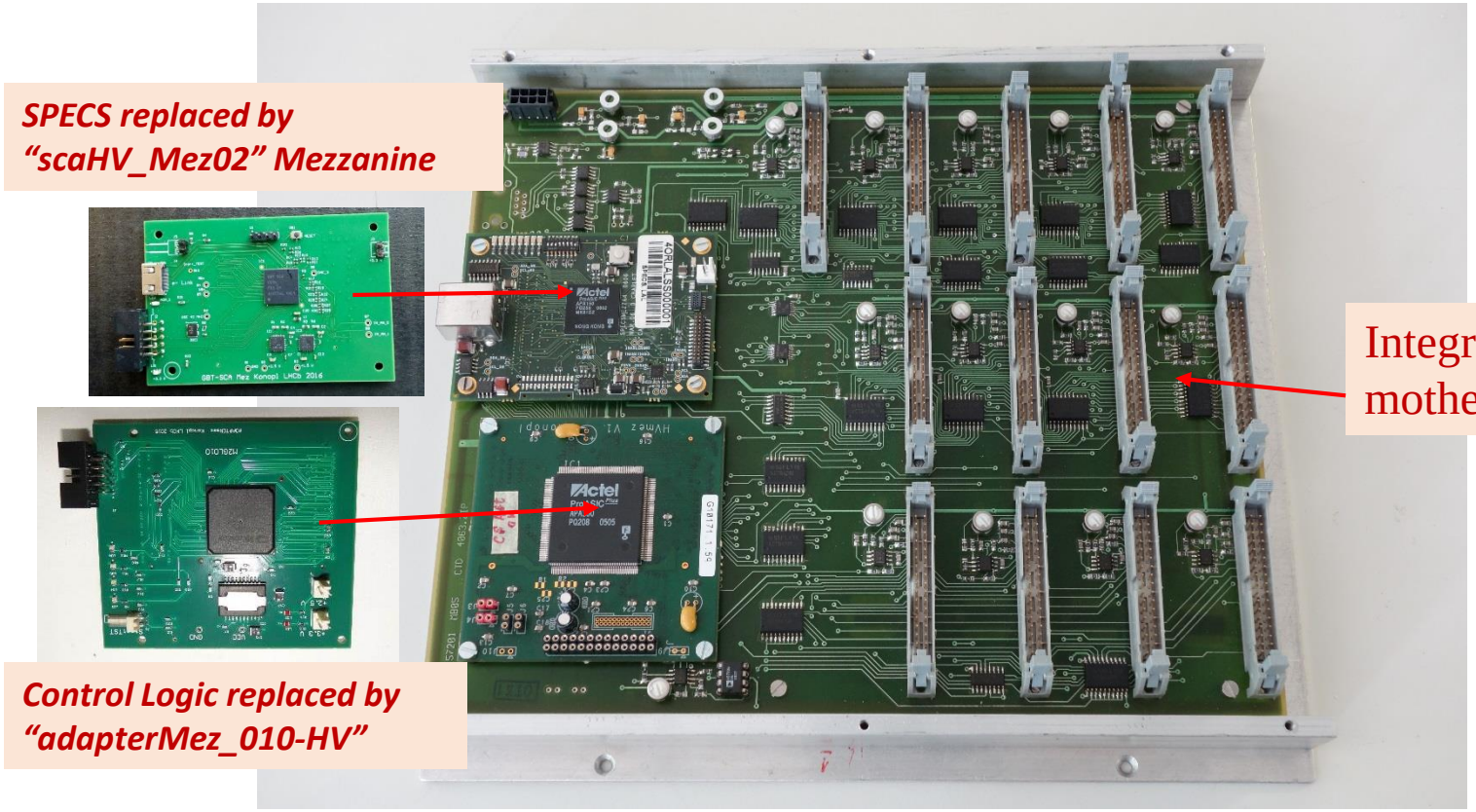
The HV Control Mezzanine was tested with "HV-LED Control" motherboard connected to the SPECS system



Setup for making full functional tests of the new mezzanine with a CALO HV-LED control motherboard

The prototype "adapterMez_010-HV" card was tested with the present CALO HV electronics interfaced to ECS by SPECS system.

The HV Control Mezzanine was tested with the integrator Readout motherboard of the Cs calibration system

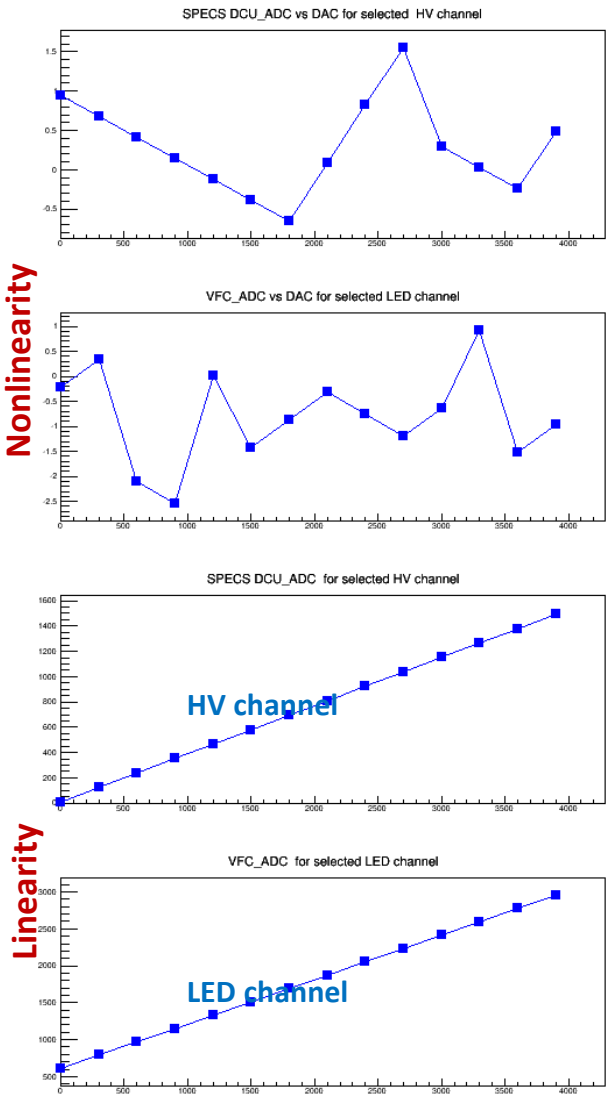


Setup for making full functional tests of the new mezzanine with the INTEG readout board

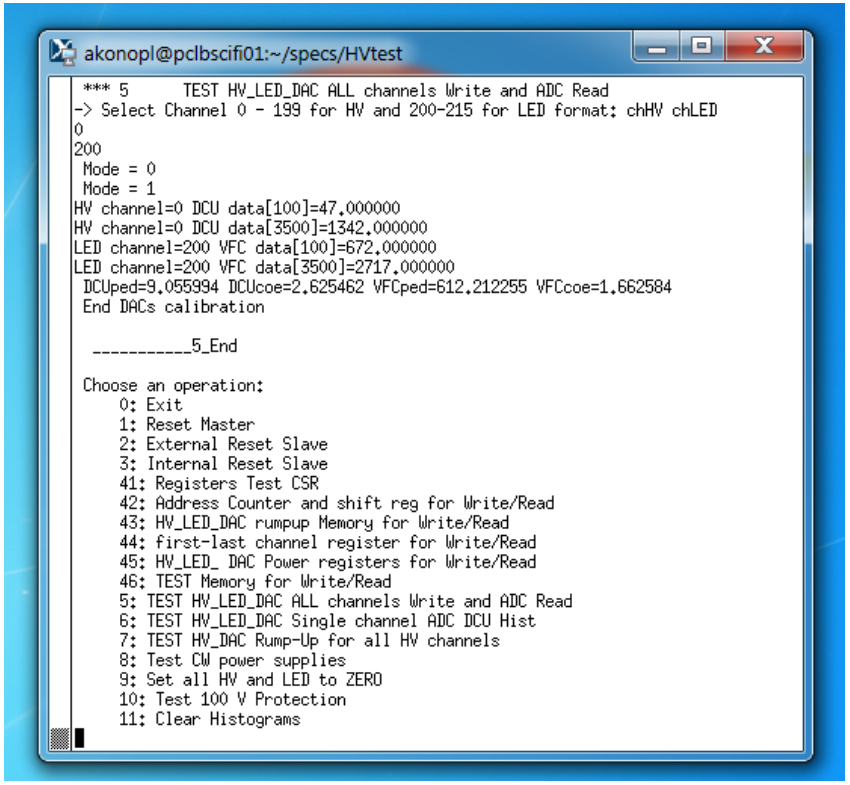
There are two steps of the tests:

- **Test and debugging Control logic FPGA with using SPECS interface card**
- **Complete test with two new mezzanines**

Illustration: Results of the HV Control Mezzanine tests with SPECS



Example of the output plots of the linearity test (ADC counts versus DAC converter value)



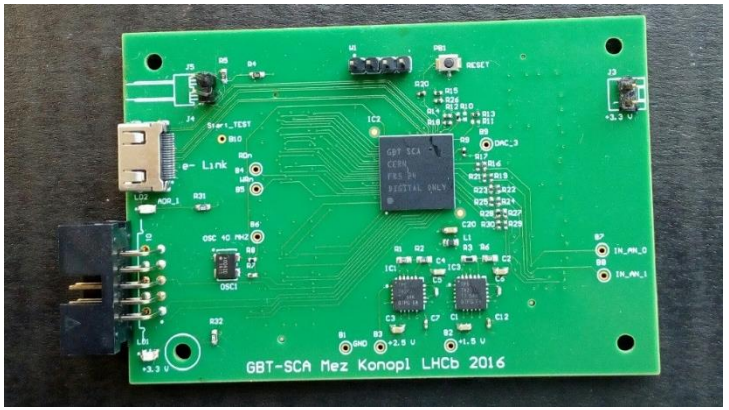
List of the validation tests used for debugging FPGA firmware.

- Powerful software has been developed for making the standalone functional tests with a CALO HV-LED control motherboard connected to PC by SPECS mezzanine.
- Finally one HV-LED_DAC motherboard equipped with a new “adapterMez_010-HV” mezzanine has been tested in the LHCb pit with working WinCCOA control system . All tests were passed.

Status of HV GBT-SCA Mezzanine design

New mezzanine card for using with the HV and Cs calibration systems based on CERN rad hard GBT_SCA ASIC was developed [Texas Instruments Linear Regulator TPS74201 is used as a rad tolerant power regulator]

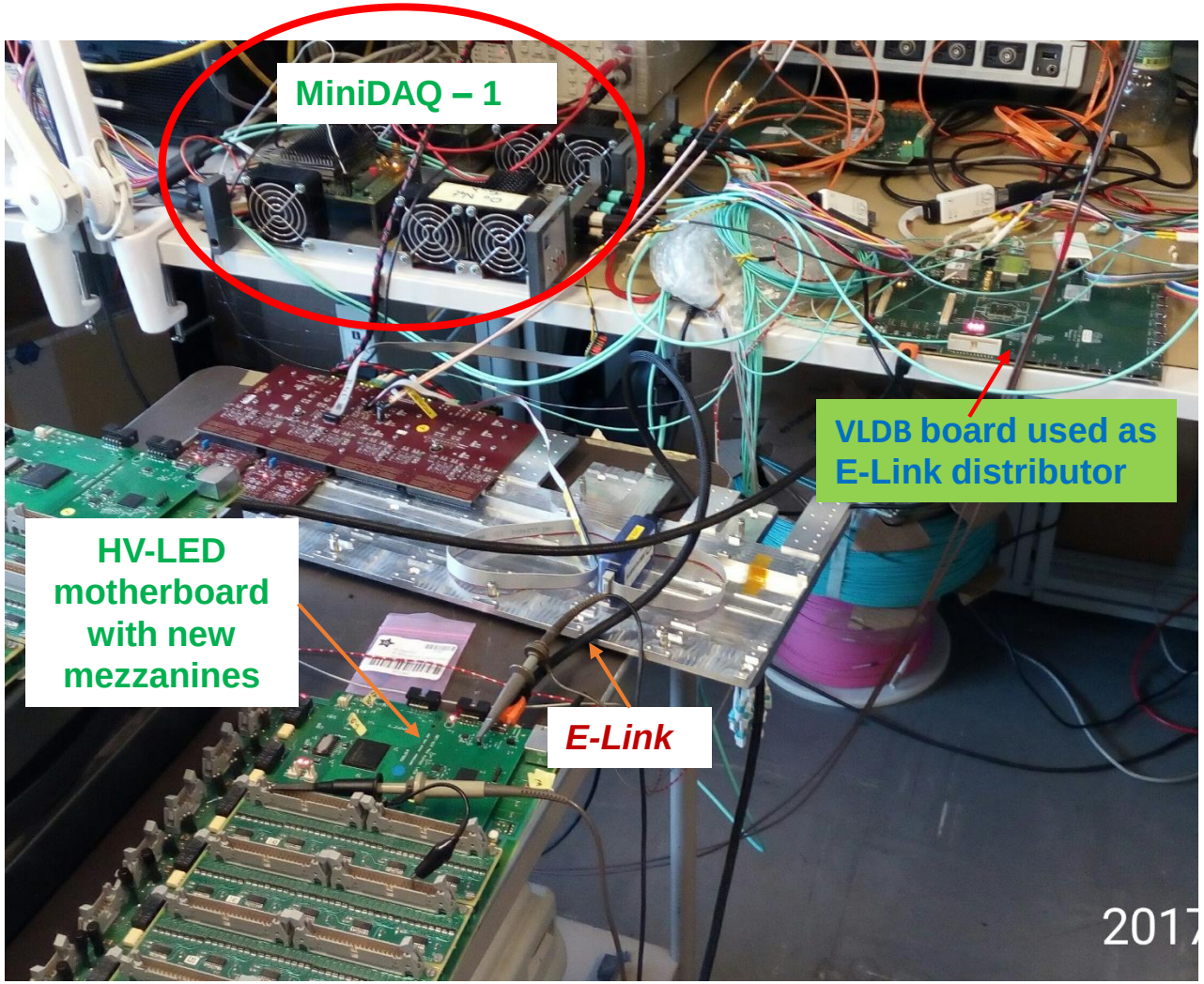
- PCB of the board has been designed and two prototype boards were produced and assembled
- Photo of the HV GBT-SCA Mezzanine named - ”scaHV_Mez02” card is shown below
- The functional tests of this mezzanine were done with using LHCb MiniDAQ-1 (thanks to Federico, Luis and Joao). CERN VLDB board is used as a E-Link distributor. (See next slide)
- LHCb MiniDAQ-1 setup dedicated for development and working with GBT system. It is equipped with all needed drivers, libraries and on top there is the WinCC OA control software



”scaHV_Mez02” photo

Unfortunately the MiniDAQ setup is rather expensive and complicated for doing simple validation tests at the time of mass production.
A standalone test bench based on XILINX KC705 board was created (thanks to Raul Martin Lesma).
Performance of this setup is sufficient for the most mass production tests.

ECS – MiniDAQ-1 system was used for the functional tests of the CALO HV system in condition very close to the real LHCb condition



LHCb MiniDAQ-1 test bench with our electronics

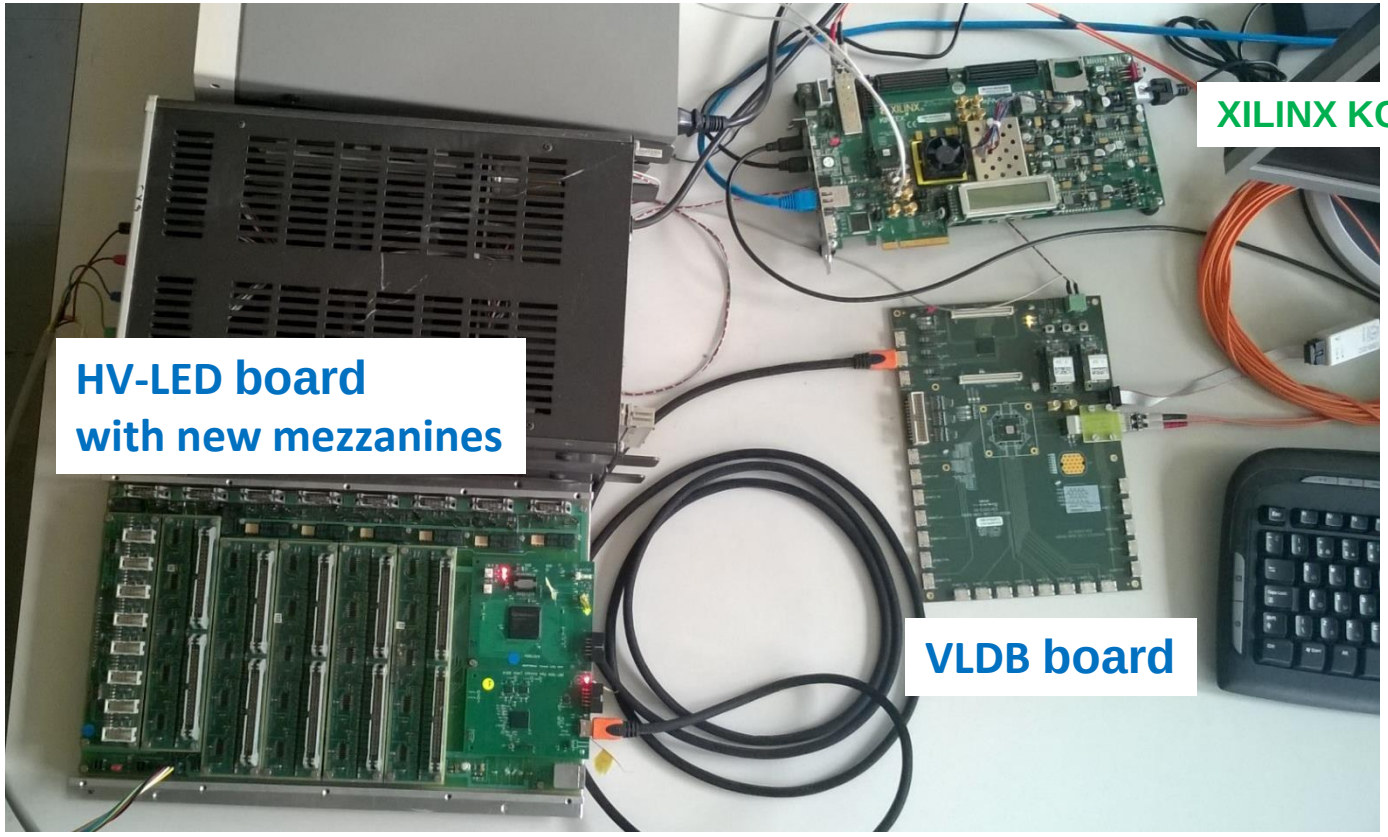
The MiniDAQ is a standalone system to test and debug Front End devices. The main control of the MiniDAQ is made via a SCADA system (WinCC OA) which provides the User Interface and archiving capabilities to control and monitor the MiniDAQ and the devices connected to it.

This setup is mainly dedicated for ECS software development by LHCb Online group. It is used as shared test bench for sub-detector users too.

Extensive tests were performed on this test bench with the calorimeter HV slow control electronics. Both control and interface cards were validated!

Test bench based on KC705 (Xilinx evaluation kit) was prepared for mass production tests

About 140 new mezzanines will be produced for LHCb calorimeter upgrade. For testing and validation these cards a flexible and inexpensive test-bench will be needed. Test bench based on Xilinx evaluation kit is prepared for mass production tests and shown below (same Xilinx kit is used by the CERN VLDB developers).

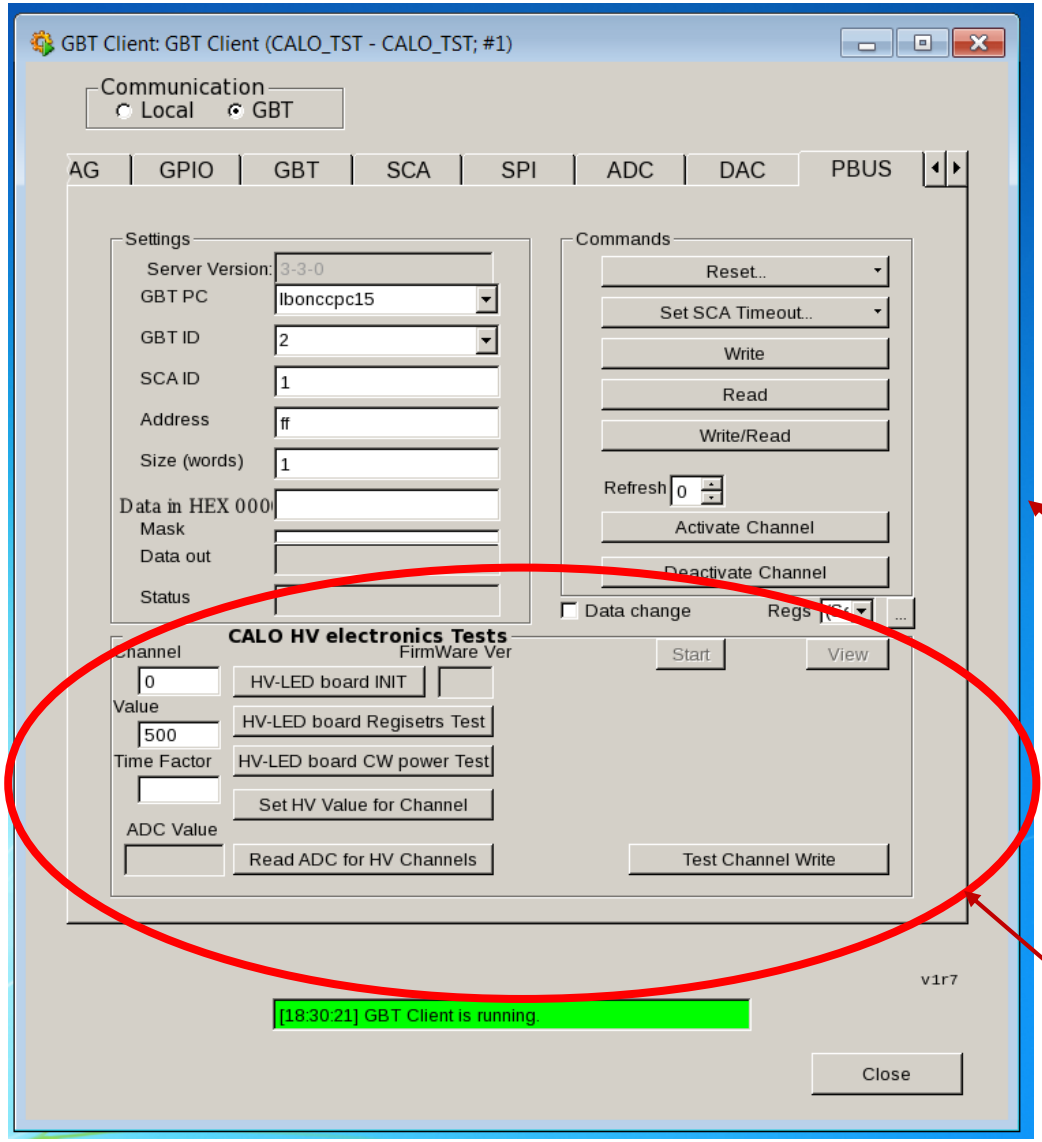


XILINX KC705, SOL40 firmware

At the moment this test bench is functional, but has very slow performance. Optimization the SOL40 firmware will be needed for speedup the PBUS operations.

Unfortunately we did not get the promised support from the CERN electronics group those designed and selling the VLDB board. We simply asked to borrow the working software that is used for the validation VLDB board before sale, but did not get it.

WinCC-OA software has been developed for the upgraded HV control electronics test



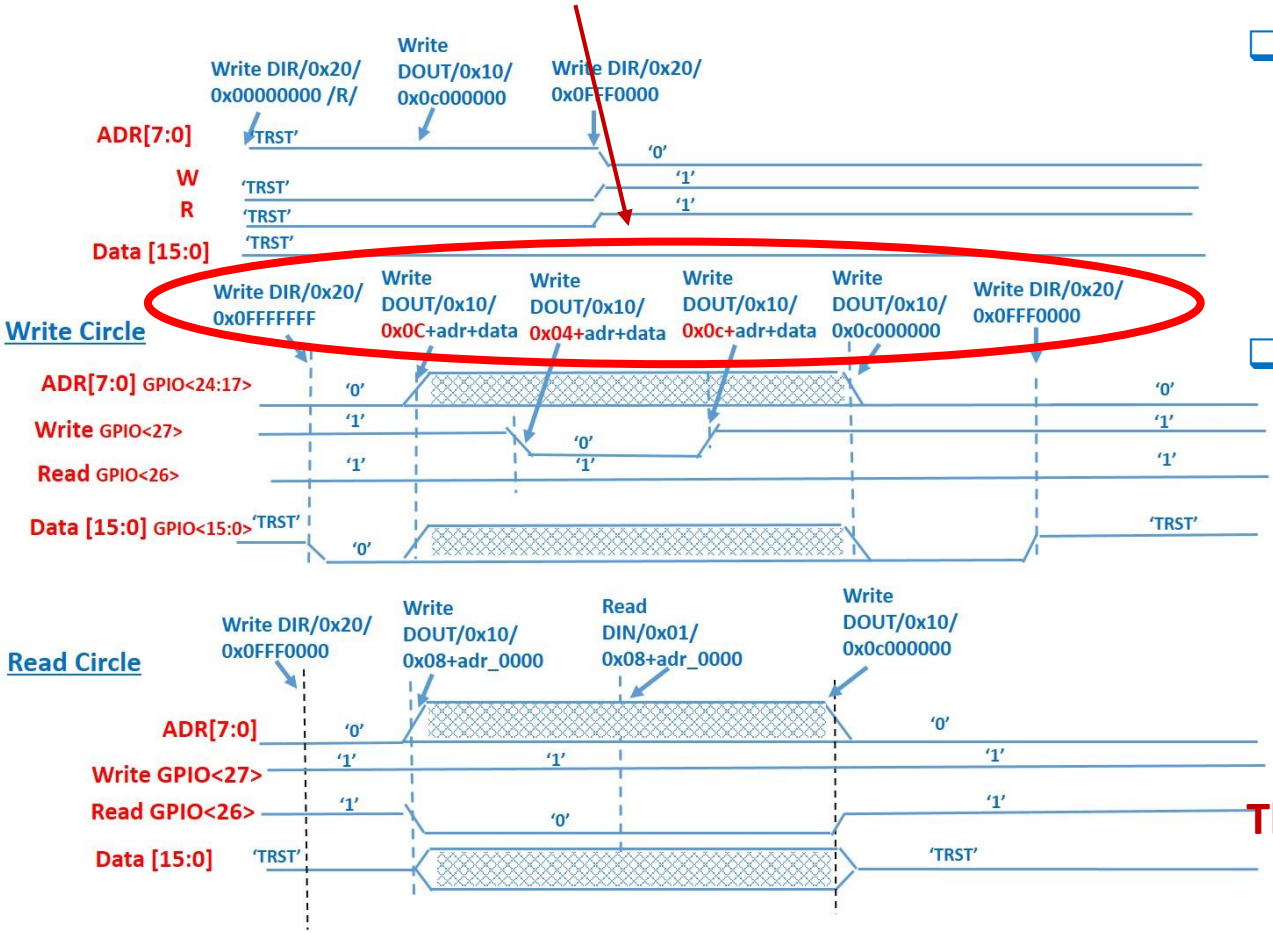
As well known, the LHCb ECS system is built on the WinCC OA software. It is important to validate our upgraded electronics with the actual software that will be used in the experiment after upgrade. LHCb MiniDAQ-1 test bench works under WinCC OA.

For testing the CALO slow control electronics a dedicated WinCC panel has been developed. It allows to perform many functional tests and estimate the timing performance.

Control Panel for the CALO HV electronics tests

Results of the PBUS timing optimization in the Gbt- Server library

Write PBUS operation needs six SCA GPIO commands



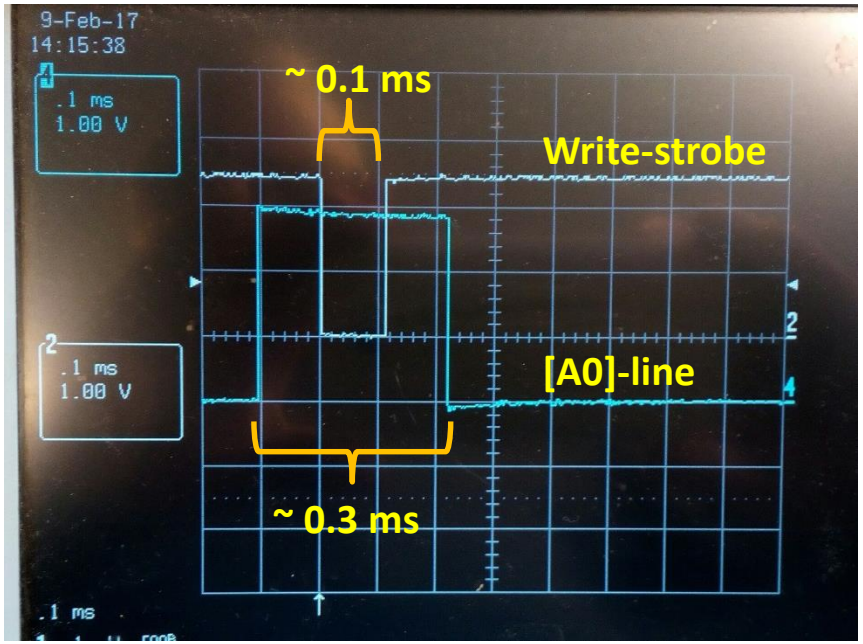
Timing diagrams of the write/read PBUS command generation by issuing the individual GBT-SCA GPIO operations

- One potential problem has been found with functionality of the GBT-SCA ASIC.
- Parallel bus [PBUS] port of the SPECS mezzanine is used as communication port in all HV, Calibration and Monitoring electronics. It was expected that in new design based on GBT-SCA chip the PBUS works too.
- Unfortunately the GBT-SCA ASIC has 32 – bits GPIO field with fully independent configuration, due to this reason for execution one PBUS operation from four to six the SCA GPIO commands are needed. First version of the Gbt Server library of the WinCCOA control software is not supported of the PBUS port operations.

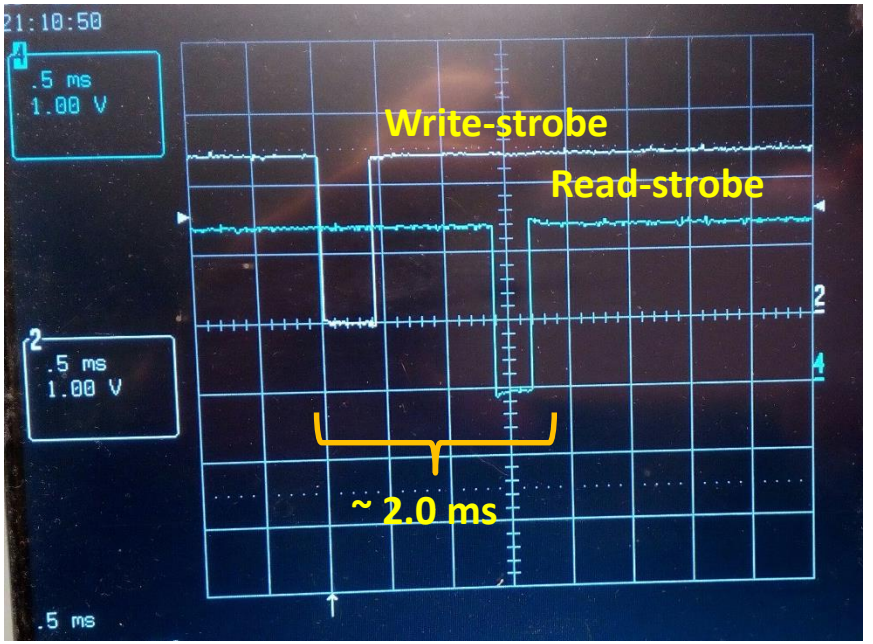
Thanks to the help of Clara, Luis and Joao the Parallel Bus operations were implemented on the level of the Gbt-Server library.

Test results are shown at the next slide.

Timing diagrams of the PBUS operations after optimization the Gbt-Server library



Oscillogram of PBUS write operation. Write-strobe and address line [A0] tracks.



Oscillogram of PBUS write/read operation. Write-strobe and Read-strobe tracks.

Log Viewer: *WCCOAui1:2017.02.16 09:19:35.774["Start Write for 200 channels"]*
WCCOAui1:2017.02.16 09:19:36.909["END HV memory write/read and Start Ramping Up!"]

From a Log View message one can see the time needed for configuration of the 200 channels of the HV memory and verification by a Read-back command is about 1.1 sec.

This timing performance is fully satisfy our requirements!

Summary of the production readiness of the new mezzanines for the HV control and Cs calibration systems

- ✓ The controlling and interfacing parts of the slow control electronics for the CALO HV control and Cs calibration systems have been upgraded. Specification of the new mezzanines met the initial design of the upgraded systems.
- ✓ Prototypes of the design have been tested with the final interfaces and the LHCb ECS software.
- ✓ All functionalities of the designed electronic cards were verified and tested.
- ✓ First working version of the firmware has been designed, simulated and tested too.
- ✓ HV board with new control mezzanines have been tested with present system at the LHCb HCAL detector.
- ✓ For the mass production tests a simplified test bench was organized.
- ✓ In time of the prototypes fabrication the design has been inspected and approved by manufacturer. We got the offers for the PCB production and components assembly.

Upgrade of the LED monitoring System

- Key module of this system is the LEDTSB motherboard
- LEDTSB board uses the infrastructure of the FEB crate where it's installed [power, clock, TTCrx commands …].
- Requirements for the control and interface mezzanines of the LEDTSB are higher than for similar mezzanines of the HV and calibration systems. In particular, LEDTSB uses Channel-B lines of the crate to make synchronisation with LHC timing. As a result, two new mezzanines have to be developed:

Control mezzanine

- The "adapterMez-LED" card is a Control Mezzanine of the LEDTSB. It has significantly more functional features compare with the HV Control mezzanine, therefore a more powerful IGLOO2 FPGA - Microsemi M2GL025 is used
- First version of the firmware was developed
- Two prototype boards have been produced and partially tested.

Interfacing to ECS mezzanine

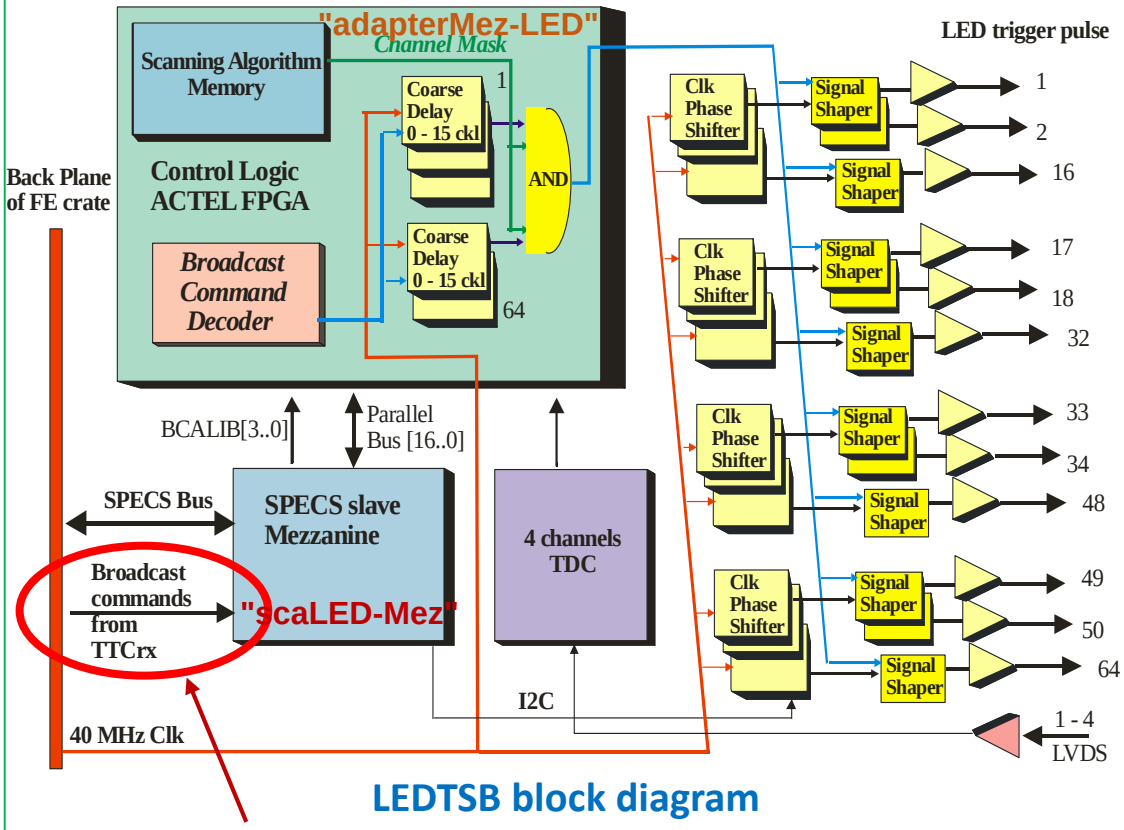
- The "scaLED-Mez" card is dedicated for intercommunication through e-link with ECS system. The functionality of the card is similar to the present SPECS slave mezzanine.
- Design of the "scaLED-Mez" is similar to the HV GBT-SCA mezzanine, but an additional IGLOO2 FPGA is used to implement the Channel B broadcast command decoding
- Two prototype boards have been produced and passed the electrical tests.

Reminder: LEDTSB motherboard Specification.

LEDTSB specification

- Number of channels – 64.
- 16 output connectors RJ45 type on a front panel,
- A level of the output signals is LVDS,
- Each channel has individual delay adjustment in a range of 0 – 300 ns with 1 ns step,
- A LED trigger signal width is 50 ns,
- LEDTSB boards have same size as FEBs board and are installed in the FE crate,
- Control Logic FPGA is placed on a mezzanine card for simplifying the chip exchange from non radhard to radiation hard ACTEL proASIC chip,
- Memory of the scanning algorithm FPGA with 64 patterns of the output trigger signals allows perform all needed sequences for LED flashing,
- SPECS slave mezzanine card (developed in LAL) is used for connection with ECS and TTCrx decoding,
- There are two operational mode:
- A) The main mode, when the LED trigger signals are generated from TTCrx command,
- B) The trigger signals are generated from a built in internal generator (Freq. ~ 1 kHz).
- Power consumption: +3.3 V -> 0.6 A; +5 V -> 0.1 A; -5 V -> 0.16 A.

LEDTSB is 64 channel pulse generator with an individual channel delay for flashing the monitoring LEDs in proper time. Monitoring-calibration signal is triggered by Broadcast TTCrx commands



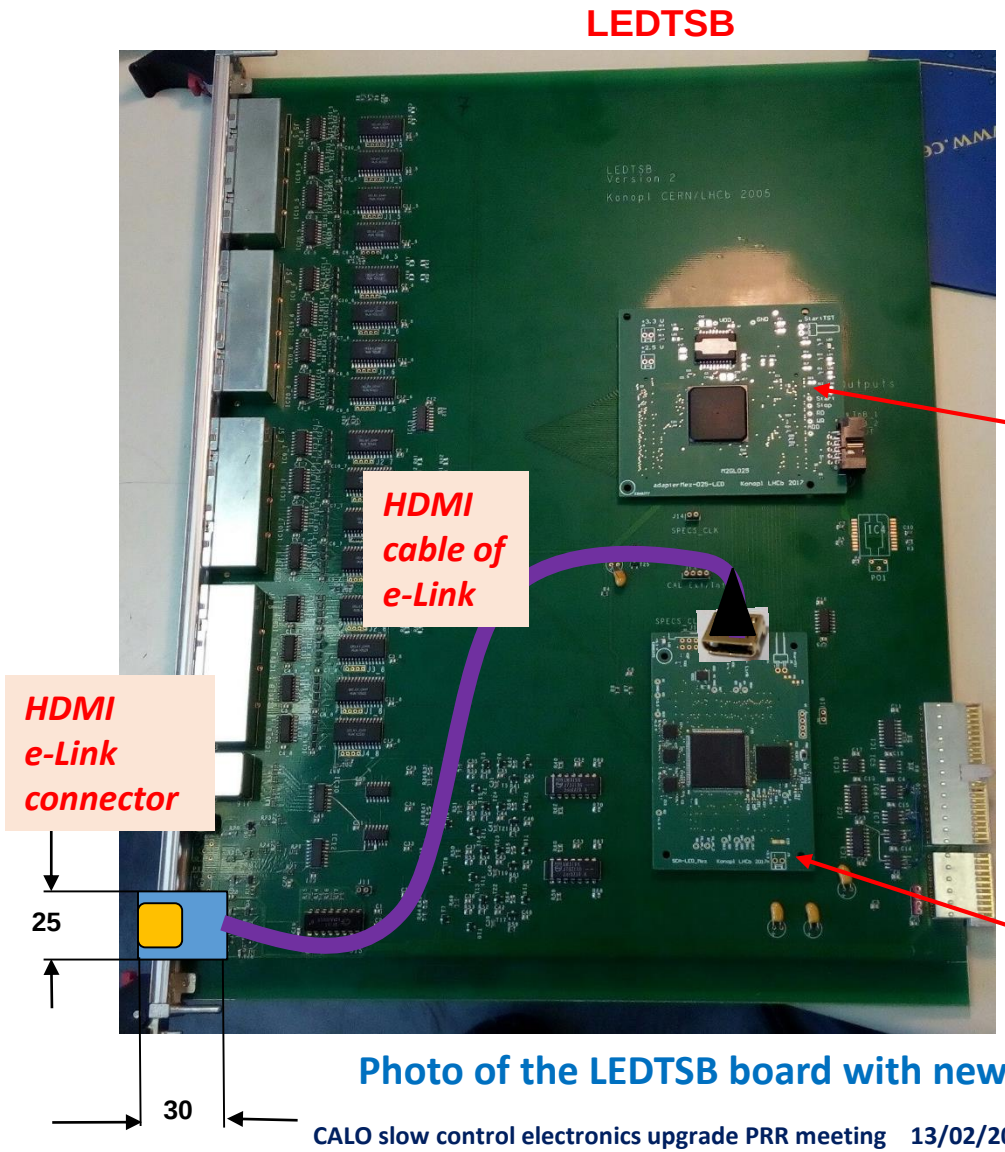
LEDTSB block diagram

Decoding of the Broadcast commands from TTCrx extends functionality of the LEDTSB GBT-SCA mezzanine card

LEDTSB adaptation for using with the new front-end crate

The backplane of the upgraded front-end electronics crate was modified. Due to this reason, the LEDTSB motherboard has to be modified too:

1. -5V power supply is needed for the LEDTSB internal calibration. This power is absent in the new FE crates, but could be arranged during the calibration by using an external power supply.



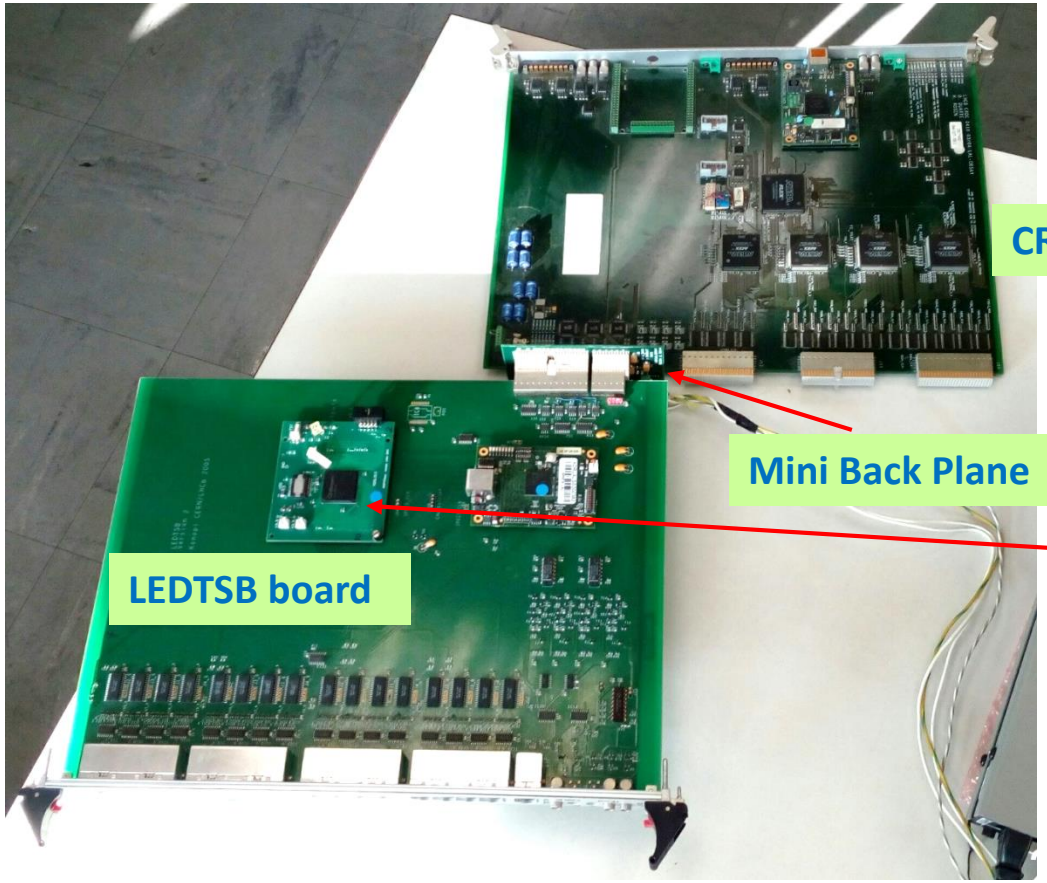
"adapterMez-LED" Control Logic card replaces existing "LEDTSB Control Mezzanine"

2. The SPECS bus is excluded from new FE back-plane. For connection the ELDM card with the "scaLED_Mez" card the HDMI connector and e-Link cable should be inserted into LEDTSB. This HDMI connector should be placed on the LEDTSB PCB near the front panel.

"scaLED-Mez" *Interface Card replaces the SPECS Mezzanine*

Photo of the LEDTSB board with new mezzanine cards and additional e-Link cable

Test bench for LEDTSB mezzanines testing and debugging



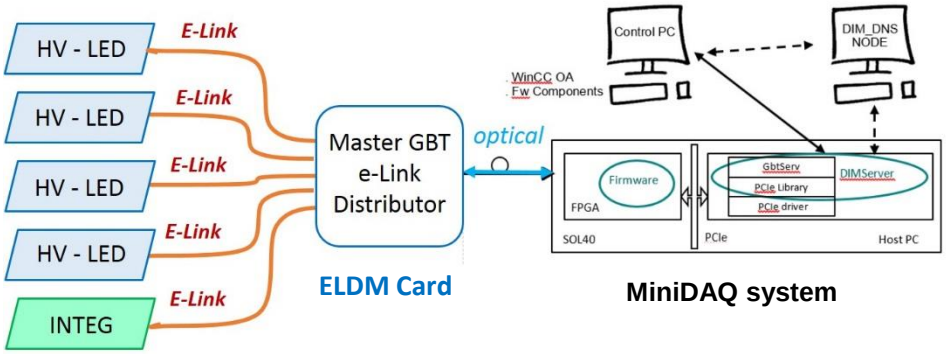
- For testing the upgraded LED monitoring electronics we are going to use the old test bench based on the LAL CROC-2 module and Mini Back-Plane card.
- "adapterMez-LED" mezzanine cards were tested with this test bench connected to SPECS system

Summary of the production readiness of the new mezzanines for the LED control and monitoring system

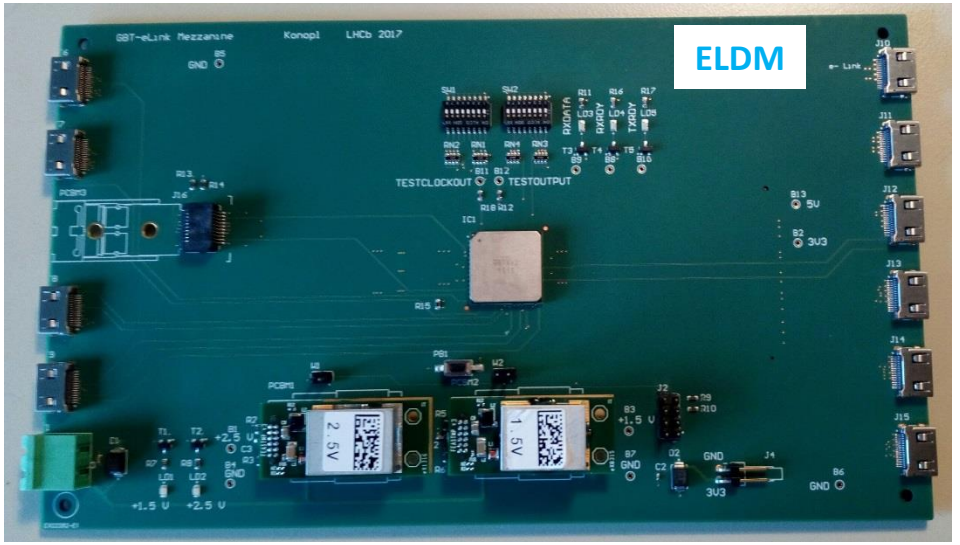
- ✓ Only the operating and interfacing parts of the slow control electronics for LED monitoring system have been upgraded. Specification of the new mezzanines met the initial design of the LED monitoring system.
- ✓ Prototype of the design have been tested with the existing SPECS interface.
- ✓ All functionalities of the designed electronic cards were verified and tested.
- ✓ First working version of the firmware has been designed, simulated and tested.
- ✓ In time of the prototypes fabrication the design has been inspected and approved by manufacturer. We got an offer from the “PCBtechnology” company for the PCB production and components assembly.

Status of the "E-Link Distributor Mezzanine" [ELDM] card design

The "E-Link Distributor Mezzanine" card was designed to ensure the communication of one DCS system to several control boards. These distributor cards will be mounted standalone nearby the HV-LED & INTEG motherboards, and few of them will be installed into the FE crates.



CALO slow Control System Architecture



The number of ELDM cards and number of E-Links per one card were chosen taking into account the required number of the e-Link ports and an allowed cable length - about 2 m.

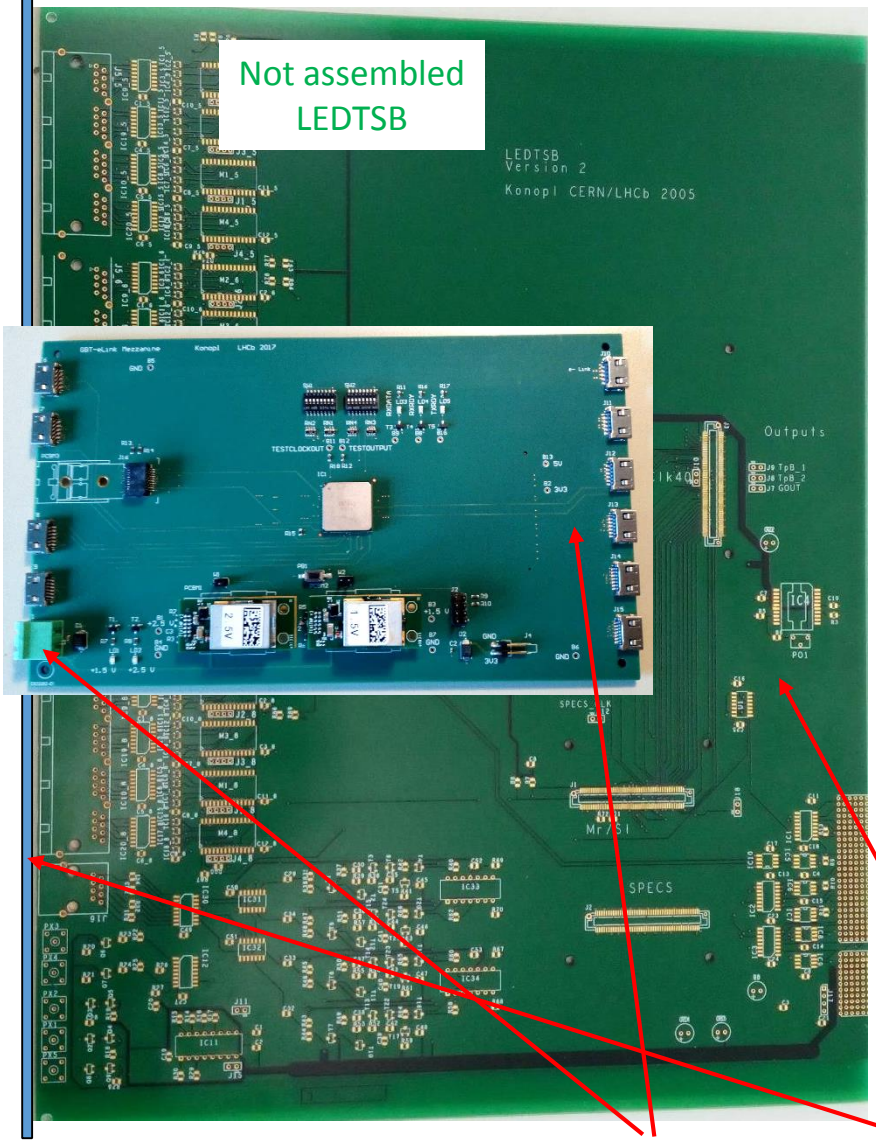
In total:

•HCAL has 4 ELDM cards (two at the platform and two at the chariot), each serving 2 HV-LED and 1 INTEG board. The ELDMs installed at the platform serve also one LEDTSB board each

•ECAL has in total 6 ELDM cards (4 at the chariot serving the HV system and 2 at the platform serving LEDTSBs).

- **The ELDM board has been designed and two prototype cards have been produced**
- **The validation test of the ELDM card has been done at CERN with the LHCb MiniDAQ system (many thanks to Federico Alessio for help in the test organizing and creating all needed configuration files)**

ELDM card specification and installation in front-end crate



The ELDM mezzanine card is equipped with GBTx ASIC, VTRx module, two CERN voltage regulators and ten HDMI connectors for the e-Link distribution. Functionally, this card is a reduced version of the CERN VLDB board, chosen as a reference design (GBT-SCA part of the VLDB is excluded). Dimension of the card is 120 x 205 mm. The PCB of the card has 10 layers and is equipped with two connectors for powering from an external power supply or a crate back-plane.

LED monitoring slow control electronics, as was mentioned, needs four E-Link distributor inserted into FE crates.
The ELDM card has been designed taking into account possibility to install this card in a standalone version and in crate version.

The existing spares (not assembled) LEDTSB boards could be used as VME frame board for insertion an ELDM card into the front-end crate.
We have just five spares not assembled LEDTSBs and planning to use them

Not assembled LEDTSB should be equipped with two connectors and front-panel

E-Link Distributor Mezzanine card validation test

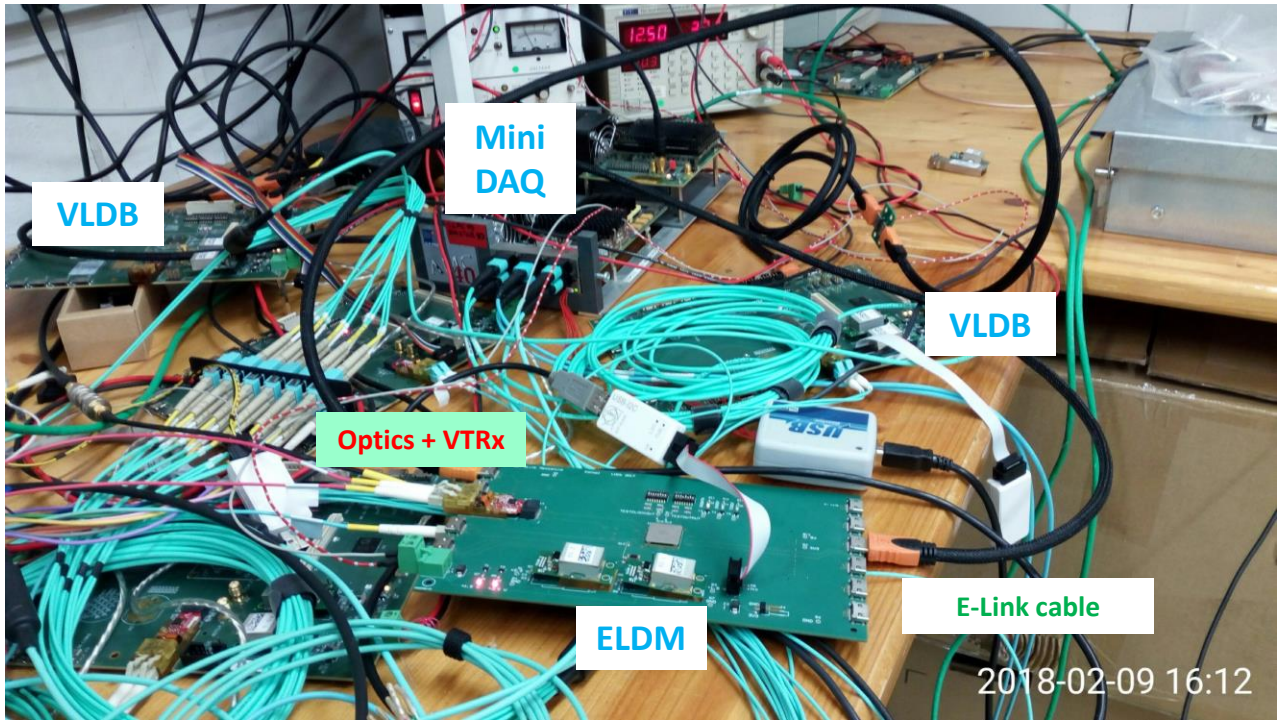
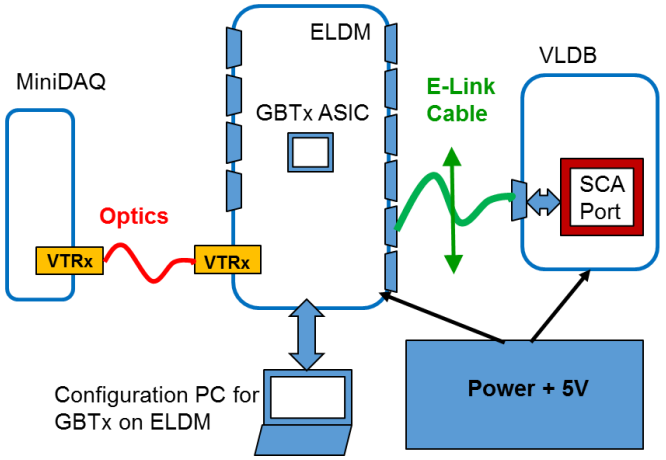


Photo of the MiniDAQ Test bench for the ELDM mezzanine card test



Schematic of the MiniDAQ Test bench for the ELDM mezzanine card test

- Final validation test of the ELDM card was done with MiniDAQ system organized at CERN by the LHCb developer group
- The updated version of the MiniDAQ firmware and needed configuration file for the GBTx ASIC of the ELDM card have been prepared and tested by Federico
- LHCb ECS control system based on the WinCC OA software was used for performing the write/read operations of the VLDB registers
- Hardware validation test of the ELDM card was successful. This card is ready for mass production
- The dedicated to ELDM configuration file was created and checked too

Summary of the production readiness of the e-Link distributor – ELDM card

- ✓ Specification of the ELDM card met the initial design of the upgraded systems.
- ✓ ELDM card is simplified version of the CERN VLDB board which is widely tested in CERN community
- ✓ Prototype of the ELDM card has been tested at CERN with MiniDAQ and ECS software.
- ✓ The production tests are foreseen on the MiniDAQ test-bench which organized and operates at LAL.
- ✓ In time of the prototypes fabrication the design has been inspected and approved by manufacturer - “EuroCircuits” company.

Prototype production and mass production readiness

Five types of the prototype mezzanine cards were produced on two PCB manufacturing companies. One is the Russian company

Москва, Почтовая Б., д.26 В, стр.2, офис 406	PCBtechnology
Тел./факс: (499) 558 0254 (107)	
Web: http://www.pcbtech.ru	
E-mail: pcb@pcbtech.ru	

Second one is European company

Eurocircuits N.V.

Antwerpsesteenweg 66
2800 Mechelen
Belgium

Directors: Dirk Stans, Luc Smets
VAT No. BE 0 444 188 140 - RPR Mechelen
BNP PARIBAS FORTIS BANK, Vital Decosterstraat 42, 3000 Leuven, Belgium
IBAN: BE66 2300 3095 5043
BIC Code: GEBABEBB

Prototype production and mass production readiness

Both companies have similar technology and can fabricate high quality PCBs.

Main capabilities of the PCB manufacturers:

- ✓ **Up to 16 layers, from 1 piece onwards**
- ✓ **100µm – 4mil technology at pooling prices; 0.090 µm – 3 mil non-pooled**
- ✓ **fully-finished with 2 solder-masks and 1 or 2 silk-screens**
- ✓ **Many technical options available**
- ✓ **No tooling charges**
- ✓ **No minimum order charge**
- ✓ **100% manufacturability check prior to production**
- ✓ **100% electrical test on all boards**

All prototype mezzanines were tested and we did not find any problem with the PCB quality.

PCB production and components assembly planning

Production plan

PCB production of the mezzanine cards for HV, LED and Cs calibration systems

- adapterMez_010-HV – 54 pcs
- adapterMez_025-LED – 12 pcs
- scaHV_Mez02 – 54 pcs
- scaLED_Mez02 – 12 pcs
- Manufacturing will be done by **PCB-Technology** company. The offer is obtained already. Production time is about 2 months

PCB production of the E-Link Distributor boards

- eLink_Mez– 12 pcs
- Manufacturing will be done by **Eurocircuits N.V.** company. The preliminary offer is obtained already. Production time is about 1 months

Components ordering and PCBs assembling

- Main active components (GBT ASICs, IGLOO2 FPGAs and power regulators) have been ordered few weeks ago and will be delivered in two weeks.
- All PCBs will be assembled in 1 – 2 months

Post production tests planning

Post production tests plan

Firmware upload and the validation test of the control mezzanine cards for HV, LED and Cs calibration systems can be started immediately after the cards assembly. The existing test bench with the SPECS system will be used.

adapterMez_010-HV – 54 pcs
adapterMez_025-LED – 12 pcs
The tests will be performed by me with possible assistance of one student.
Estimation time for these tests is about 1 - 2 months

The validation tests of the mezzanine cards providing the interface from the detector front-end to the experiment ECS system could be started immediately after the cards assembly. The existing test benche with the MiniDAQ system and test bench based on Xilinx evaluation kit will be used .

scaHV_Mez02 – 54 pcs
scaLED_Mez02 – 12 pcs
eLink_Mez– 12 pcs
The tests will be performed by me with possible assistance of one student.
Estimation time for these tests is about 1 - 2 months

Production Readiness Review report for HV, LED Monitoring and Cs Calibration systems

Conclusions

- Hardware design for the CALO HV and HCAL Cs calibration systems has been validated and prototypes of the controlling and interfacing mezzanine cards were fabricated
- Extensive tests were performed on the test-bench and at the LHCb pit with HCAL
- First version of the FPGA firmware has been developed and used in the tests
- The firmware optimisation will be continued
- These mezzanine cards are ready for production and the offer for manufacturing has been obtained

- Hardware design of the LEDTSB mezzanines those are a heart of the CALO LED monitoring system and the prototype production has been finished
- Test bench for the prototype study and it's validation has been prepared and main functional tests been passed
- First operating version of the FPGA firmware has been developed and used in the tests
- The firmware optimisation should be continued
- These mezzanine cards are ready for production and the offer for manufacturing has been obtained

- ELDM mezzanine card development has been finished and the prototype card has been produced
- The hardware verification with the reference design - VLDB has been done and approved. The validation test was done and these mezzanine cards are ready for production

Production Readiness Review report for HV, LED Monitoring and Cs Calibration systems

References

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