Design and characterisation of HV/HR-CMOS sensor chips for the CLIC vertex and tracking detectors

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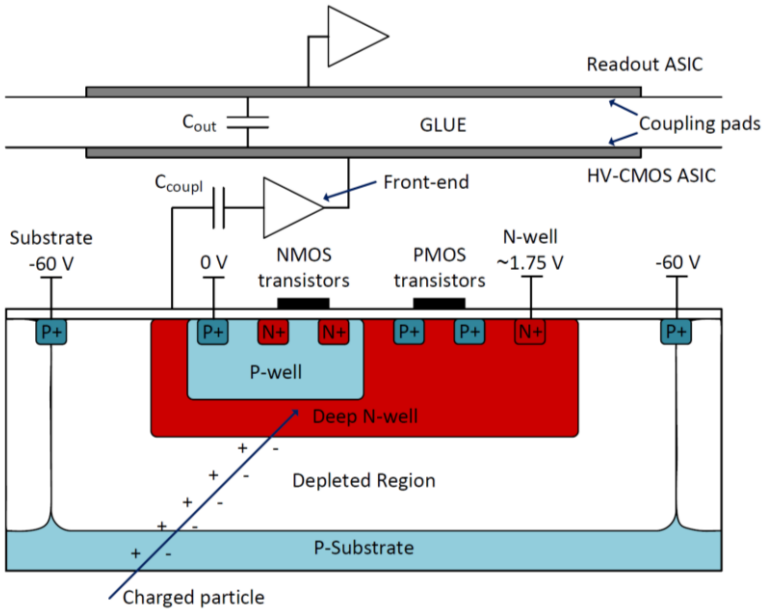
Part I:

Characterisation of capacitively coupled assemblies for the CLIC vertex detector

Introduction to capacitively coupled pixel detectors

- High-Voltage (HV) CMOS sensors:
  - All electronics are placed in a deep N-well, which is also the collecting electrode
  - Due to the reverse applied high-voltage bias, a depletion region with a depth of $\sim 10\ \mu m$ is created under the collection electrode, which leads to fast signal collection through drift

- Capacitively coupled pixel detectors:
  - A thin layer of glue is applied between the sensor and the readout chip
  - The charge collected in the HV-CMOS pixel is amplified by an on-pixel Charge Sensitive Amplifier (CSA) and then transferred to the readout chip



- Two chips have been designed in the framework of the CLIC vertex detector studies
  - The CLICpix2 readout chip *[1]* (65 nm CMOS process)
    - Simultaneous time (8-bit ToA) and energy (5-bit ToT) measurements, 10 ns time tagging
  - The C3PD HV-CMOS sensor chip *[2]*, (180 nm HV-CMOS process)
    - Produced on wafers with 20, 200 and 1000 Ωcm resistivity for the substrate
  - Both chips feature matrices with 128×128 square pixels, with $25\ \mu m$ pitch
  - Successors of a 1st generation of chips that have been tested in capacitively coupled assemblies *[3]*

[1] CLICpix2 User's Manual (E. Santin, P. Valerio and A. Fiergolski): https://www.overleaf.com/4621916xdqqmb#/13998870/
[2] CLICDP-PUB-2017-001 (I. Kremastiotis et al.): https://arxiv.org/pdf/1706.04470.pdf
[3] CLICdp-Pub-2015-003 (N. Alipour Tehrani et al.): https://doi.org/10.1016/j.nima.2016.03.072

Capacitively coupled assemblies

- Capacitively coupled assemblies with the C3PD HV-CMOS sensor glued on the CLICpix2 readout chip have been produced at Geneva University with an SET Accura 100 flip-chip machine

- The C3PD sensor chip has been produced in wafers with different values for the substrate resistivity
  - **Standard resistivity (20 Ωcm):**
    - First (laboratory and/or beam) tests performed with assemblies with the standard substrate resistivity for C3PD
  - **Higher resistivity:**
    - **1 kΩcm:** Two assemblies with **1 kΩcm** C3PD chips have been produced and tested in the laboratory.
      Assembly #10 tested in beam → analysis in progress
    - **200 Ωcm:** C3PD samples from a 200 Ωcm wafer have been received.
      First assembly is produced → testing in progress
    - The collected signal is expected to be larger for higher substrate resistivity *[4]*

- Laboratory and test-beam measurements of capacitively coupled assemblies were performed using the CaRIBOu data acquisition system:
  https://gitlab.cern.ch/Caribou

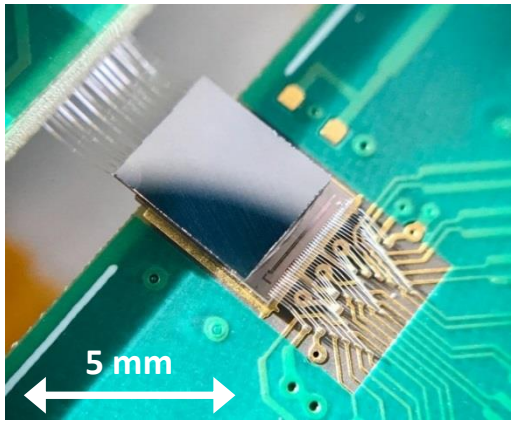
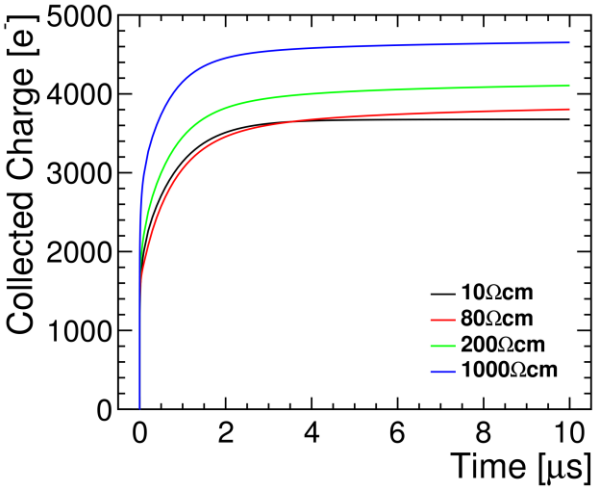


Photo: M. Vicente

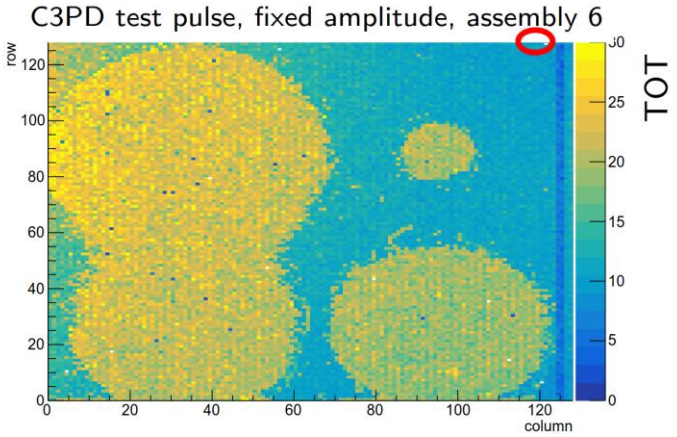


Simulated collected charge for different values for the substrate resistivity [4]

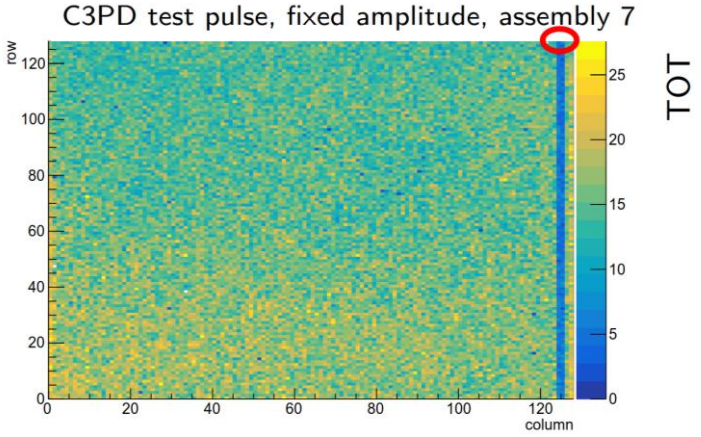
[4] CLICdp-Note-2016-004 (M. Buckland): https://cds.cern.ch/record/2159671/

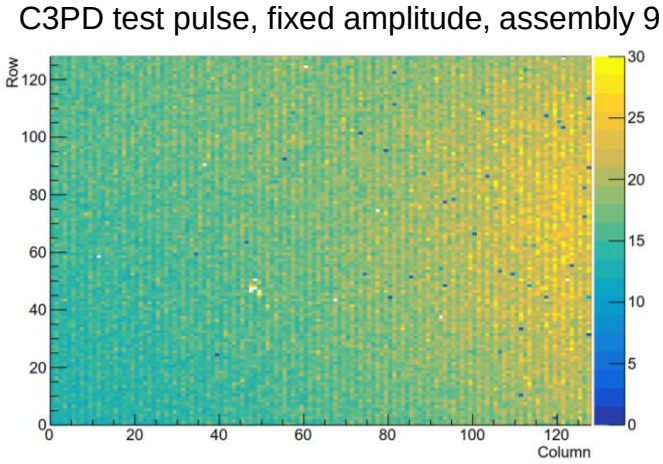
Coupling capacitance

- Test pulse injection in C3PD. Readout from CLICpix2
- Variations in response across the matrix have been observed in some assemblies
  - Non-uniform glue deposition, flip-chip misalignment

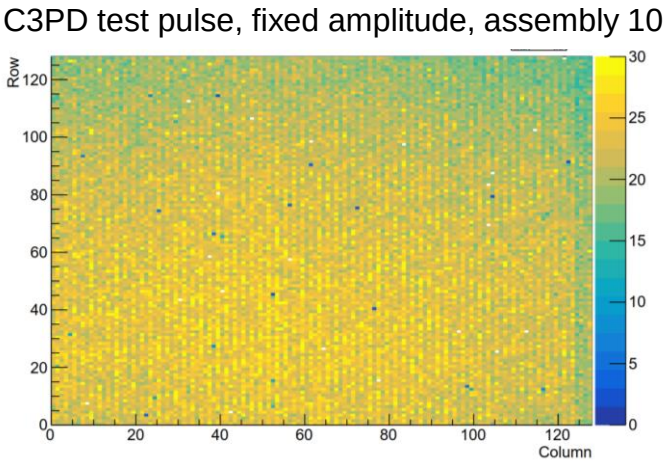


20 Ωcm





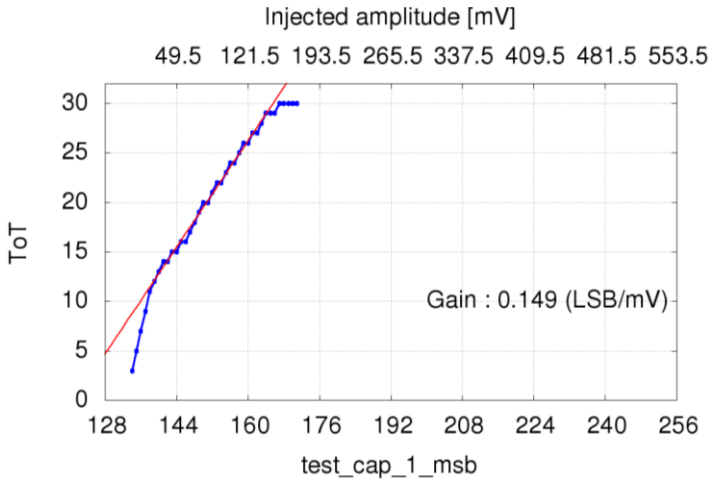
1 kΩcm

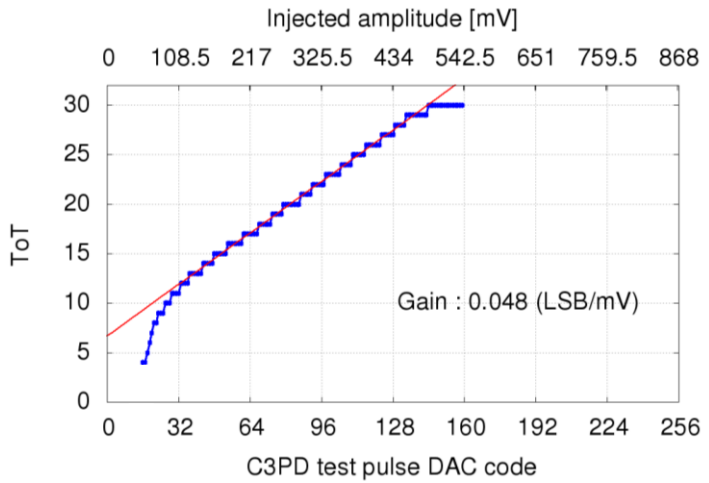


Assemblies with 200 Ωcm C3PD chips

- Low yield has been observed for the assemblies with the C3PD chips from the 200 Ωcm wafer
  - Low statistics: 1 out of 4 produced assemblies is functional
  - Short from power to ground, problems in powering observed for other assemblies as well as for bare C3PD chips from the same wafer
  - No similar issues have been observed for the first C3PD production, with the standard substrate resistivity (20 Ωcm)

- Preliminary results are available for the functional assembly (Assembly #17)
  - Test pulse injection in a single pixel in CLICpix2 (left) and C3PD (right)
  - For large signals, the ToT counter saturates



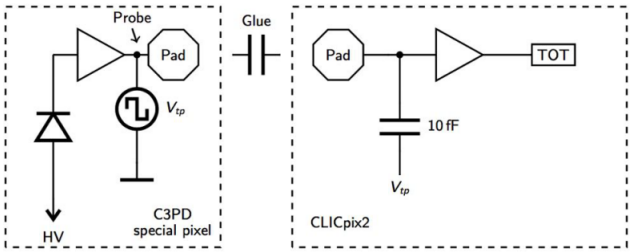


Measurements on coupling (glue) capacitance

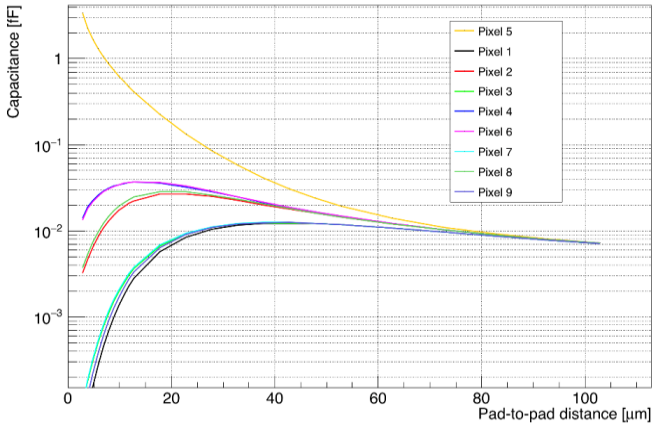
- Following destructive cross-section measurements on two mechanical samples, the pad-to-pad distance is ~3 µm, largely dominated by passivation layers
- The simulated value of the glue capacitance is ~3.5 fF *[5]*
- A “special” C3PD pixel where the injected test pulse signal is connected directly to the coupling pad, was used to measure the coupling capacitance between the two chips
- Using the design value for the CLICpix2 test pulse injection capacitance ($C_{test} = 10\ fF$), the coupling capacitance (C_{glue}) can be estimated:

Assembly #	C3PD Substrate Resistivity (Ωcm)	C_{glue} [fF]
1	20	3.66
6	20	1.43
7	20	2.95
9	1000	2.72
10	1000	2.63
17	200	3.20

C3PD / CLICpix2 test pulses



CLICpix2 + C3PD coupling simulation (M. Vicente)

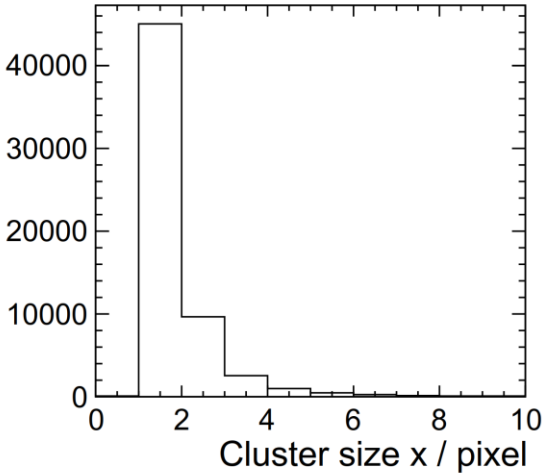


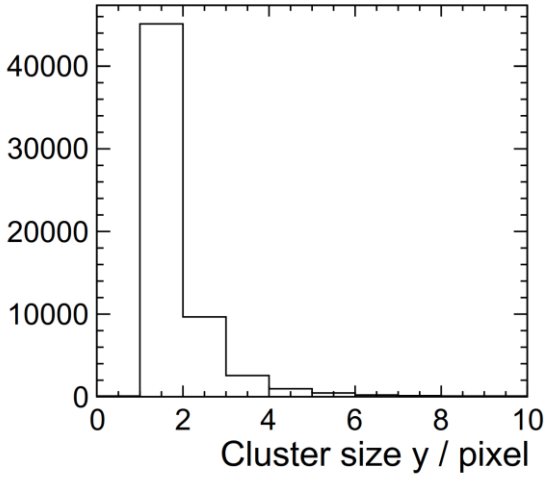
[5] CLICdp-Note-2017-003 (M.Vicente): https://cds.cern.ch/record/2267848/

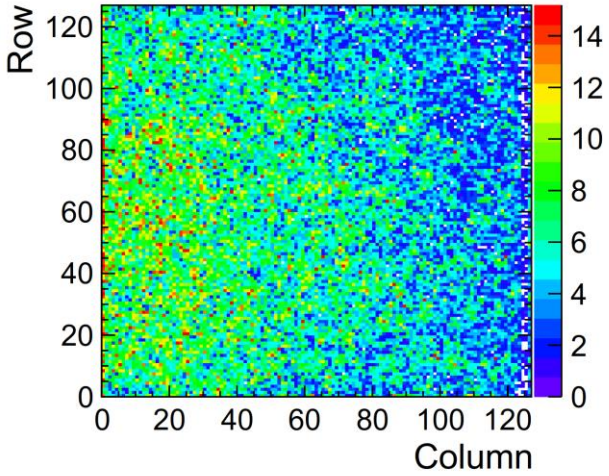
Measurements with ^{90}Sr source

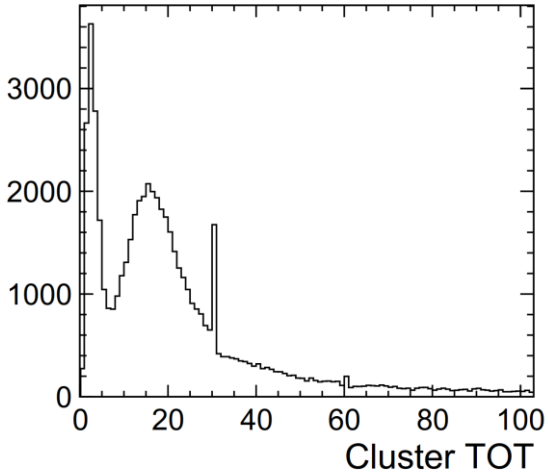
Particles from a ^{90}Sr source, read out from CLICpix2

Assembly #10:
CLICpix2 + ‘1 kΩcm’ C3PD









Summary and conclusions

- The CLICpix2 and C3PD ASICs have been tested in capacitively coupled assemblies:
  - Assemblies with higher resistivity C3PD samples are being tested
  - Higher resistivity C3PD chips show similar amplifier performance to the ones with standard resistivity (20 Ωcm)
    - Similar amplifier gain, noise, rise time
  - Larger and faster signal collection is expected for the capacitively coupled assemblies with higher resistivity C3PD
  - Variations in glue uniformity and alignment have been observed
  - CLICpix2 assemblies with planar sensors have been produced and tested.
    Please refer to Morag's talk for more information on planar assemblies

- Next steps:
  - Test beam analysis is on-going for the assembly with 1 kΩcm C3PD (#10)
  - Assembly with 200 Ωcm C3PD (#17) to be further tested in the laboratory

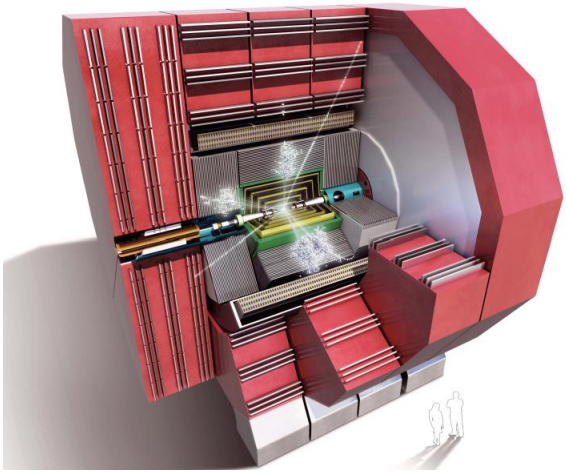
This work is a combined effort between CERN EP-LCD and EP-ESE-ME groups

Part II:

Design of a monolithic HR-CMOS sensor chip for the CLIC silicon tracker

Requirements

- Requirements for a chip for the Compact Linear Collider (CLIC) silicon tracker *[1]*:
  - Single point resolution in one dimension ≤7 µm (transverse plane)
  - Length of short strip/long pixel: $1 - 10\ mm$ (300 µm for the prototype, based on the minimum area required for the functionality)
  - Energy measurement with 5-bit resolution
  - Time measurement with 10 ns bin and 8-bit resolution
  - No multi-hit capability
  - Material budget 1-1.5% X_0 (i.e. ~200 µm for silicon detector and readout)
  - Power consumption < 150 mW/cm^2 (Power pulsing, duty cycle 156 ns / 20 ms)

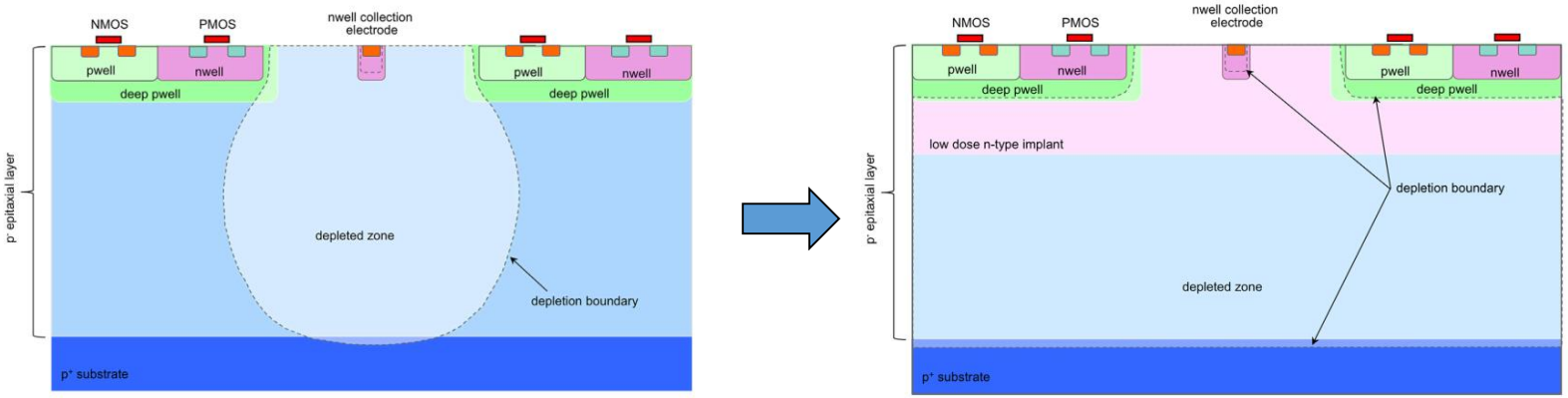


- CLIC Tracker Detector (CLICTD): Monolithic detector chip, targeted at the CLIC silicon tracker

[1] CLICdp-Note-2017-002 (D. Dannheim, A. Nurnberg): https://cds.cern.ch/record/2261066

The process

- The process selected for the CLICTD design
  - TowerJazz 180 nm High Resistivity (HR) CMOS imaging process
  - Small N-well as collecting electrode
    - Small detector capacitance → Lower analog power consumption
  - Circuits placed in deep P-well, separated from collecting electrode
    - NMOS and PMOS devices can therefore be used with this technology without being coupled to the sensor
  - Process modification: additional n-implant inserted to achieve full depletion
  - Successfully tested with monolithic pixel detector chips (e.g. ALPIDE, ALICE Investigator)

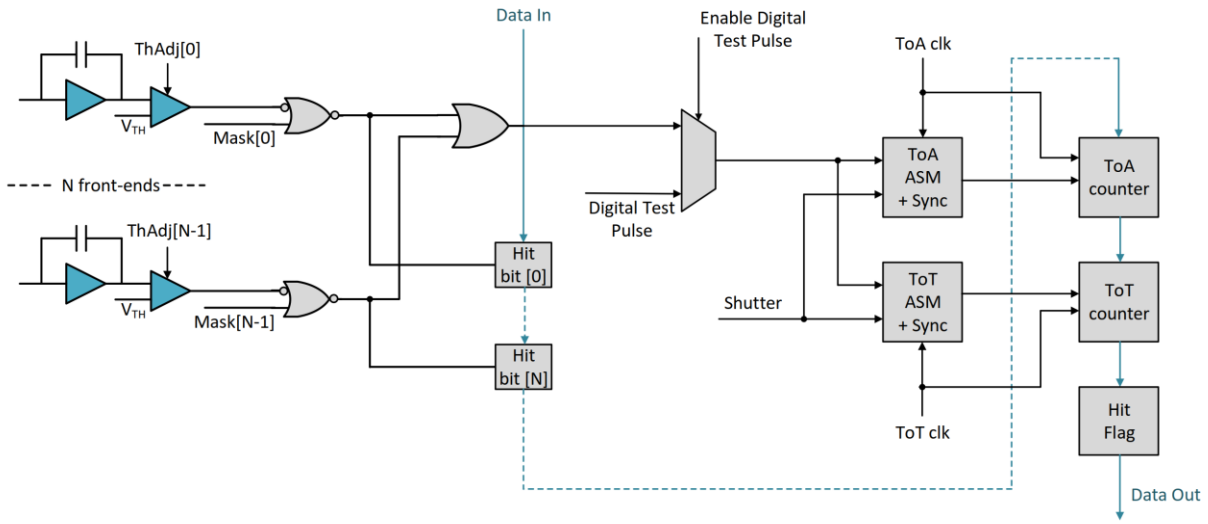


ORIGINAL PROCESS

MODIFIED PROCESS

The CLICTD channel

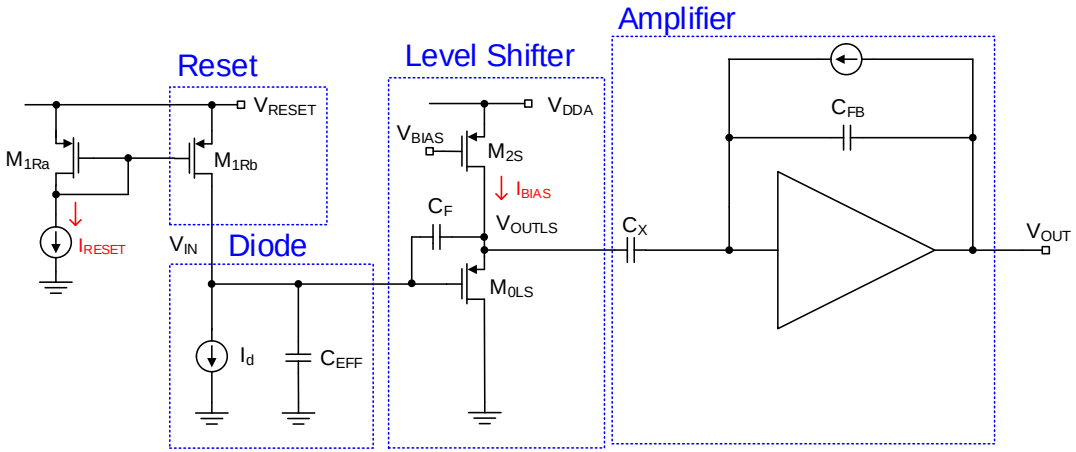
- The detector channel:
  - The detector unit cell consists of a short strip of $30 \times 300\ \mu m^2$
  - The analog part is segmented in 8 front-ends to ensure prompt charge collection in the diodes
  - Each front-end consists of:
    - The collecting diode
    - A charge sensitive amplifier
    - A discriminator
    - A 3-bit tuning DAC
  - Binary hit information is stored for each of the segments
  - Discriminated outputs are combined by means of an 'OR' gate
  - Time of Arrival (ToA – 8 bits, 10 ns time-stamping) and Time over Threshold (ToT – 5 bits) measurement is performed for the combined output



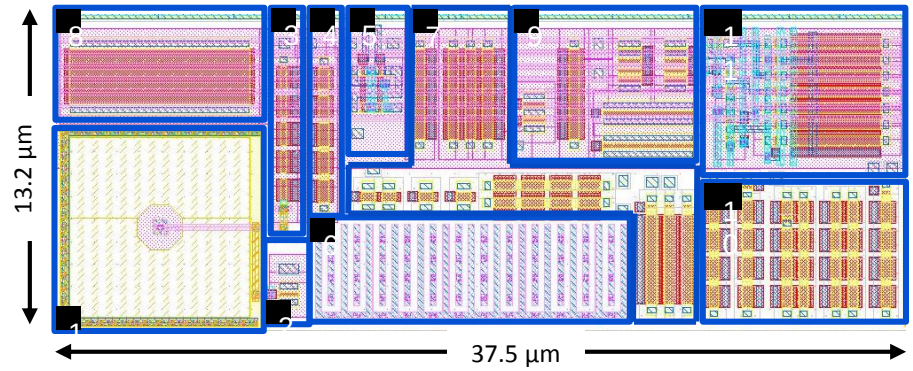
The CLICTD channel – Analog front-end

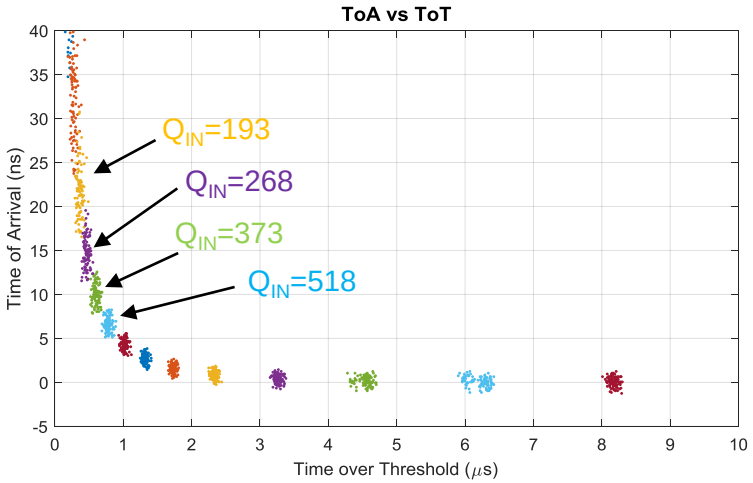
Level shifter, charge amplification and stage with linear TOT

$$V_{OUT} = \frac{Q_{DET} C_X}{C_{EFF} C_{FB}}$$



- Simplified first stage (Alpide approach, transistor reset)
- Signal amplification (xC_X/C_{FB})
- AC coupling between stages
- 1 power supply ☺
- Monotonicity in the ToA vs Q_{IN} ☺



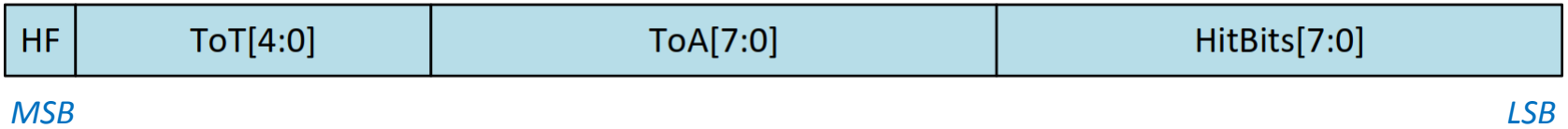


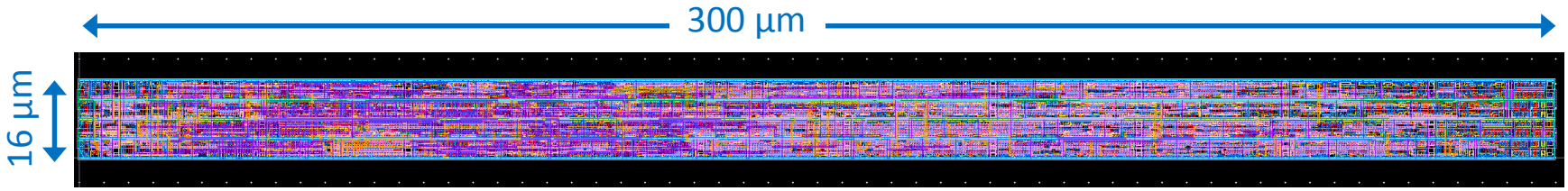
The CLICTD channel – Digital logic

- 3 modes of measurement:

Mode	Description
Nominal	8 bits timestamping information (ToA) + 5 bits energy information (ToT)
Long counter	13 bits timestamping information (ToA)
Photon counting	13 bits photon counting (number of hits that are above the applied threshold)

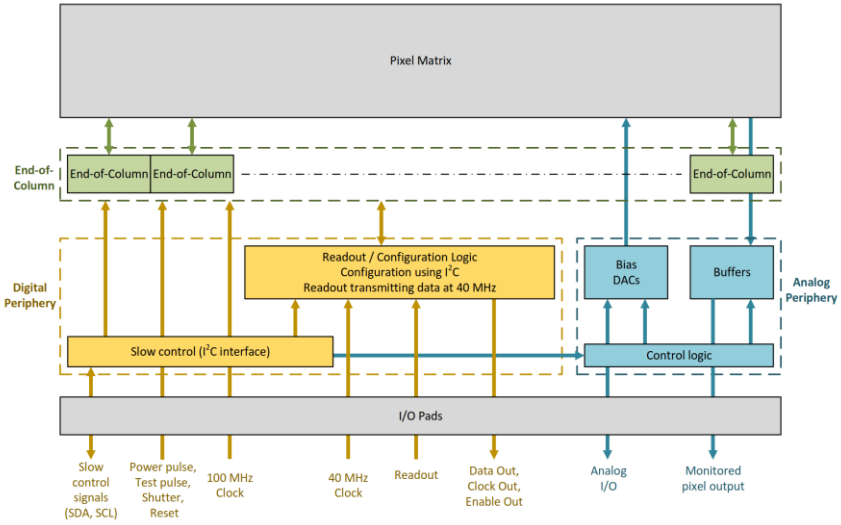
- During acquisition, a 100 MHz clock is provided to the matrix
- During readout, the data are shifted out at 40 MHz
- Readout with zero compression (at channel level) is available
- Total area for digital logic: $\sim 16 \times 300\ \mu m^2$





The CLICTD chip

- Total sensitive area: 128 rows and 16 columns ($4.8 \times 3.84\ mm^2$)



- Testability
  - Analog test pulse injection to individual front-ends
  - Digital test pulse injection to the input of the logic
  - Cluster of pixels monitored in the analog signal domain

- Power consumption (CLICTD matrix only)
  - Analog → Power pulsing
    - Analog power consumption in **continuous power mode:** $\sim 100\ mW/cm^2$
    - Front-end is set to "Power Off" mode between subsequent bunch trains (power can be reduced by a factor of ~50)
    - Average analog power consumption over the 20 ms cycle: $P_{analog,avg} \cong 2\frac{mW}{cm^2}$
  - Digital → Clock gating
    - Acquisition: clock is enabled only for channels that detect a hit
    - Readout: the clock is enabled only for the column that is being shifted out
    - Acquisition time: ~156 ns , Readout time: 500 µs (for $1\ cm^2$ matrix, 3% occupancy)
    - Average digital power consumption over the 20 ms cycle: $P_{digital,avg} \cong 3\frac{mW}{cm^2}$
  - Periphery power consumption not included in the above calculations
    - Preliminary estimation: $\sim 50\frac{mW}{cm^2}$ (continuous power, dominated by LVDS drivers' power consumption)

Work in progress

The CLICTD chip interface

- An I^2C interface is used for the slow control (reading/writing internal registers)
- Configuration data are shifted in the matrix using the slow control interface (I^2C)
  - A total of 41 configuration bits is shifted in per channel (in two stages, since the area does not allow for 41 flip-flops)
- A serial readout at 40 MHz will be used to shift the data out of the CLICTD chip
  - Compressed readout at channel level:
    - 22 bits are read out for cells that have been hit
    - 1 bit read out for cell that are not hit
  - ENABLE_OUT signal is used to synchronise with DAQ (along with clock output)
  - A 22-bit long header is added before the transmitted data of each column (and also at the beginning / end of frame)
- The CLICTD chip interface is designed to be compatible with the Caribou DAQ system

	Data per frame *	Readout time
No compression	45 kbits	1.12 ms
Pixel compression	3.7 kbits	93 µs

* Calculated assuming an occupancy of 3%
Matrix area: $4.8 \times 3.84\ mm^2$ (16×128 pixels)
Readout clock running at 40 MHz

Design status

- Pixel matrix:
  - Analog front-end and in-channel digital logic are designed
  - Physical verification (DRC/LVS) in progress
- Periphery:
  - Digital periphery blocks are designed. Layout to be finalised following chip integration
  - Analog periphery design in progress
  - Different blocks re-used from ALPIDE libraries (LVDS driver/receiver, I/O pads, bandgap …)
- Chip integration:
  - Digital-on-top
  - Analog periphery to be integrated
  - Further verification (physical and functional) to be performed once the layout is complete
  - Cluster with monitoring pixels to be added in the periphery. Cluster size to be defined
- Verification:
  - Full chip verification is being performed using the Universal Verification Methodology (UVM)
  - First tests are in progress, using the Verilog netlist
  - Tests using the post-layout extracted netlist will follow

Summary and next steps

- The CLICTD chip:
  - Simultaneous 8-bit ToA and 5-bit ToT measurement
  - I^2C interface used for slow control and for programming the pixel matrix
  - Serial readout with a clock frequency of 40 MHz
  - Data compression at channel level is available
  - Chip dimensions: $5 \times 5\ mm^2$
  - Sensitive area: $4.8 \times 3.84\ mm^2$ (16×128 channels)

- Next steps:
  - The chip is currently in the final design stage
  - Full chip verification is being performed using the Universal Verification Methodology (UVM)
  - Integration to be complete in the coming months
  - Submission is planned for ~November 2018