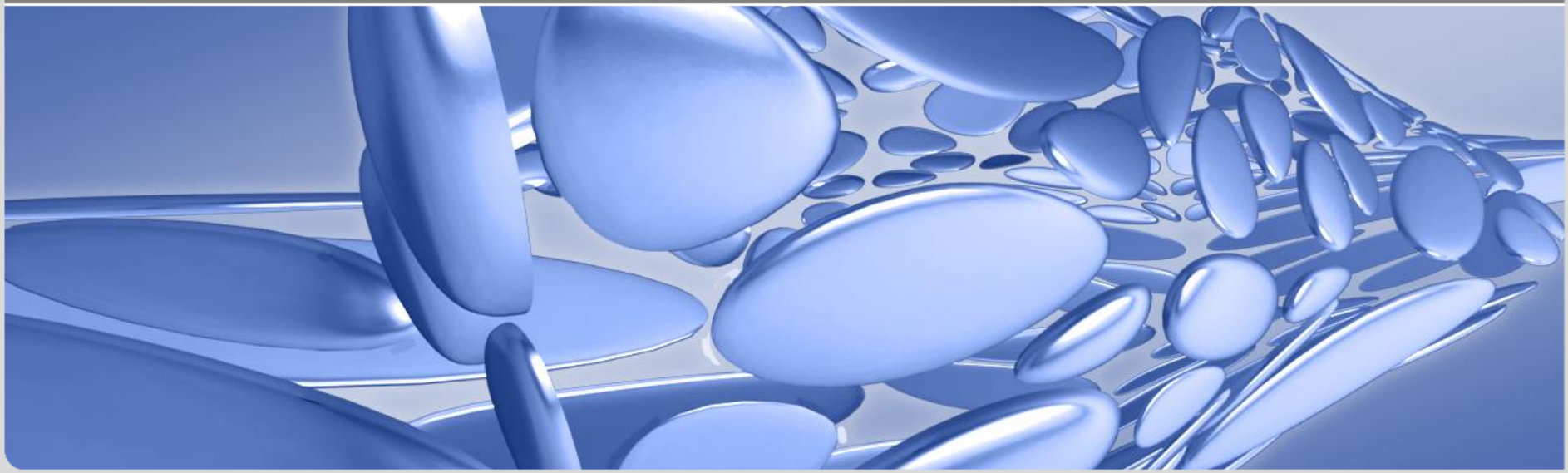
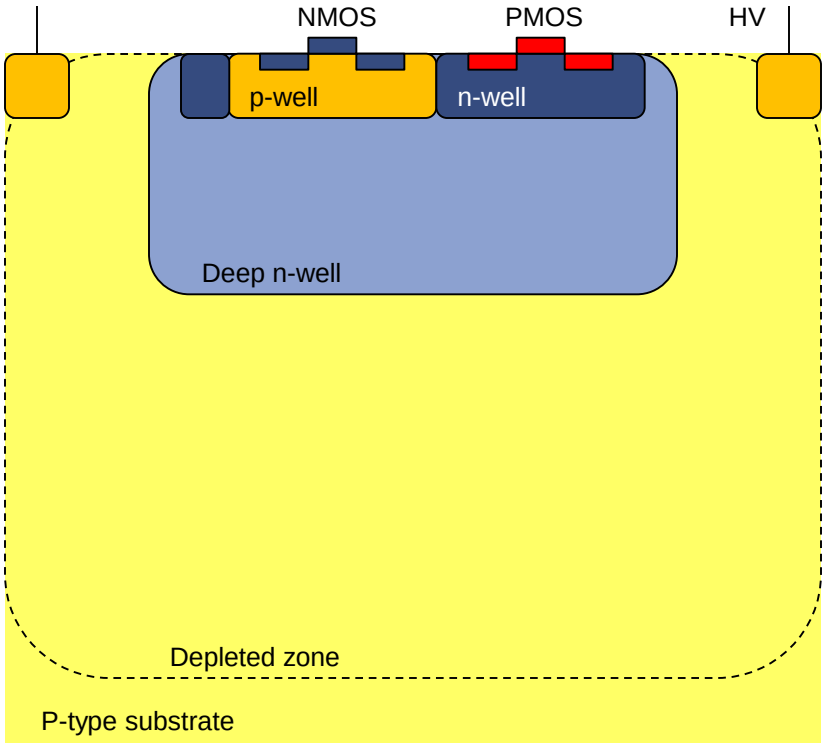
ATLASpix status and development of a version for CLIC

Ivan Peric



- ATLASPIX is a HVCMOS large area prototype for ATLAS
- Produced by AMS in 180nm HVCMOS process
- Submitted as engineering run
- Different substrates: standard, high resistivity
- 1. MuPix8 (area 1cm x 2cm)
- 2. ATLASPixM2 (area 3.5mm x 2cm)
- 3. ATLASPixSimple/ATLASPixIsoSimple (both: area 3mm x 2cm)
- The chips have been implemented on 4 different substrates: 10 Ωcm (standard substrate), 50-100Ωcm, 200-400Ωcm and 0.7-2kΩcm.

- HVCMOS sensors are monolithic depleted active pixel sensors in standard HVCMOS technologies
- Smart diode concept
- Pixel electronic placed inside the collection electrode
- Properties:
- Monolithic
- Fast signal generation and charge collection
- High radiation tolerance
- Cost effective production (no need for bumps)



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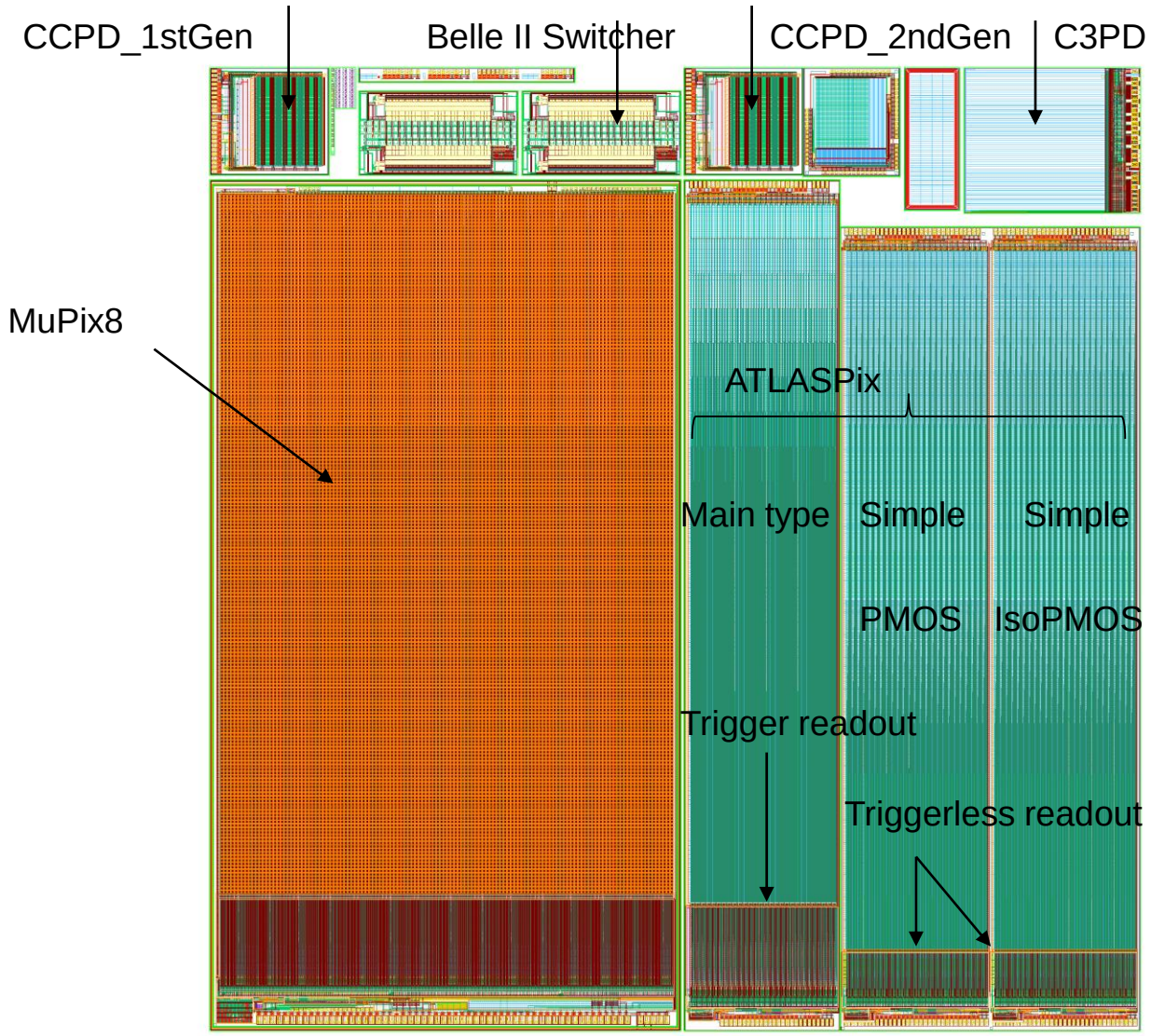

MuPix, ATLASPIX

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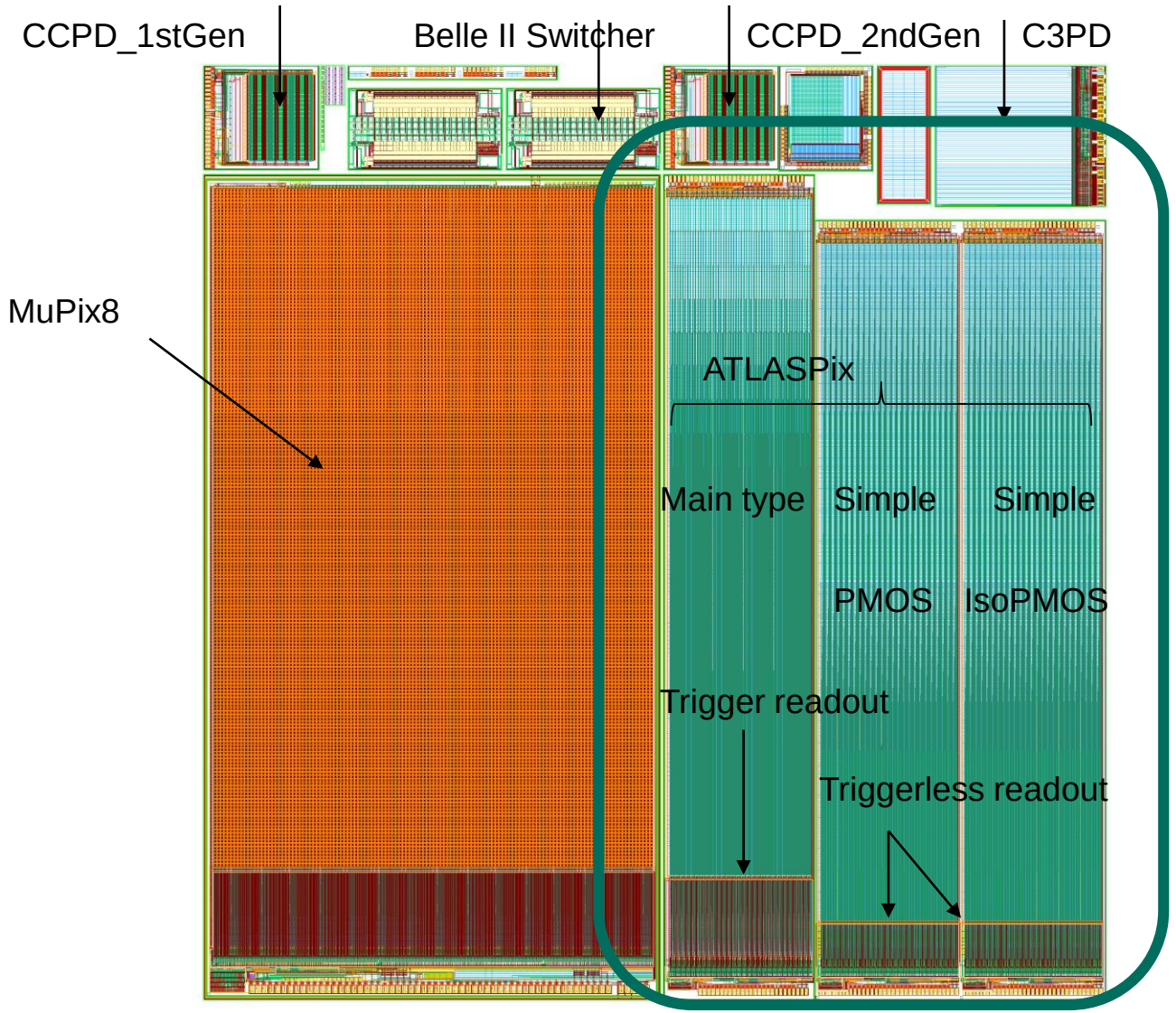
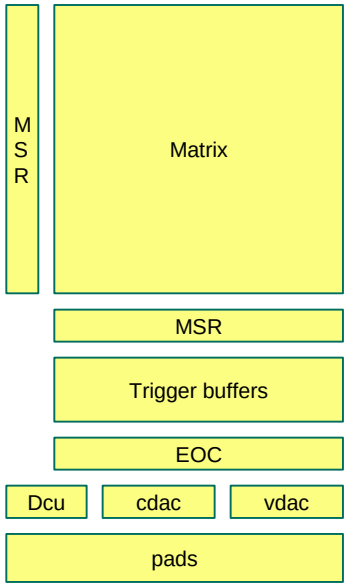
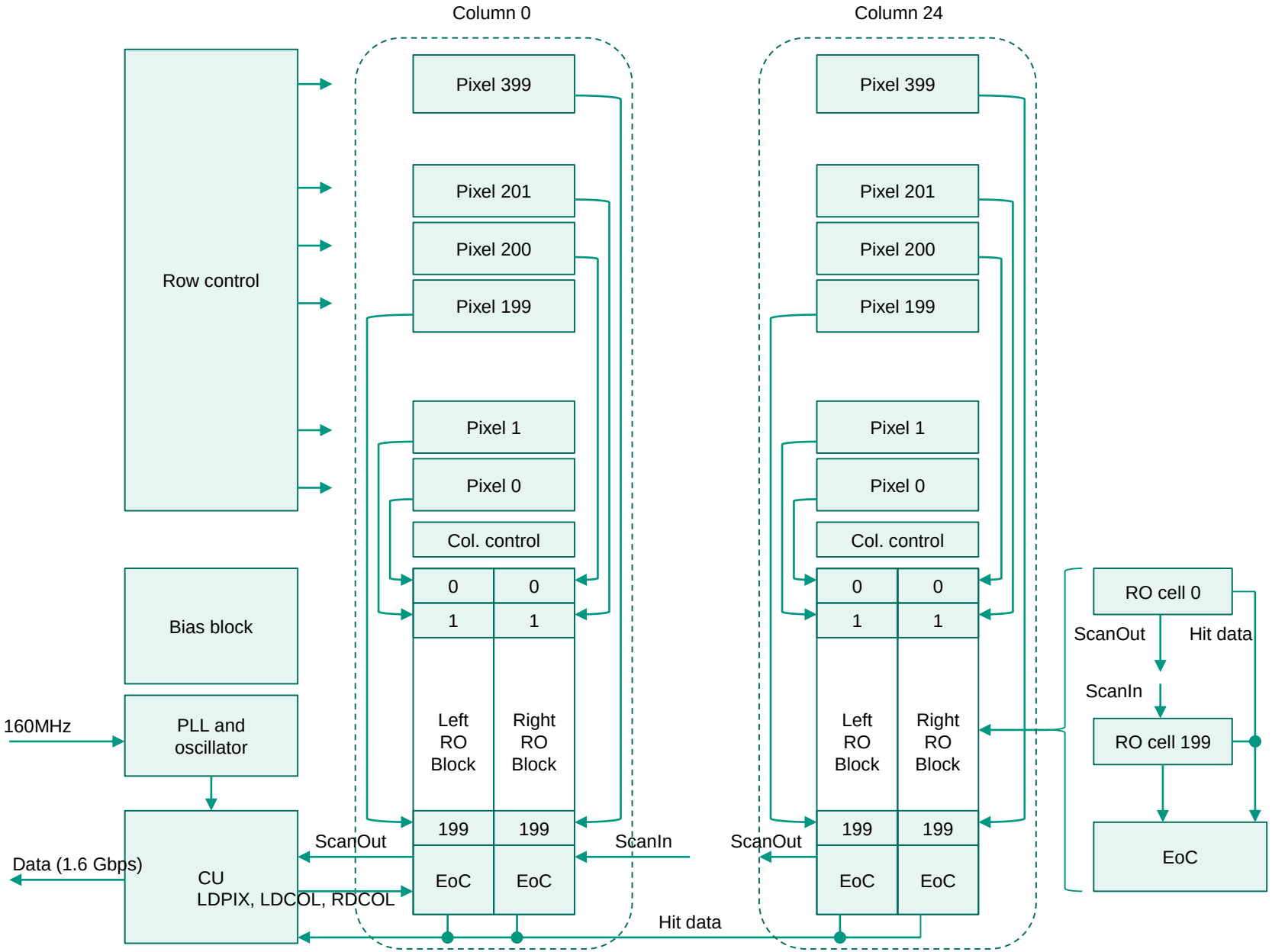


MuPix, ATLASPIX

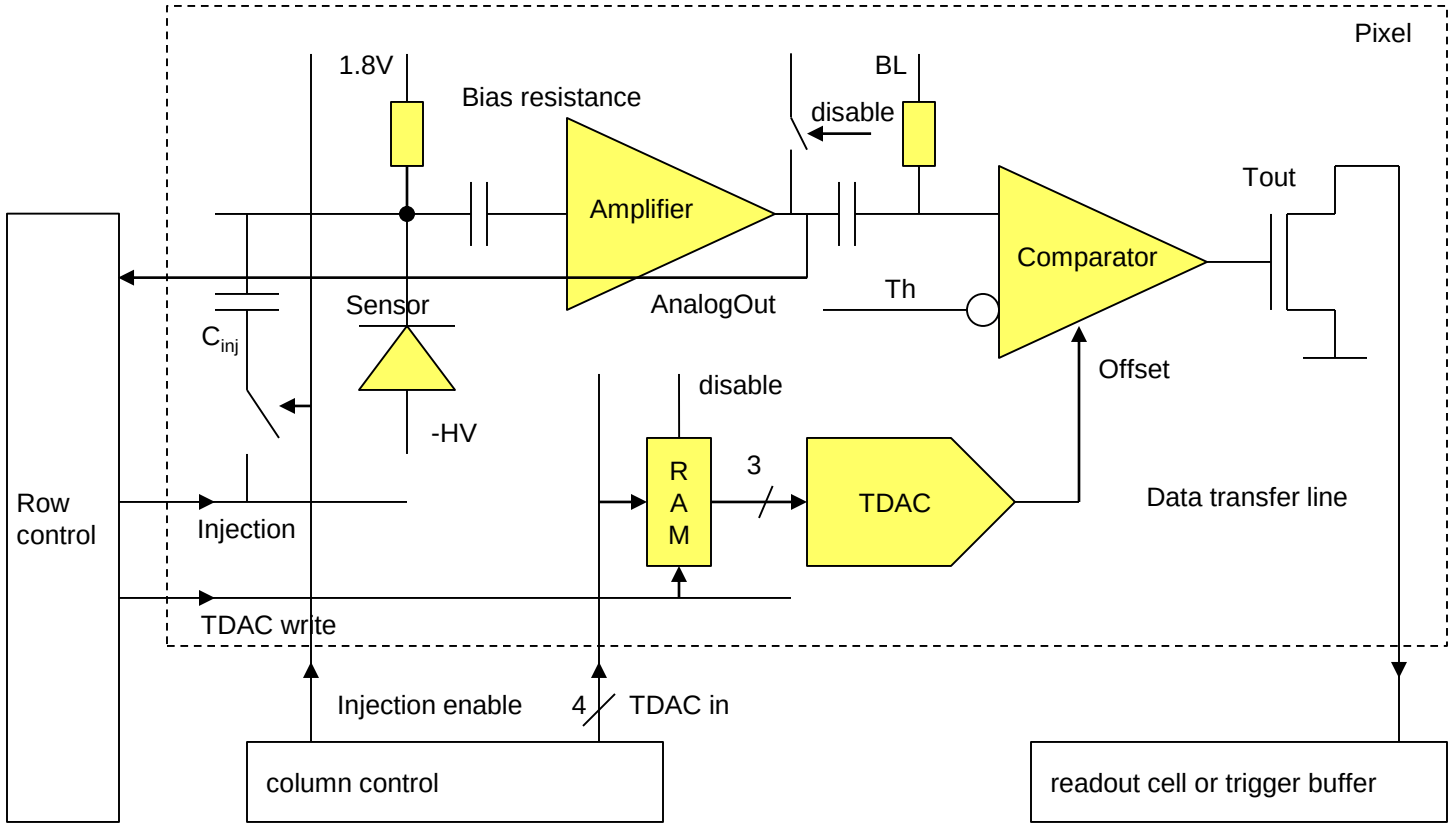
- ATLASPIX simple with triggerless (hit driven) readout

- Architecture of the chip
- Pixel matrix: 24 x 400 pixels of 40µm x 130µm size.
- Matrix control shift register (MSR) used to select pixels for injection, enable analogue output and hitbus (hitbus not implemented in M2) and write the pixel RAM
- Hit buffers that receive pixel signals and enable priority based readout
- EoC buffer to allow horizontal multiplexing
- Digital control unit (DCU), PLL
- Current-mode and voltage-mode DACs – they use shift register for configuration
- The DAC-SR, VDAC-SR, matrix-SR and a configuration-SR form a chain
- Pads

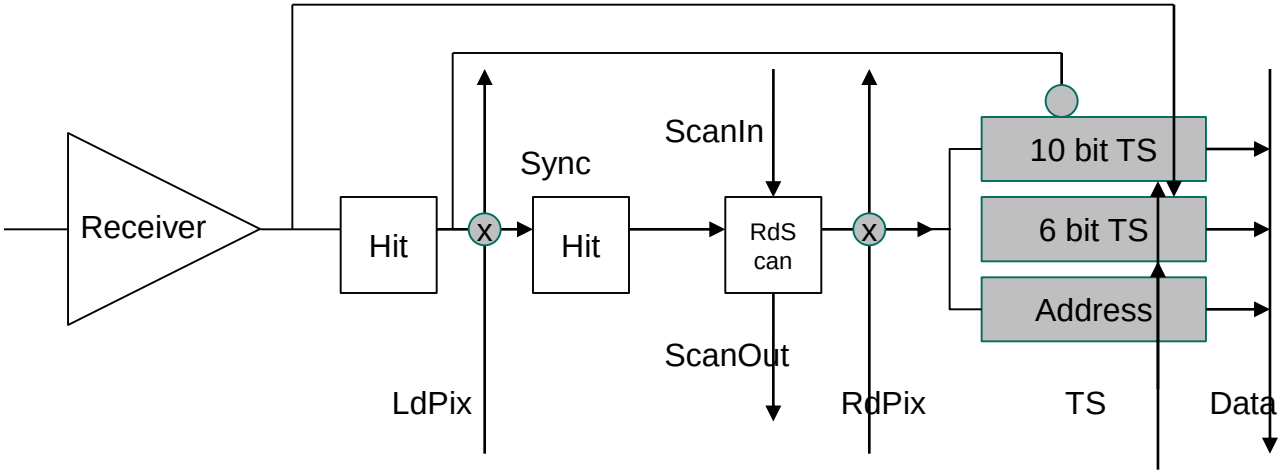



Column 0
Column 24
Row control
Pixel 399
Pixel 201
Pixel 200
Pixel 199
Pixel 1
Pixel 0
Col. control
0
1
Left RO Block
Right RO Block
199
EoC
Bias block
160MHz
PLL and oscillator
Data (1.6 Gbps)
CU
LDPIX, LDCOL, RDCOL
ScanOut
ScanIn
Hit data
RO cell 0
ScanOut
Hit data
ScanIn
RO cell 199
EoC

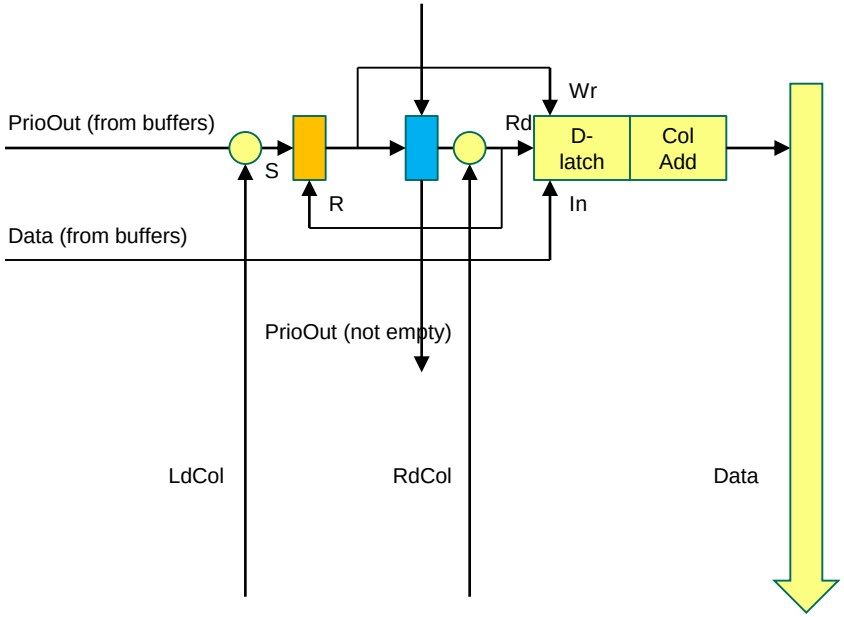
- Pixel contains sensor diode, charge sensitive amplifier, comparator, threshold tune DAC, RAM for tune bits (3) and disable bit and output driver
- The outputs of the pixels are transmitted to the column periphery (long metal lines)



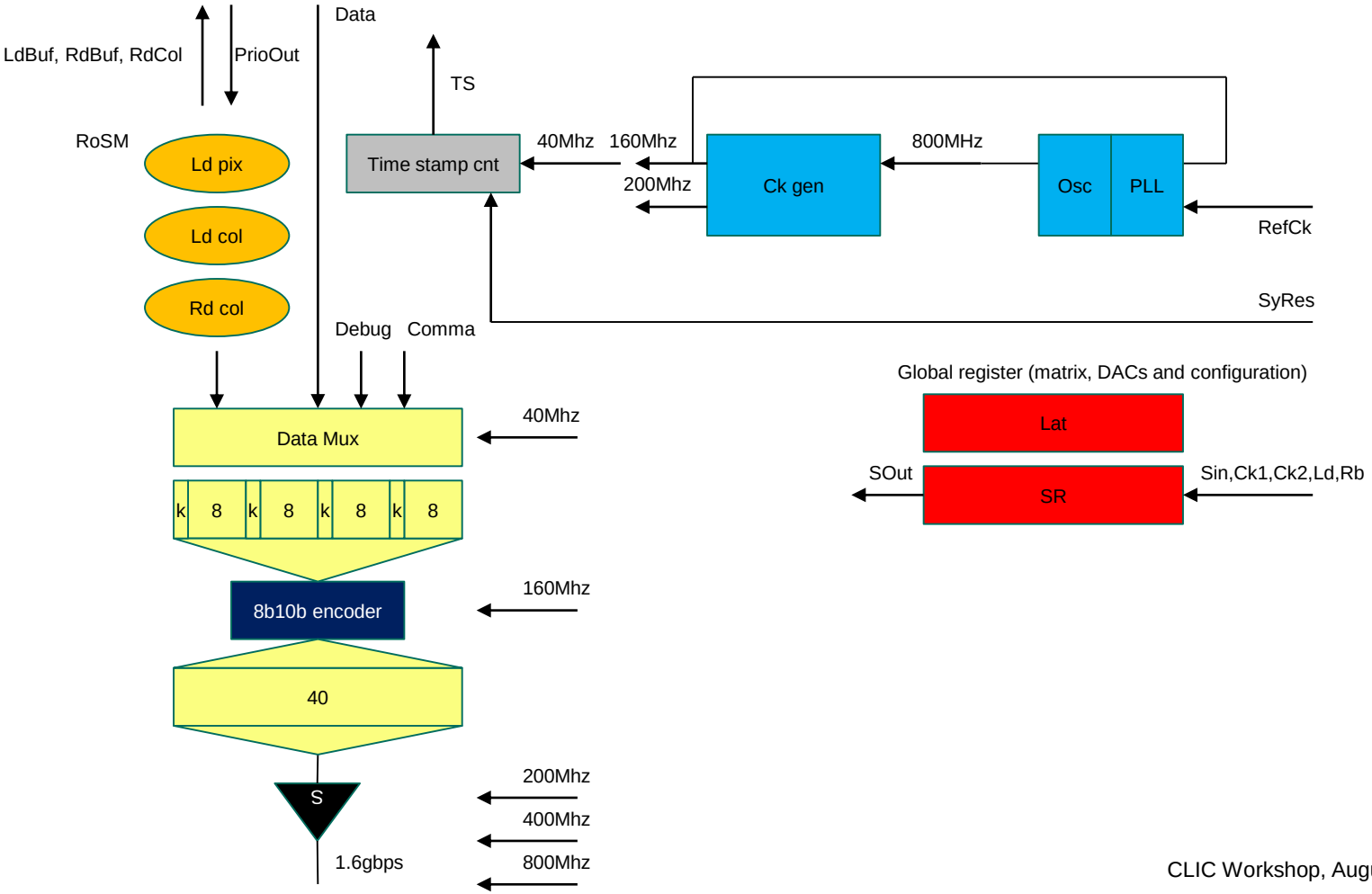
- Every pixel has its RO cell at the periphery
- Readout cell contains hit flag latch, timestamp memory (for leading edge time stamp and time over threshold), address generator, priority logic, bus driver



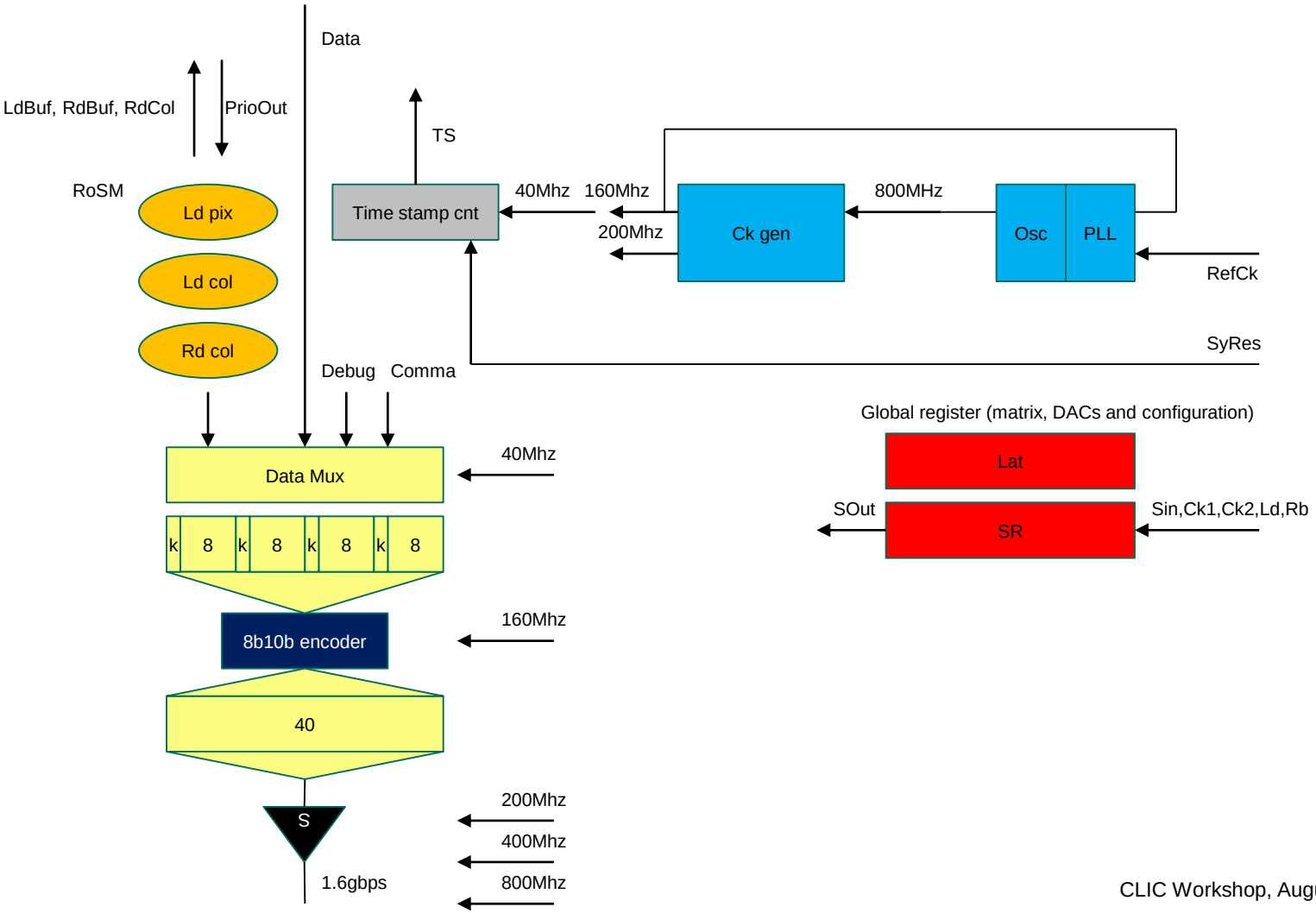
- By issuing read, the hits are transferred to EoC buffers. These EoC buffers are forming an active bus, they don't change the data received by triggered buffer they just add the column address to the hit data. The hits are transferred from EoC buffers by RdCol signal in a priority way – the same as used for hit buffers



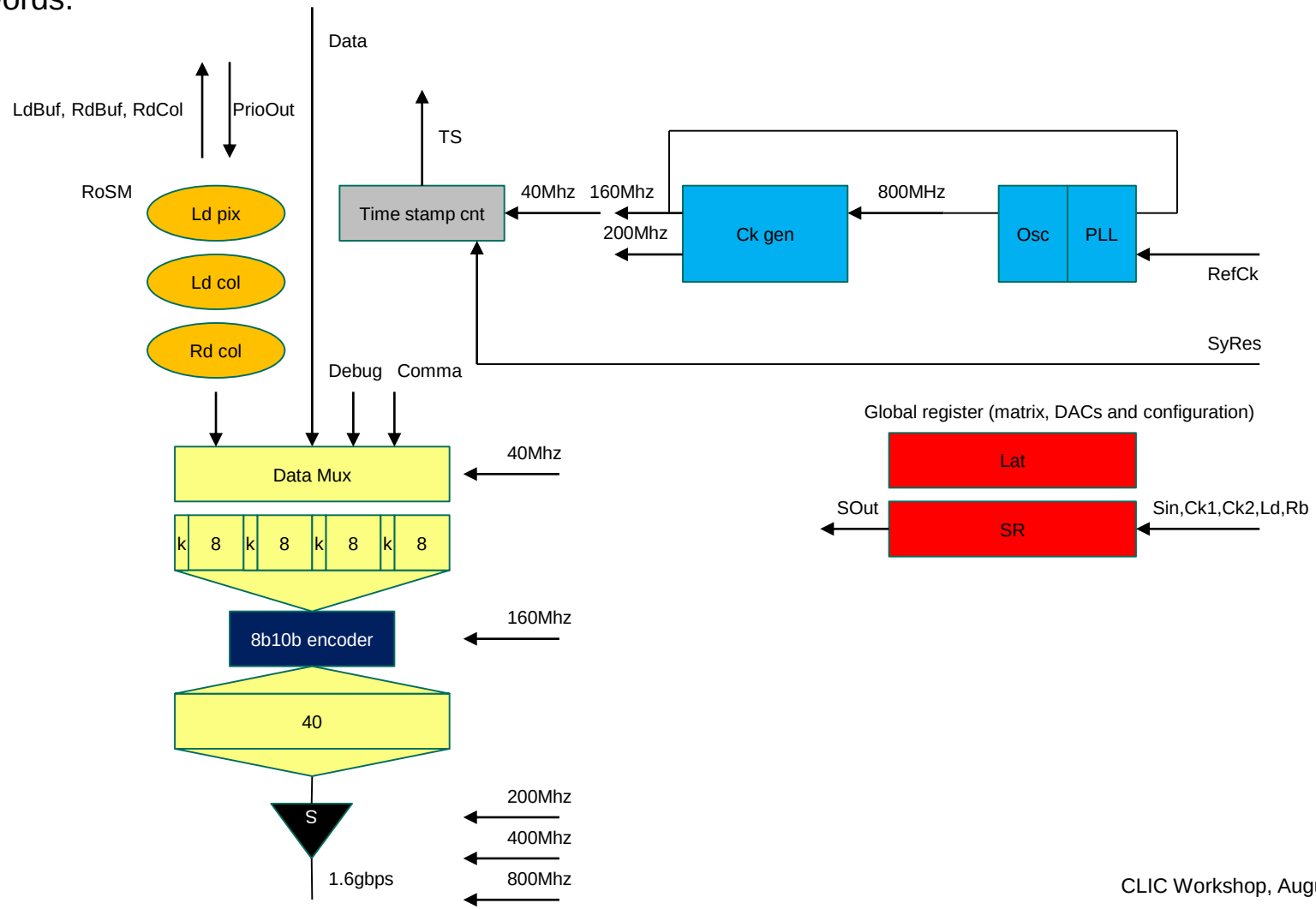
- Digital control unit generate the signals for the buffer readout: time stamps, Wr, trigger, RdBuf, LdBuf and RdCol. It receives and formats hit data and sends them using a fast link (1.6gbps).
- Digital control unit has the inputs: RefCk (160Mhz), for debug FastCk (800MHz), SyncReset, Trigger and fast output. There are many parameter bits (e.g. for changing of time stamp speed) that are stored in the configuration shift register.



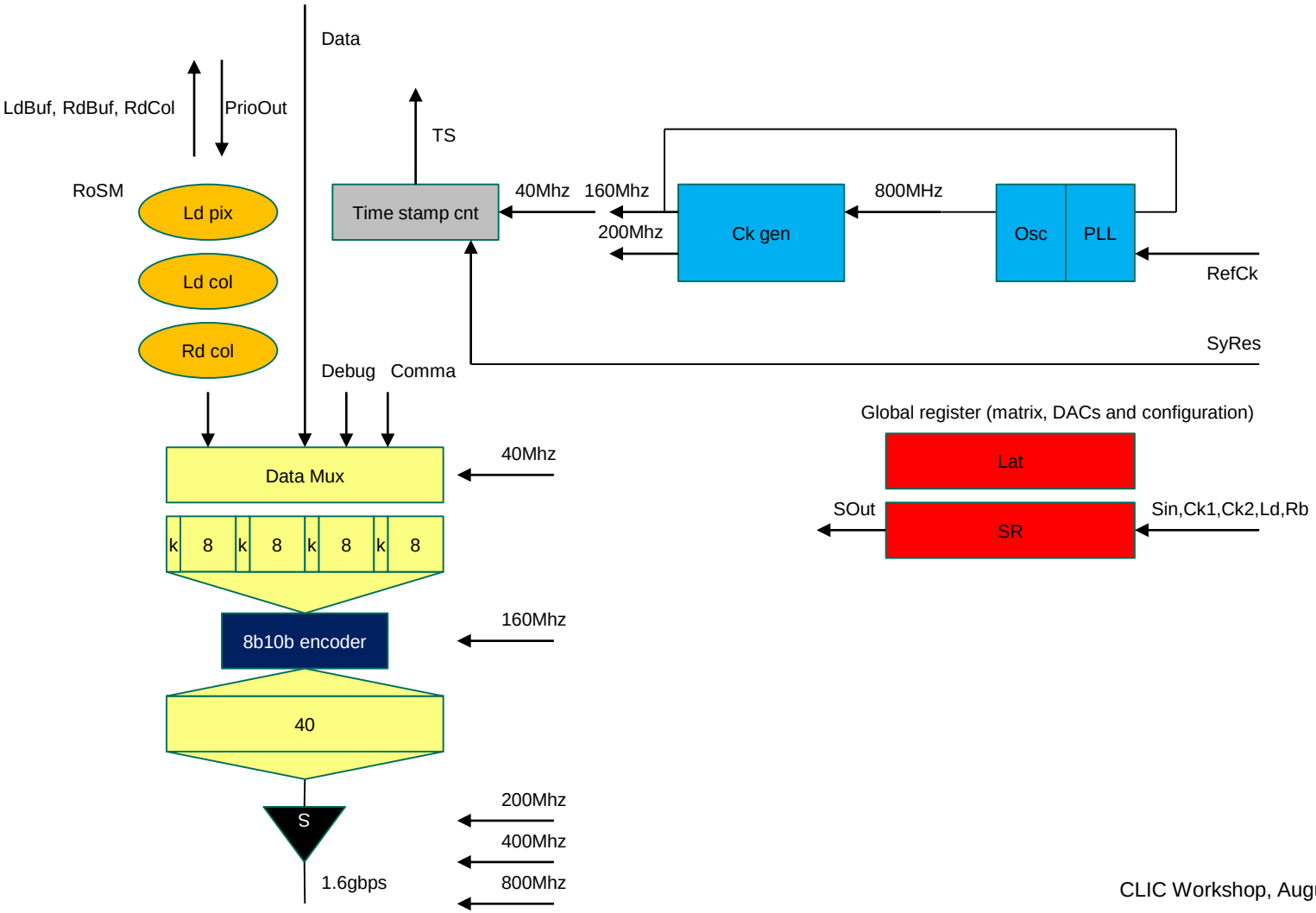
- Digital control unit contains following blocks:
- Clock generator that includes PLL and oscillator
- Time stamp counter



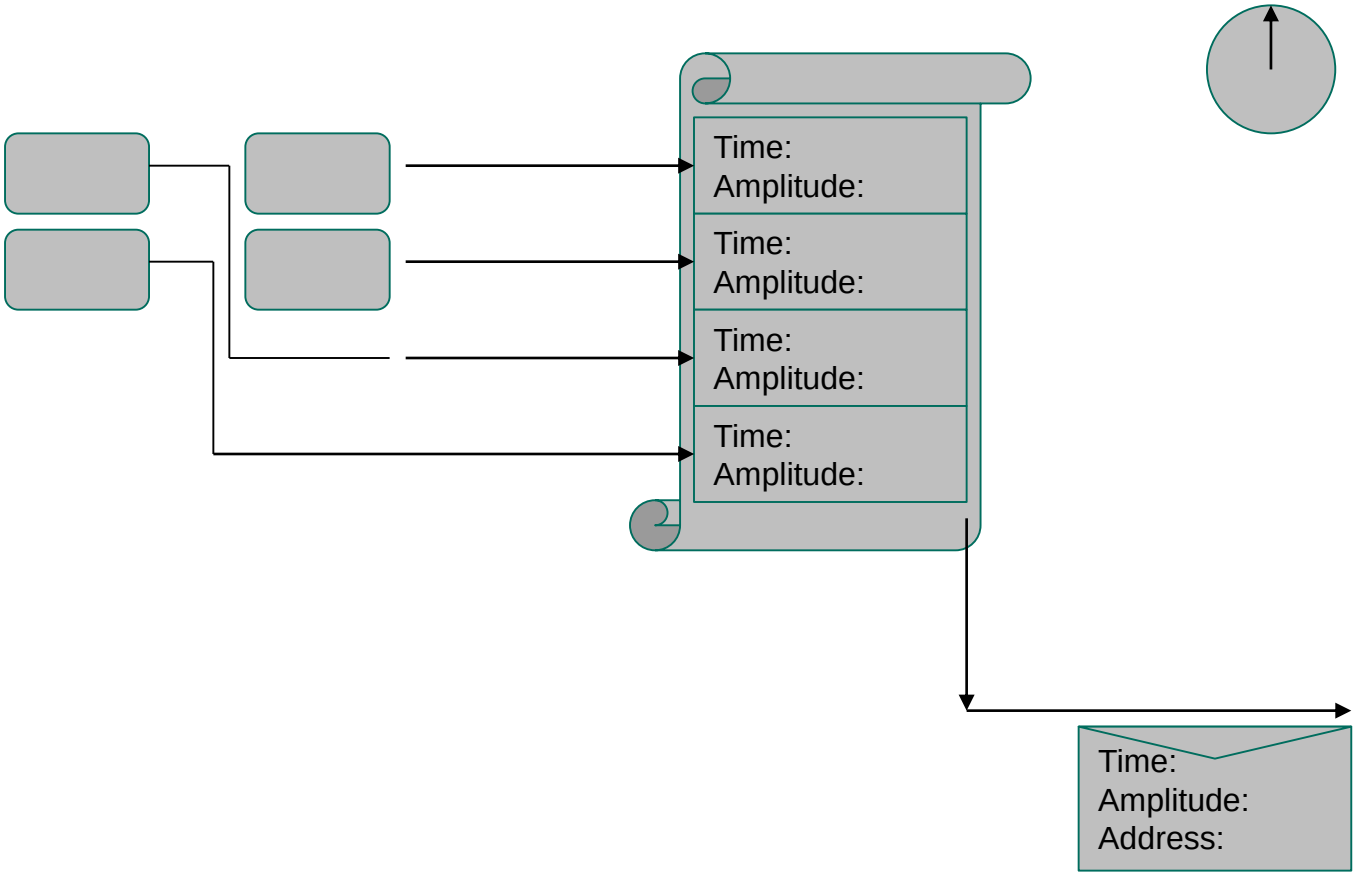
- Readout state machine. It receives the priority output from EoC cells (empty signal) and generate a sequence of LdBuf, RdBuf and then if EoCs are not empty, RdCol. The state machine also controls the data multiplexer and sends either the hit data, debug data or the comma words to the 8b10b encoder. The data are sent in RdCol states and in other states debug data or comma words.



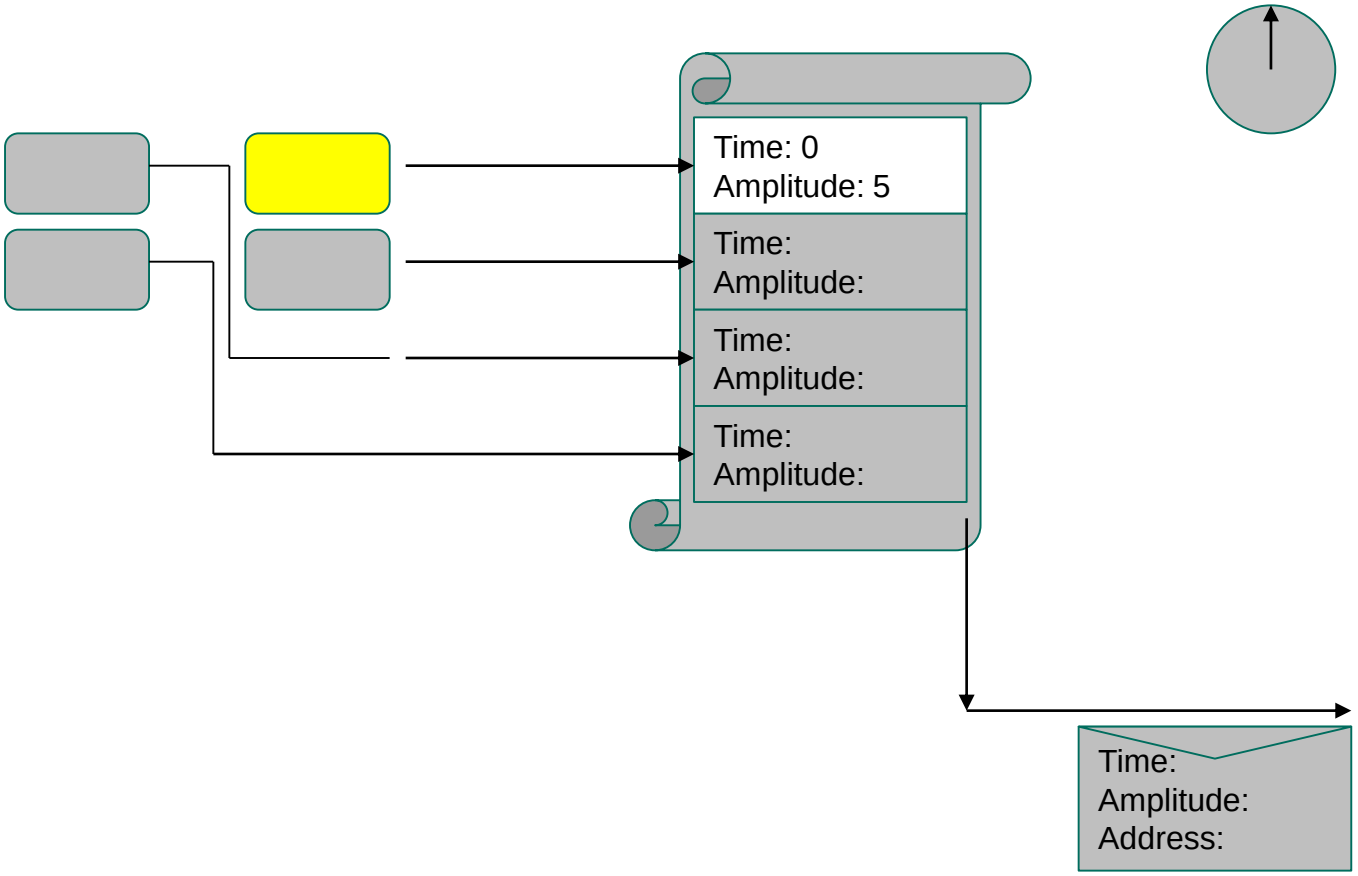
- Encoder: Custom made pipelined 8b10b encoder is used
- Serializer: Novel 8to1 serializer (S) based on binary tree is used to produce bit stream. Blocks of 4 words (40 bits) are sent to the serializer



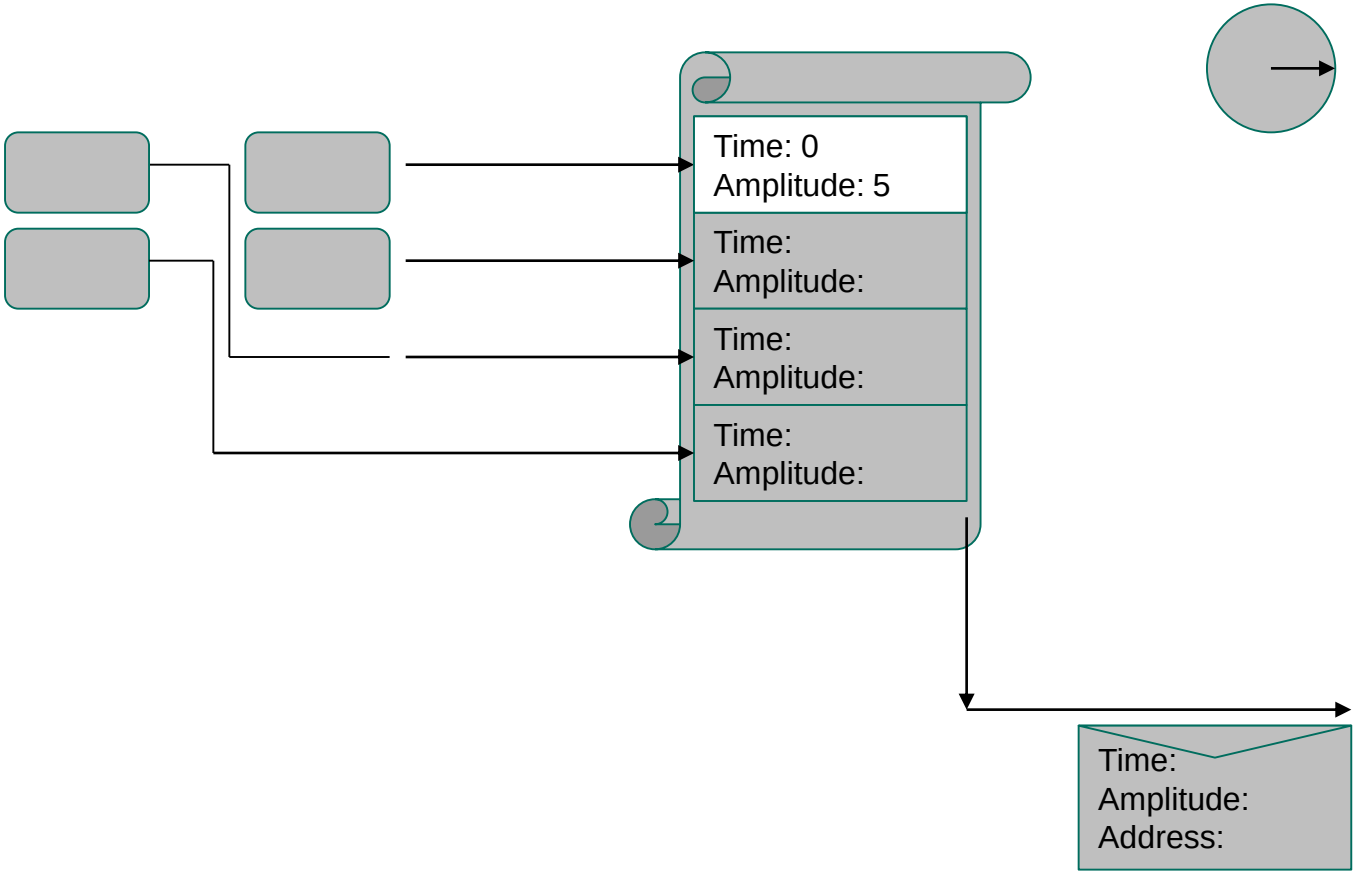
- Hit driven, trigerless, readout (MuPix8, Simple ATLASPix)



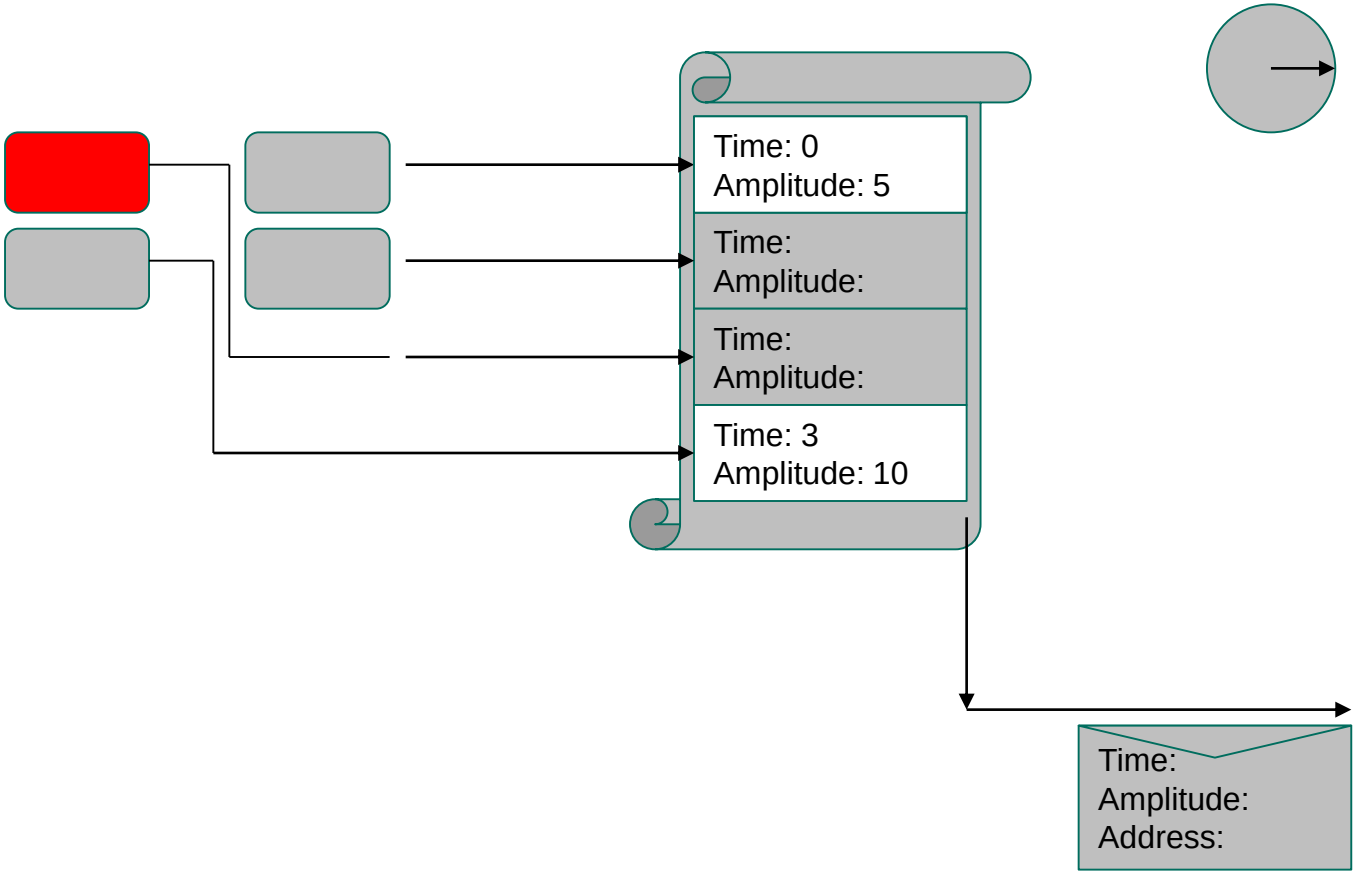
- Hit driven, trigerless, readout



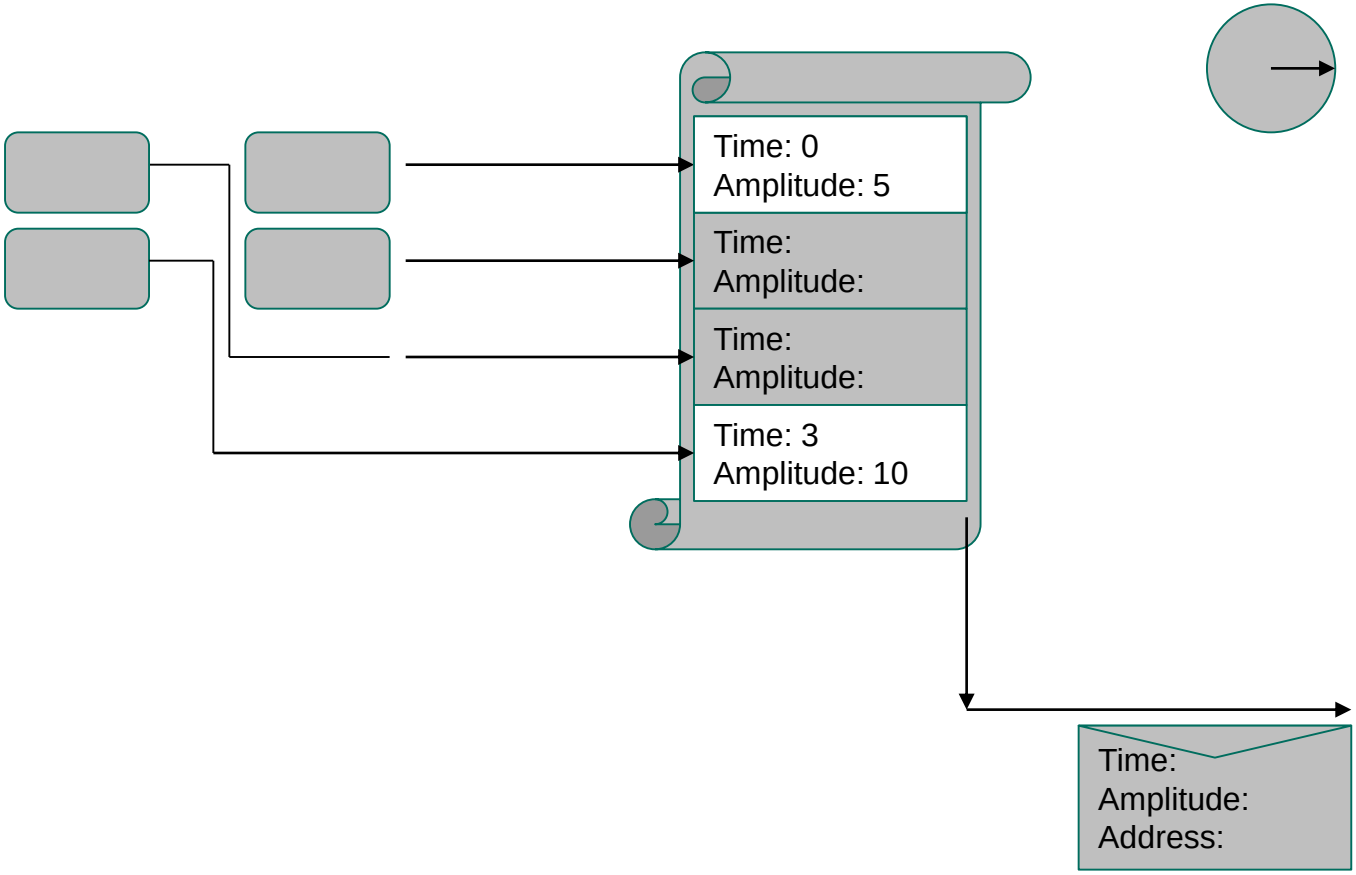
- Hit driven, trigerless, readout



- Hit driven, trigerless, readout



- Hit driven, trigerless, readout



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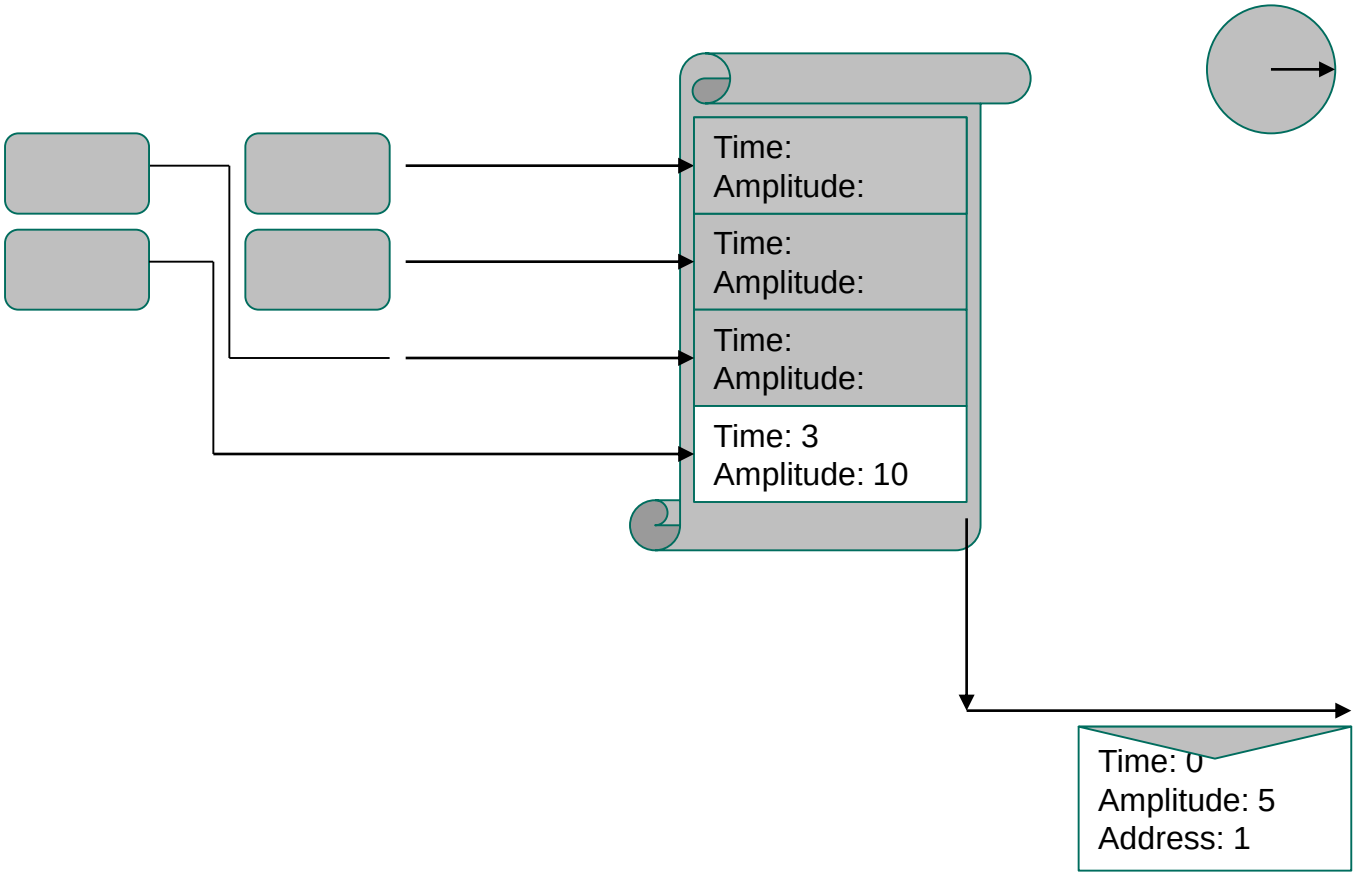

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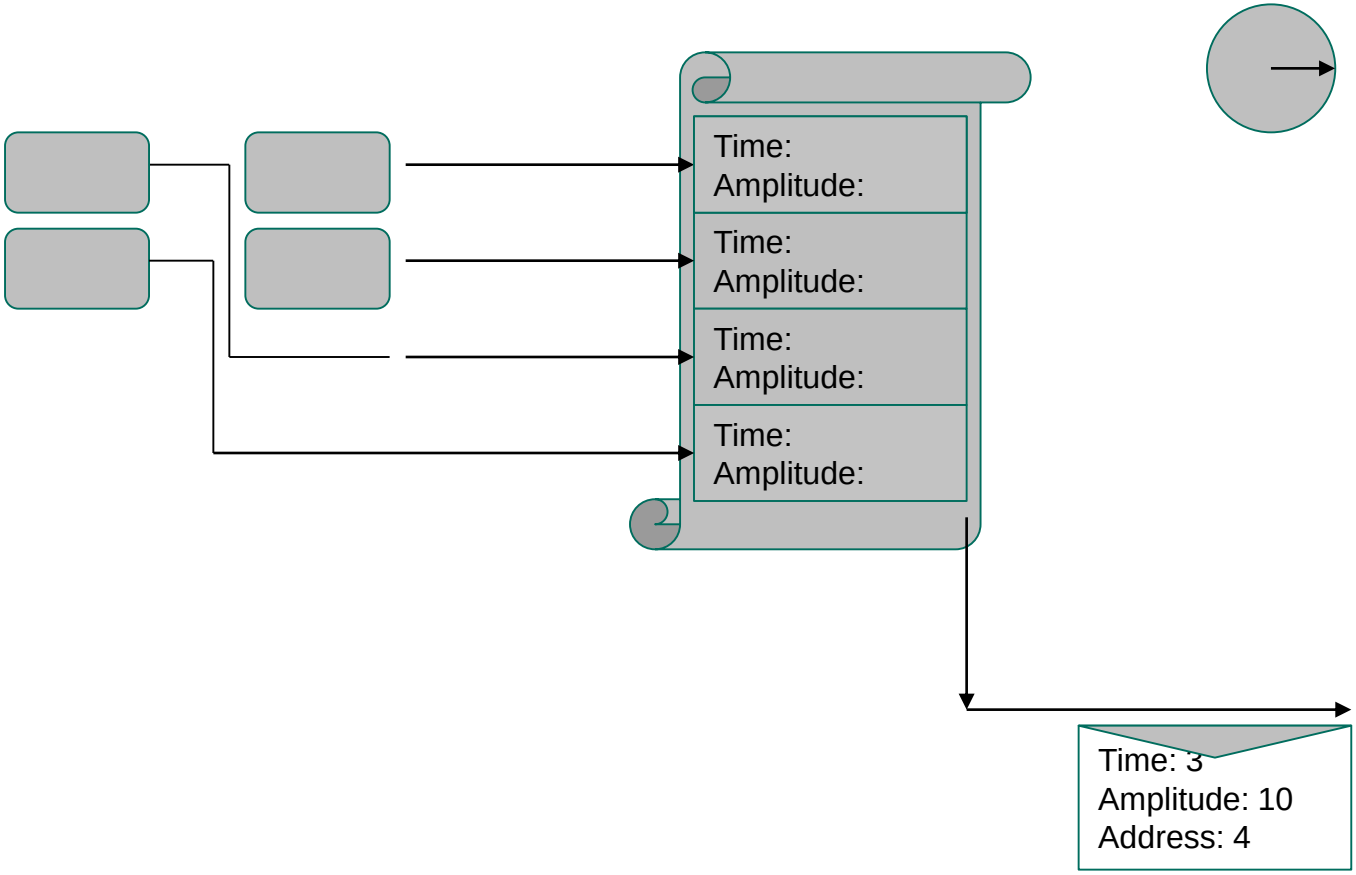
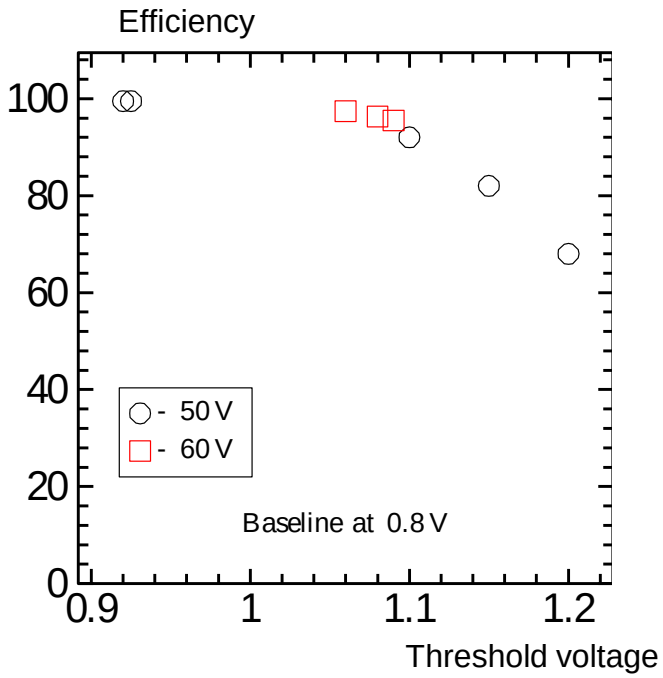
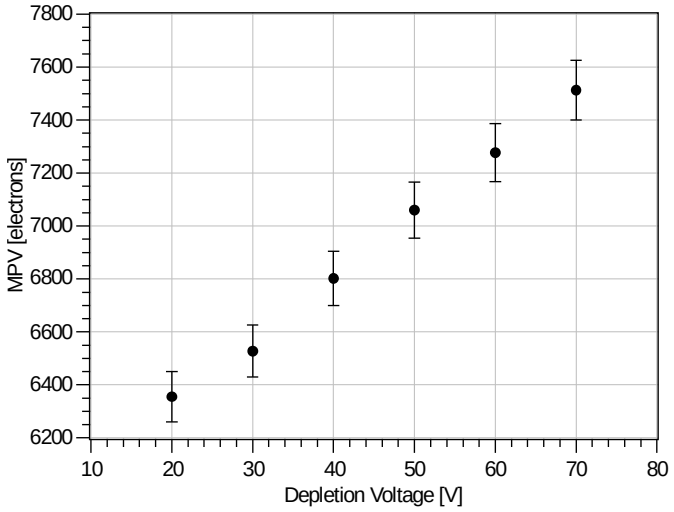


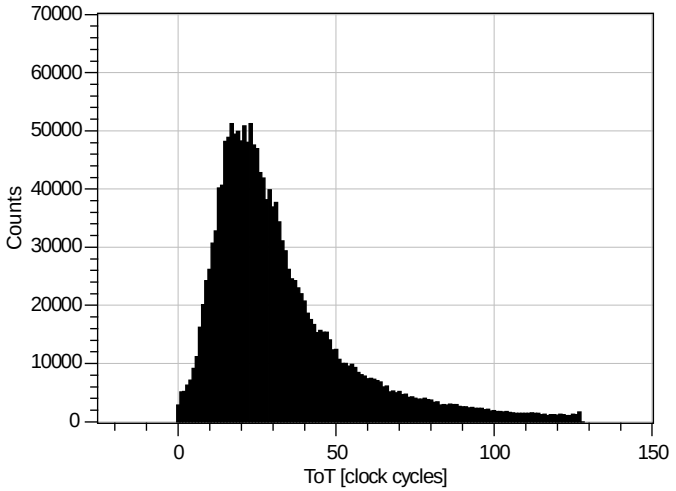
- ATLASPix efficiency measured at CERN SpS – CLIC telescope > 99%
- Spatial resolution: RMS = 12.6µm



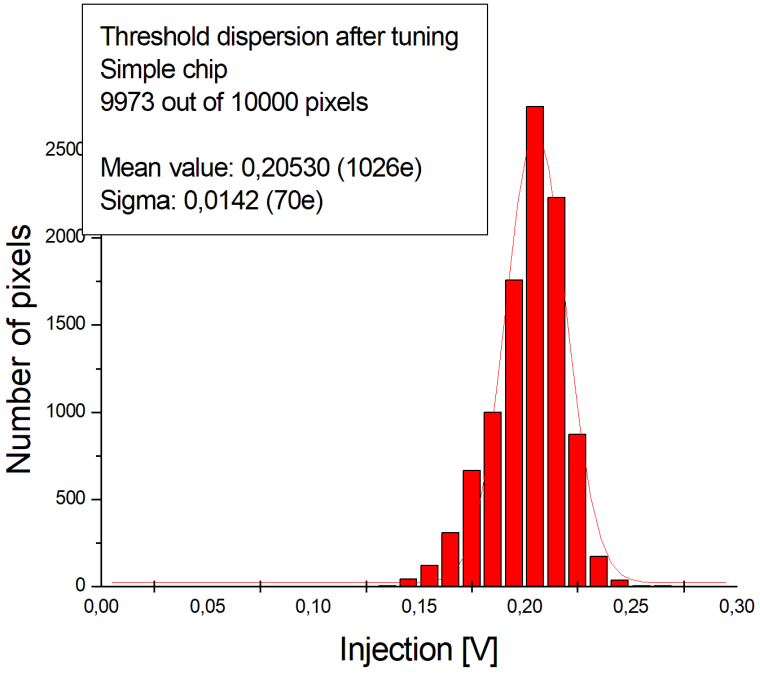
Dominik Dannheim, Andreas Nürnberg

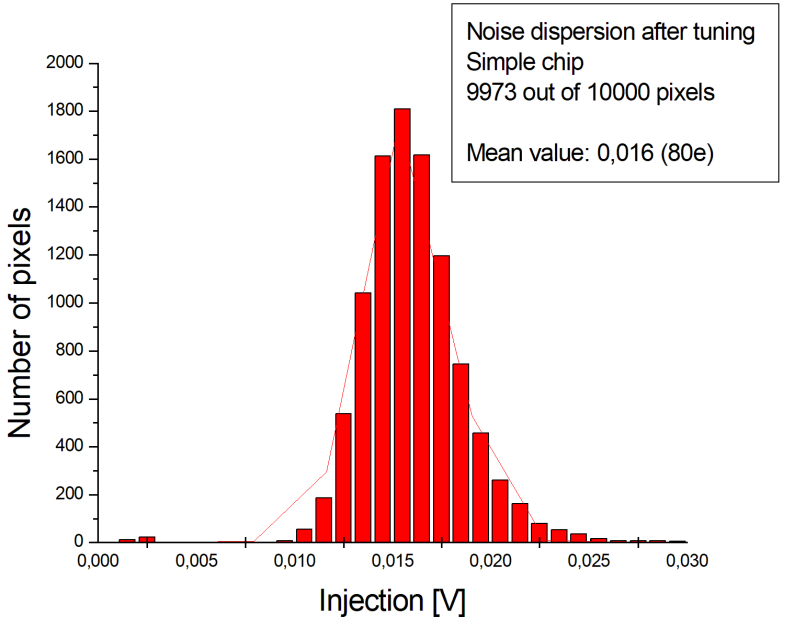
- Figure shows the measurement performed with ATLASPixSimple at 200 Ωcm substrate
- Fast readout has been used, TS period was 25ns (800mbps)
- Sr-90 spectrum has been measured with ToT. (ToT has 6 bits)
- The spectrum peak is 7000e. (Calibrated with x-rays)
- Figure right shows signal (MPW – Sr-90) vs depletion voltage



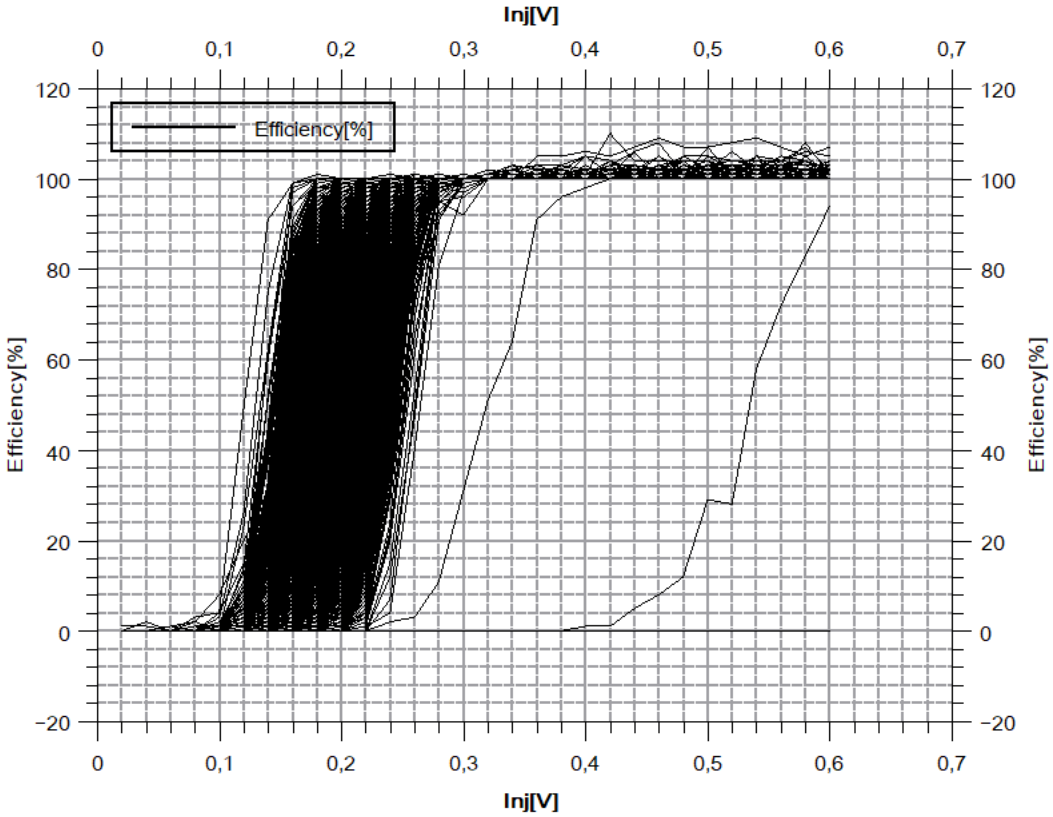


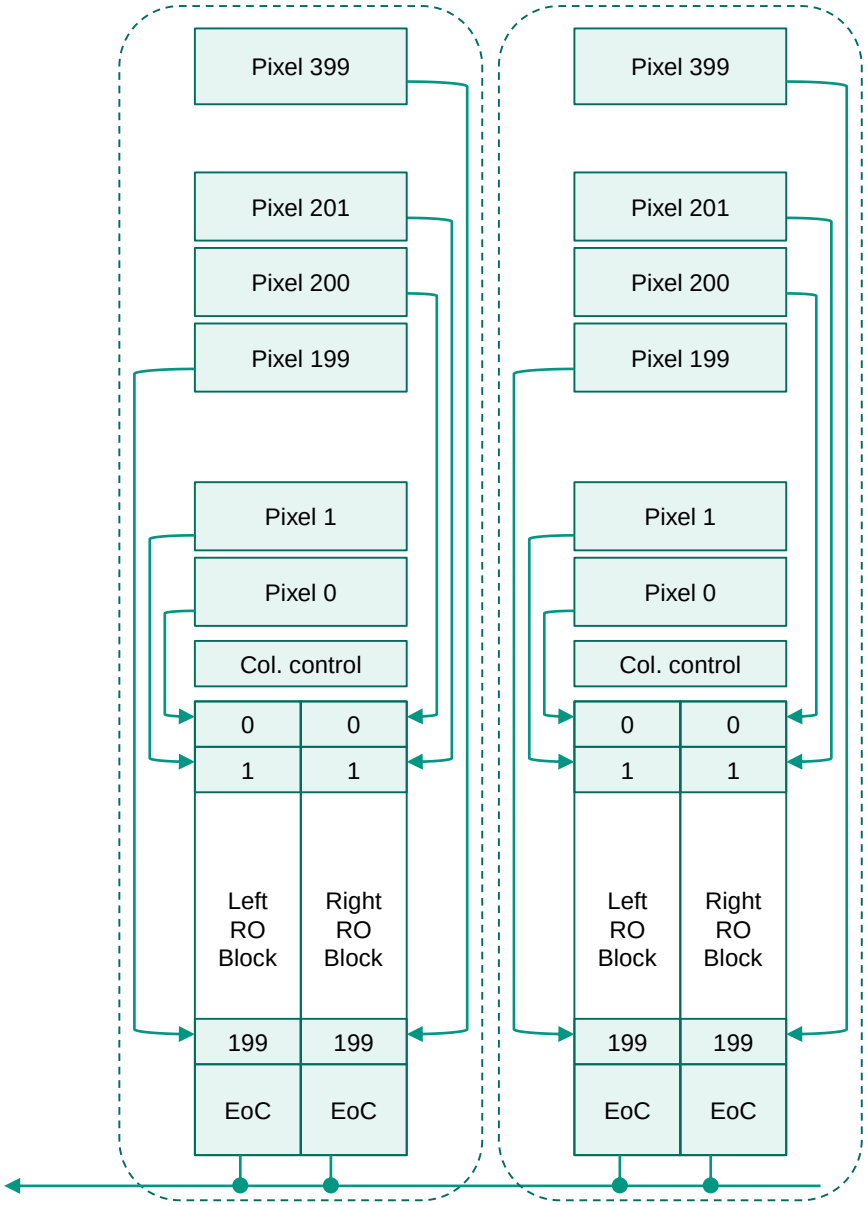
- Result of the threshold scan for ATLASPIxSimple. Matrix has been tuned
- Average threshold is ~1026e and the threshold dispersion 70e.
- The noise dispersion is shown in the figure right. Average noise is 80e.
- Signal to noise ratio of ATLASPIxSimple is about 80. There is enough signal. It would work also at standard substrate

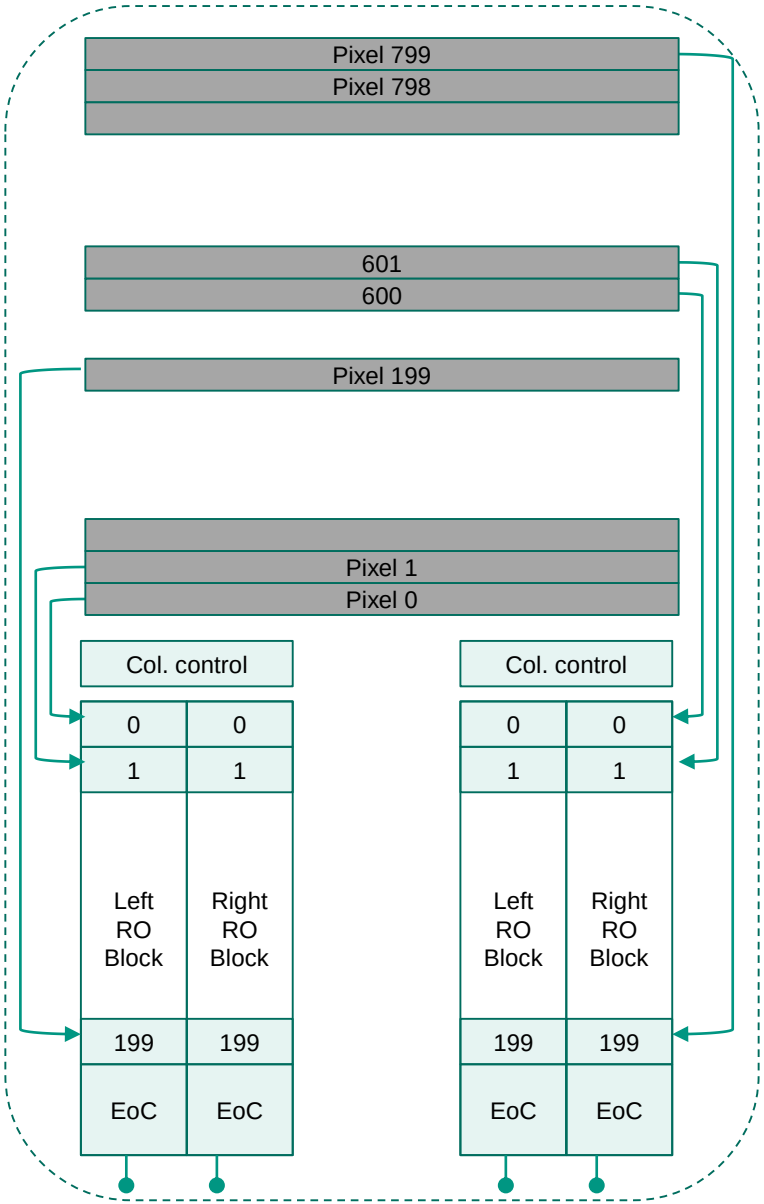




- All s-curves are shown as well. Signals > 0.3V (1700e) can be detected with 99% efficiency

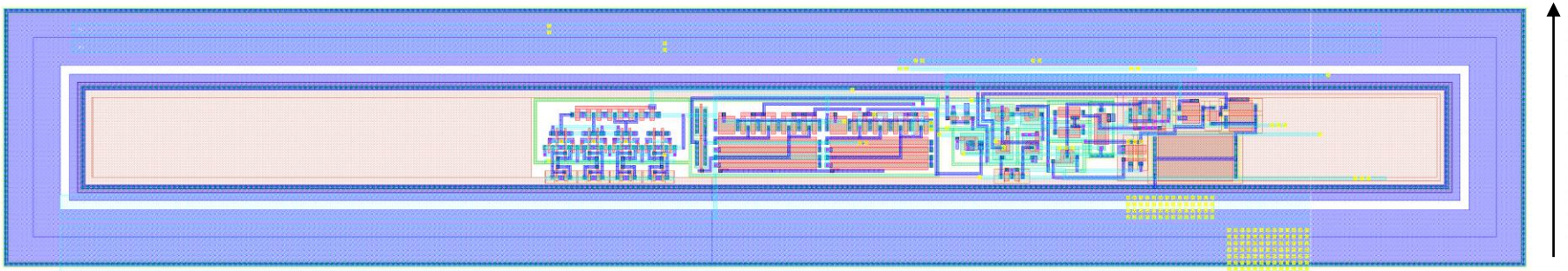



Pixel 399
Pixel 201
Pixel 200
Pixel 199
Pixel 1
Pixel 0
Col. control
0
0
1
1
Left RO Block
Right RO Block
199
199
EoC
EoC
Pixel 399
Pixel 201
Pixel 200
Pixel 199
Pixel 1
Pixel 0
Col. control
0
0
1
1
Left RO Block
Right RO Block
199
199
EoC
EoC


Pixel 799
Pixel 798
601
600
Pixel 199
Pixel 1
Pixel 0
Col. control
Col. control
0
0
1
1
Left RO Block
Right RO Block
199
199
EoC
EoC

Layout of the CLIC pixel

22 – 25µm



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- Produced by AMS in 180nm HVCMOS process
- Submitted as engineering run
- Different substrates: standard, high resistivity
- Features:
- Pixel matrix: 24 x 400 pixels of 40µm x 130µm size
- 6.5 bit time over threshold
- 10 bit time stamp
- Time stamp resolution up to 12.5ns
- 1.6 Gbps data transfer with 8b10b conversion
- Efficiency measured in beam > 99%
- SNR ~ 80
- Power consumption < 200mW/cm^2
- Time resolution: sigma ~ 12ns (pixel to pixel variation corrected, preliminary)
- Spatial resolution: 12.6µm
- Design for CLIC ongoing