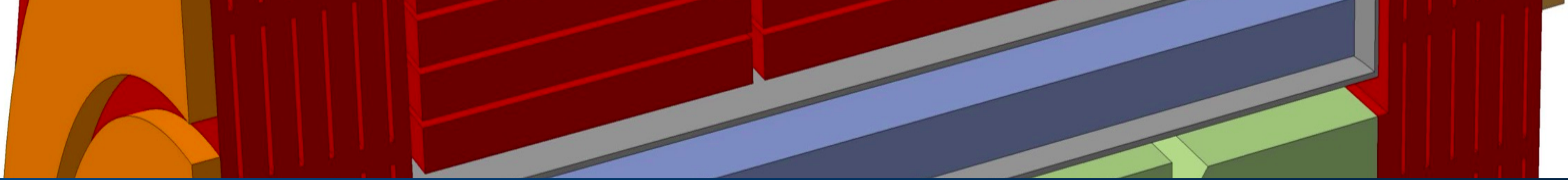
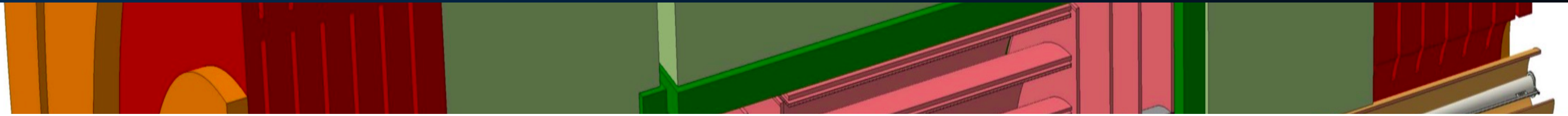


SiW Ecal beam tests in 2017 and 2018

Review and preliminary results

A. Irles, LAL

29th August 2018, CLIC Workshop

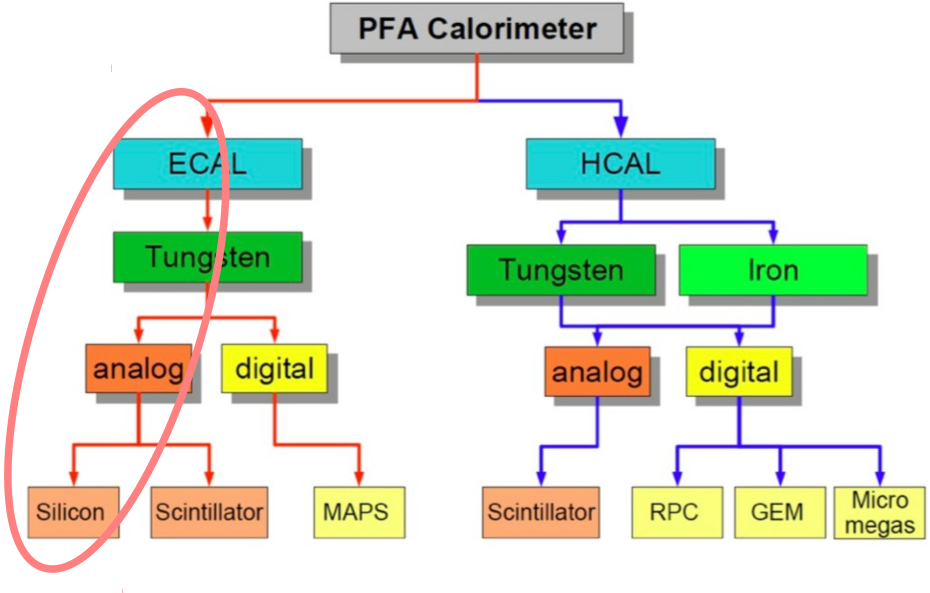


Outline of the talk

- The SiW-ECAL technological prototype

- Beam Test 2017 – DESY TB24
- Beam Test 2018 – DESY TB21 and TB24

- Ongoing activities



Basic requirements of a **PF calorimeter** for future LC

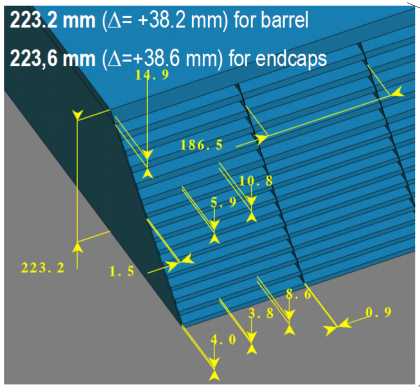
- Extreme high granularity
- Compact and hermetic (inside magnetic coil)

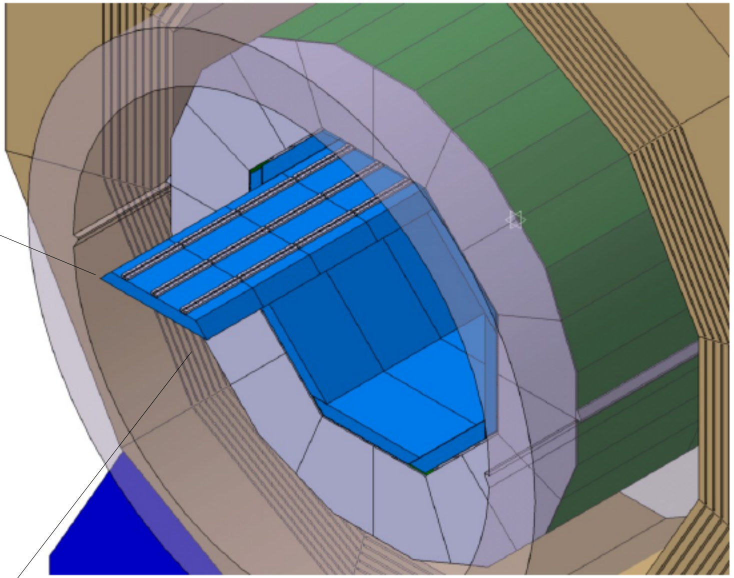
Tungsten as absorber material

- Narrow showers
- Assures compact design
- Low radiation levels forseen at LC
- X_0=3.5 mm, R_M=9mm, I_L=96mm

Silicon as active material

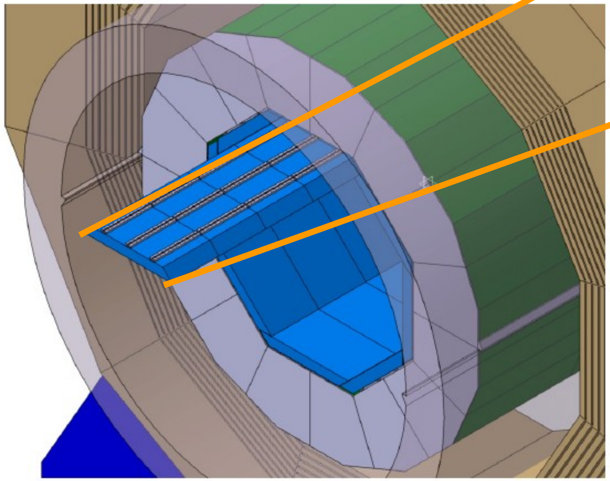
- Support compact designs
- Allows pixelisation
- Robust technology
- Excellent signal/noise ratio



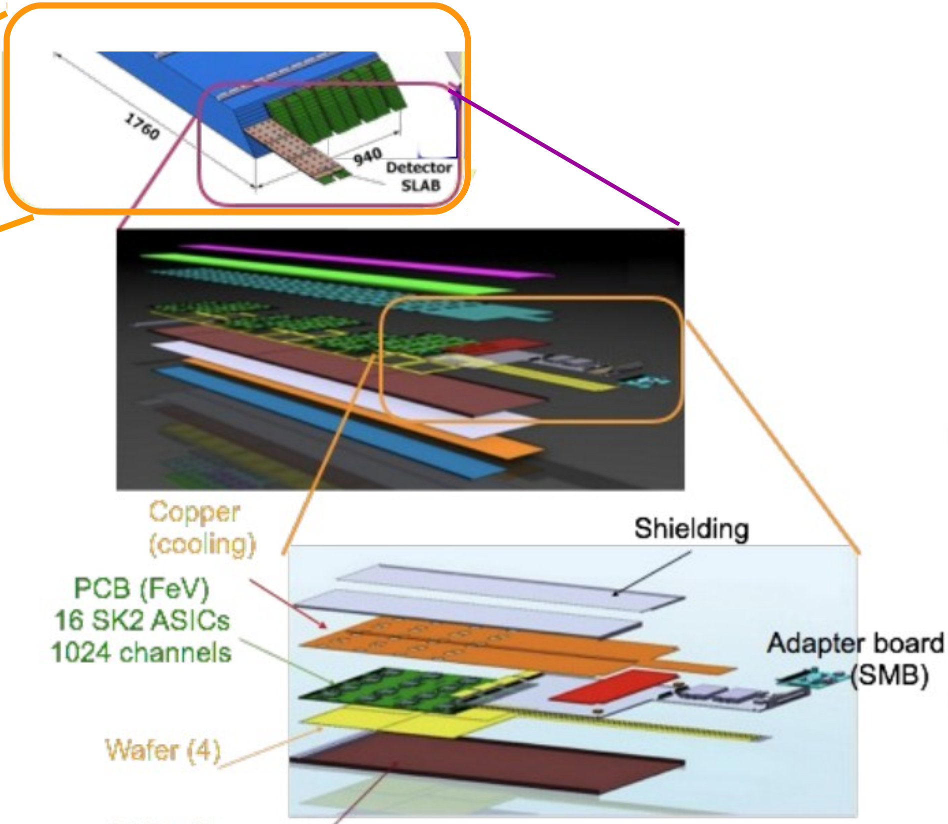


The SiW ECAL in the ILD Detector

The **SiW ECAL R&D** is tailored to meet the specifications for the **ILD** ECAL **baseline** proposal

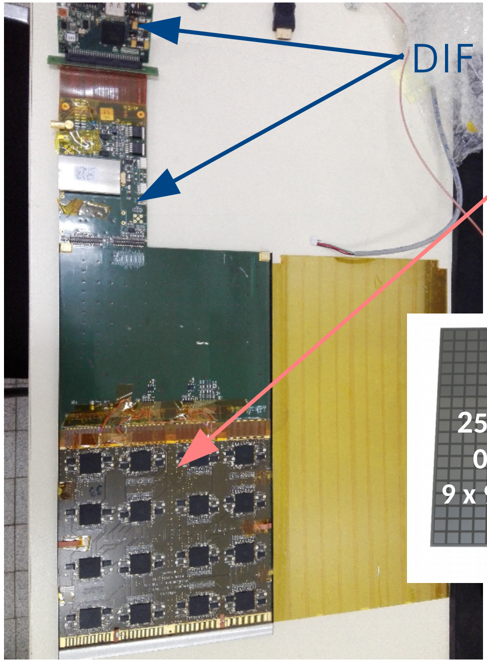


The SiW ECAL in the ILD Detector



U layout of a short slab

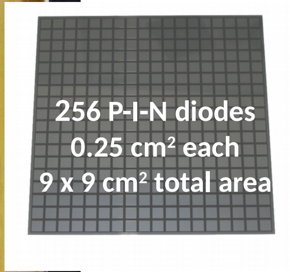
SiW-ECAL technological prototype



DIF + SMB

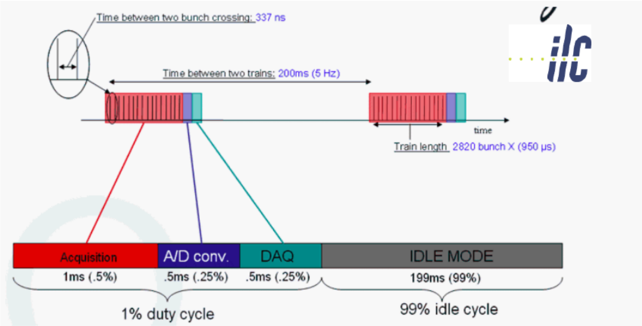
ASU

equipped with 4 Si-wafers



Short slab:

- Adapter board (**SMB**) and Detector Interface (**DIF**)
- **ASU (Active Sensor Unit)**,
  - PCBs (FEV10/11) with silicon P-I-N diodes as active material (325um, 4 kΩcm, N-type)
  - 1024 channels per slab
- VFE electronics: 16 **Skiroc2 ASICS** (in the ASU)
  - Auto trigger, double gain ADC
  - Low power consumption & power pulsing (25µW/ch)
  - 15 memory cells (SCA) per channel

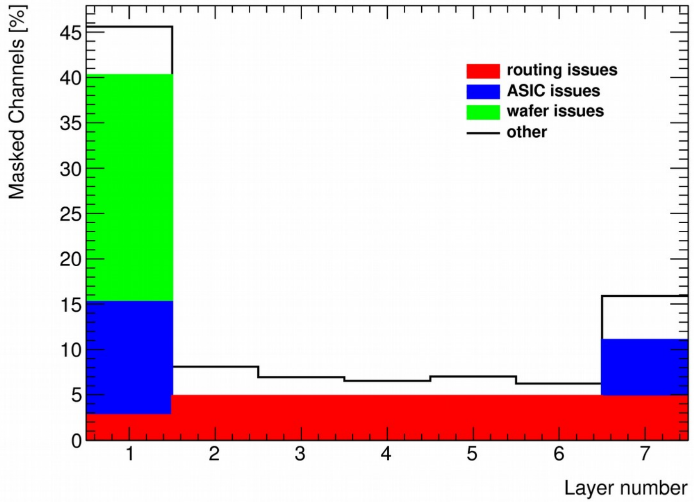


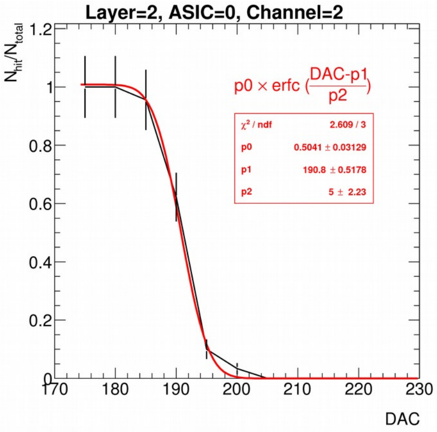
N.B. Final numbers may vary

Commissioning & Passport delivery

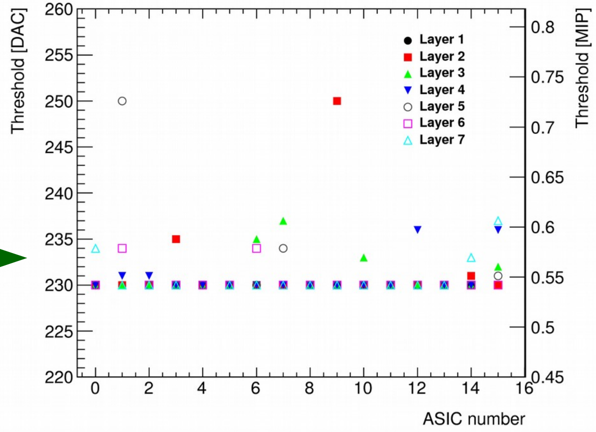
- **Noise control → noisy channels**: **7-8%**: very conservative approach.
  - Found a pattern on the spatial distribution of ~4% some noisy channels

- **Autotrigger** optimization
  - Threshold scans made for all channels → one optimal threshold found for each ASIC





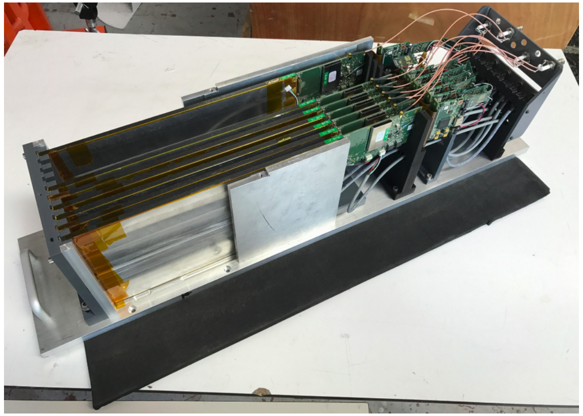
Threshold scan curves with noise

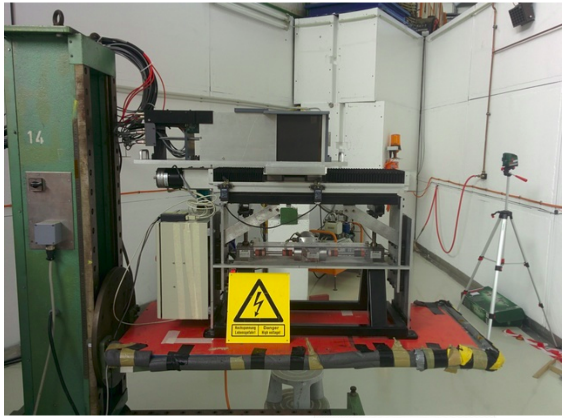


Auto trigger threshold set at ~0.5 MIP

DESY@2017 – Setup & program

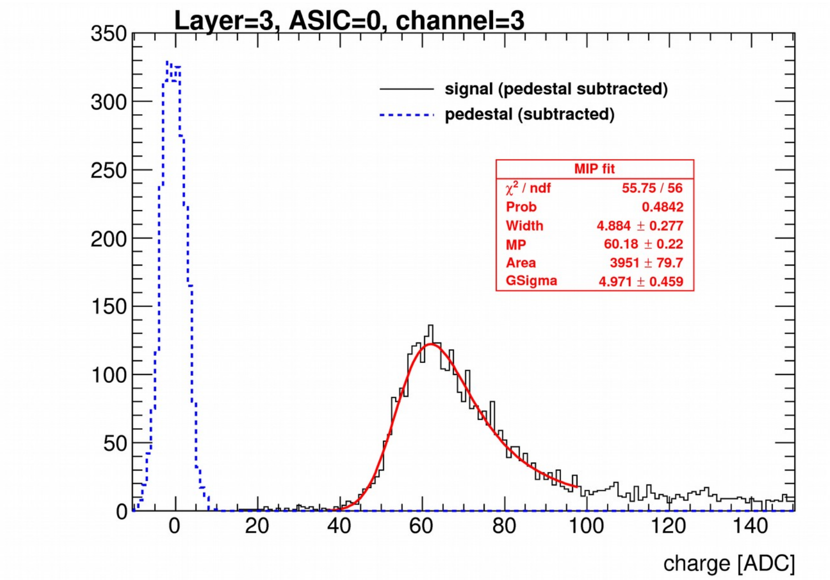
- **Setup** :
  - 6 FEV11, 1 FeV10 each equipped with 4 325um Si wafers and 16 Skiroc2
  - Power pulsing and ILC mode (emulated ILC spill conditions)
- **Physics program:**
  - Calibration run with 3 GeV positrons perpendicular beam without tungsten absorber plates
  - Electromagnetic showers program.
  - Calibration run with 3 GeV positrons in ~45 degrees (6 slabs)
  - Magnetic field tests with 1 slab (up to 1 T)

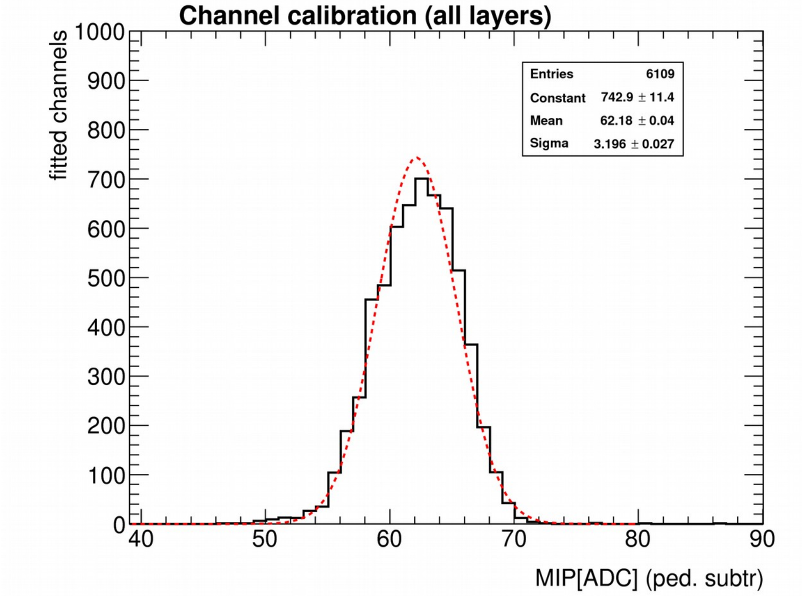




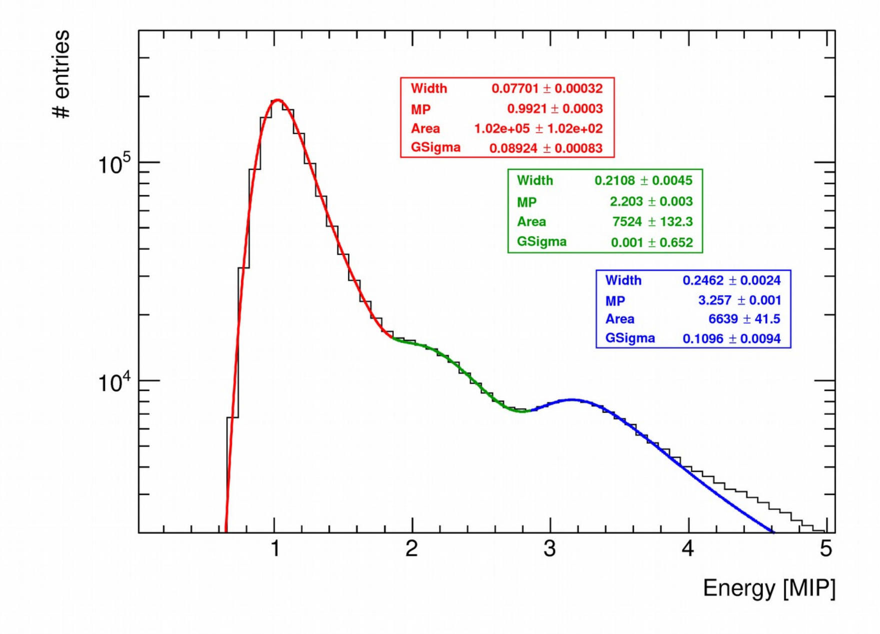
DESY@2017 – MIP calibration

- MIP scan: Si - ECAL **(w/o the W)**
  - Positrons of 3 GeV (~2 kHz rate, beam spot with slightly irregular shape and size <2cm diameter)
  - Simple analysis done module by module
  - Pedestal correction done chip/channel/sca wise, Energy calibration done chip/channel wise
  - MIP: We fit the 98% of available channels → MPV = 62.2 ADC, sigma= 3.2 ADC (dispersion of 5.1 %)

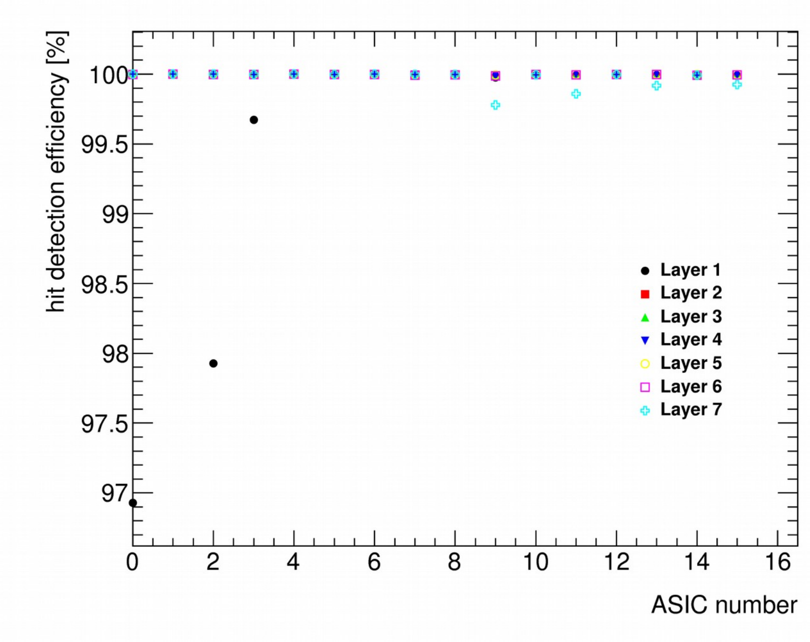




- After calibration we performed the track reconstruction.



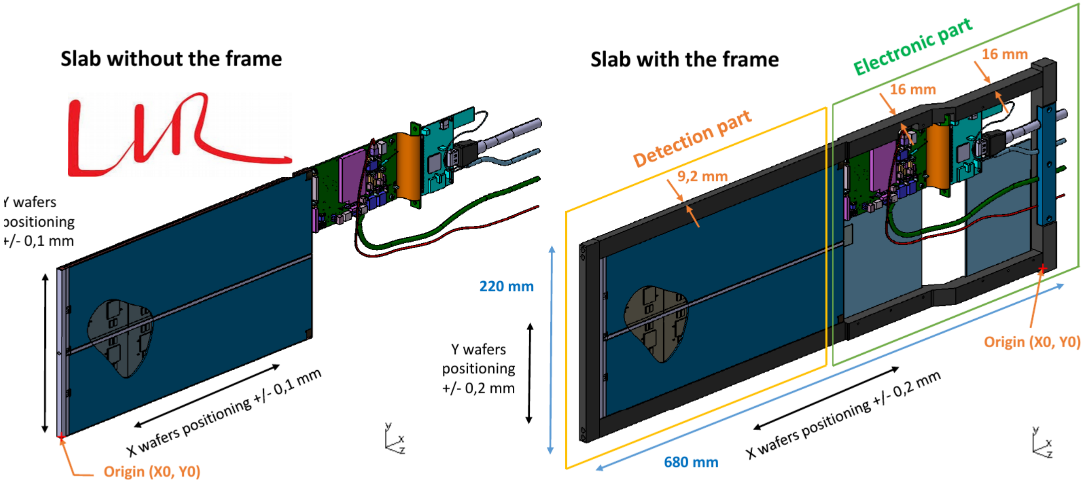
Hit energy distribution in tracks for all calibrated cells



Hit detection efficiency for tracks

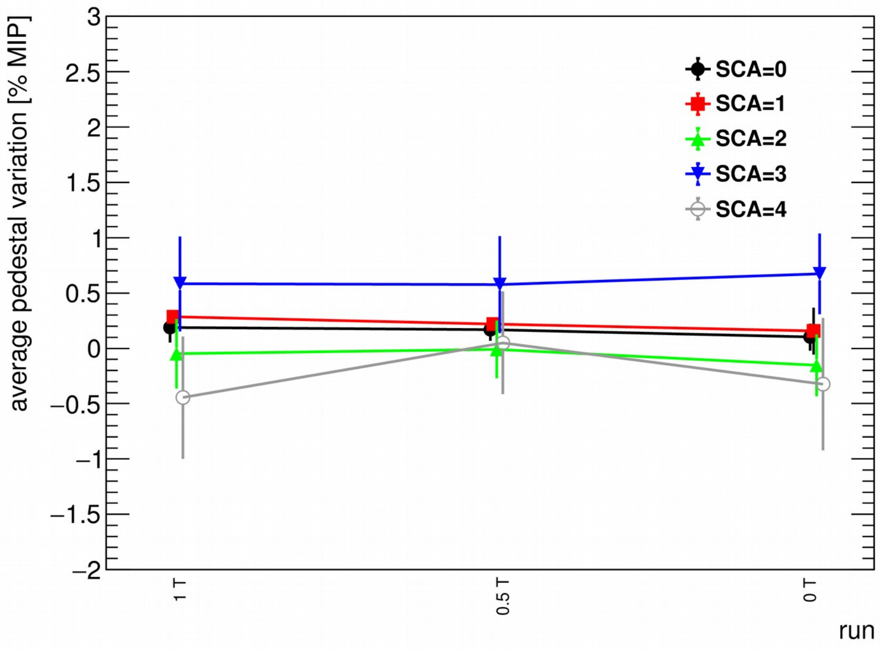
DESY@2017 – Tests under Magnetic Fields

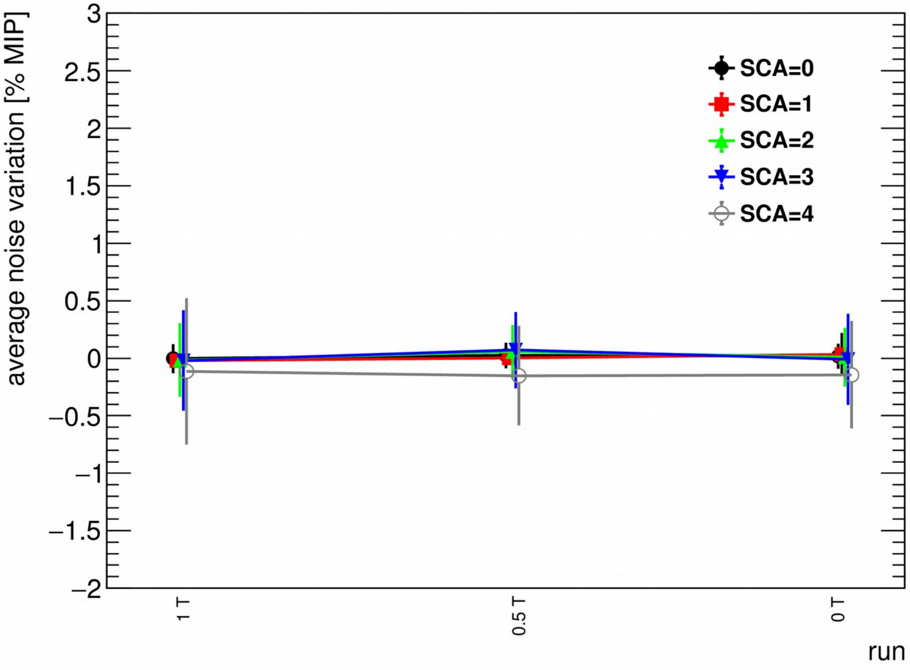
- Magnetic field tests
  - One slab in a special plastic support
  - Magnetic field from 0 to 1 T.
  - With and without beam.
- No failure/loss of performance observed during the operation and after the first analysis.
  - ~20 hours of data in total.



DESY@2017 – Tests under Magnetic Fields

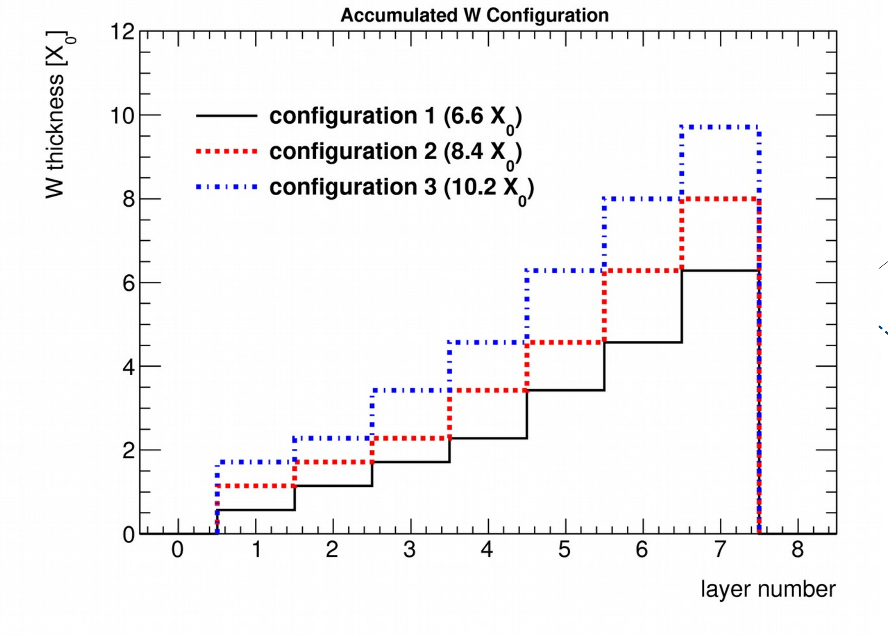
- Very stable noise conditions





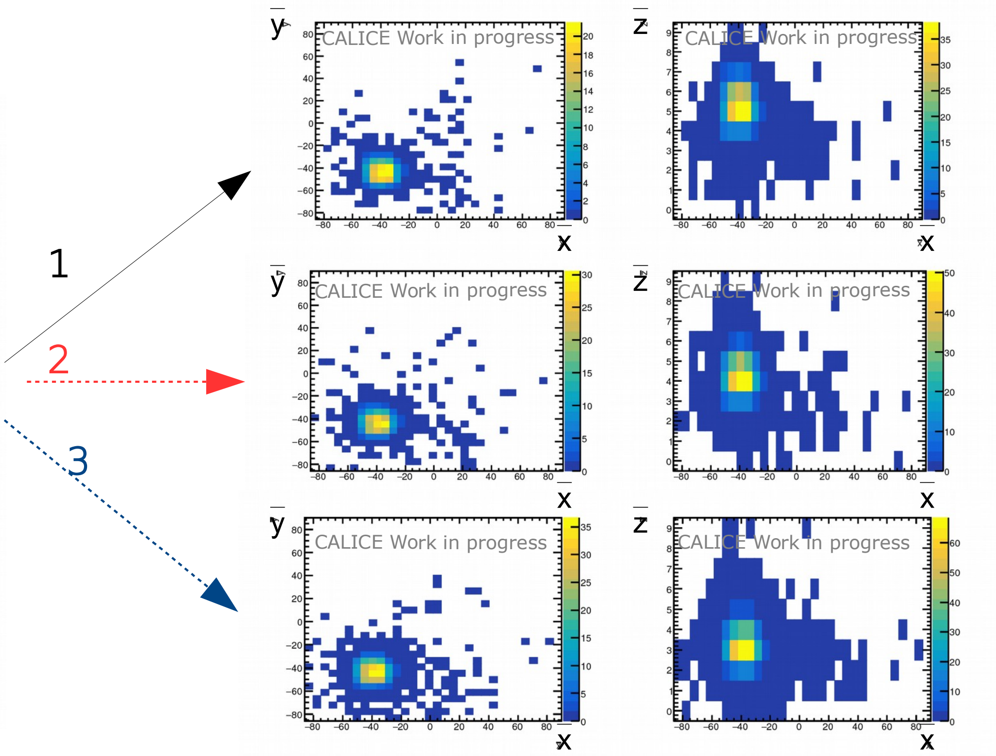
Tungsten program

- Scans of various energies (from 1-5.8 GeV).
- Scan using different tungsten configurations



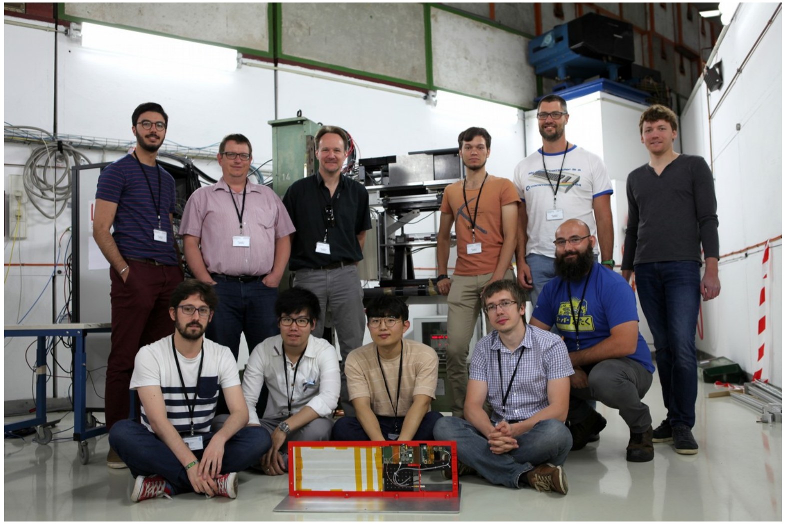
Raw shower barycenter maps

$$\bar{x} = \frac{\sum_{i=cells,\, j=layer\ number} x^i w_0^j E_i}{\sum_{i=cells,\, j=layer\ number} w_0^j E_i}$$



DESY@2017 – Summary

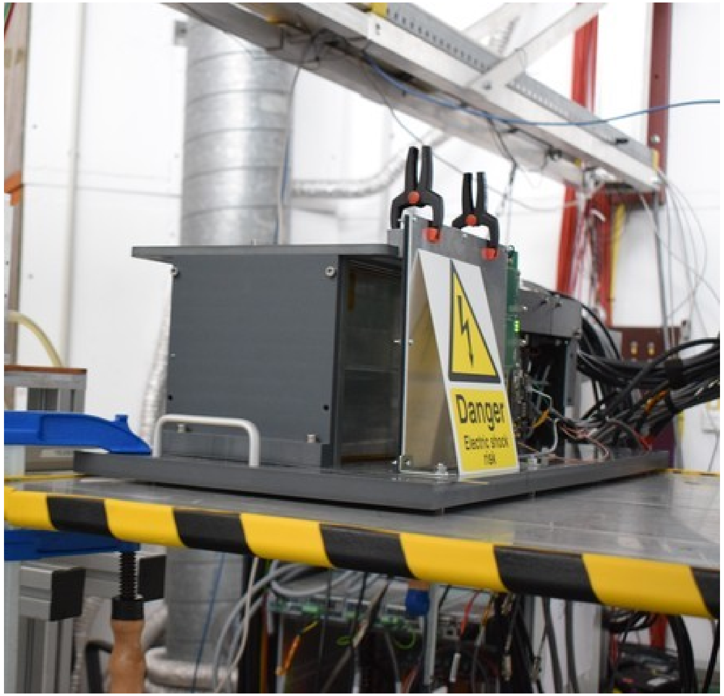
- Successful beam test of the SiW-ECAL technological prototype.
  - first time with fully assembled detectors elements (first 7 of 10000 needed for ILD)
- MIP calibration achieved at the **5% level.**
- First looks at **shower response are very promising**
- **Operating in 1T magnetic field**
  - Also nice and consistent calibration results

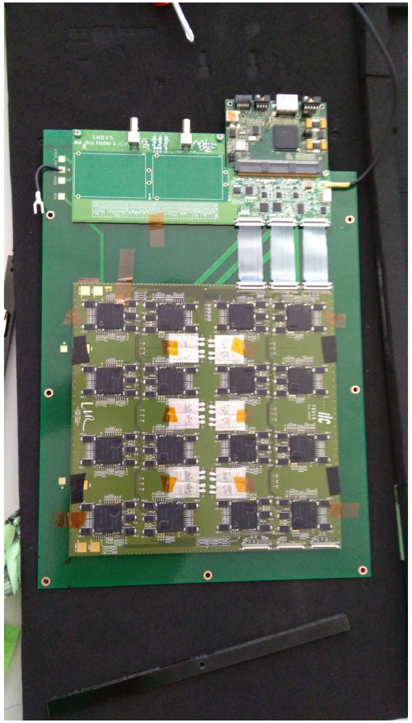


- Presentations + proceedings for **CHEF2017, IEEE2017, LCWS2017**
- Writing of a technical paper is ongoing.

- Excellent prospects for next beam tests !! → DESY@2018

- **Technical beam test with the goals of:**
  - Testing an electrical prototype of a long slabs (next slides)
  - Crosscheck 2017's results → same modules and same commissioning files
  - Tests of a new ASU prototytpe FEV13





FEV13&SMBv5: **LLR & Kyushu university** collaboration

- With the **aim of noise level improvement** by separating PCB layers for the analogue and digital power of the ASIC
- 4x750 µm wafers (instead of 320)

- VFE: SK2a instead of SK2
  - allows for fine tunning of thresholds + brings the possibility to use the TDC
- Data is being studied.

DESY@2018 – Electrical prototype of Long Slab

Goals

- Validating the electrical behavior of a long slab (clocks, data integrity, noise level on length)
- Readout time and electrical consumption studies

The prototype:

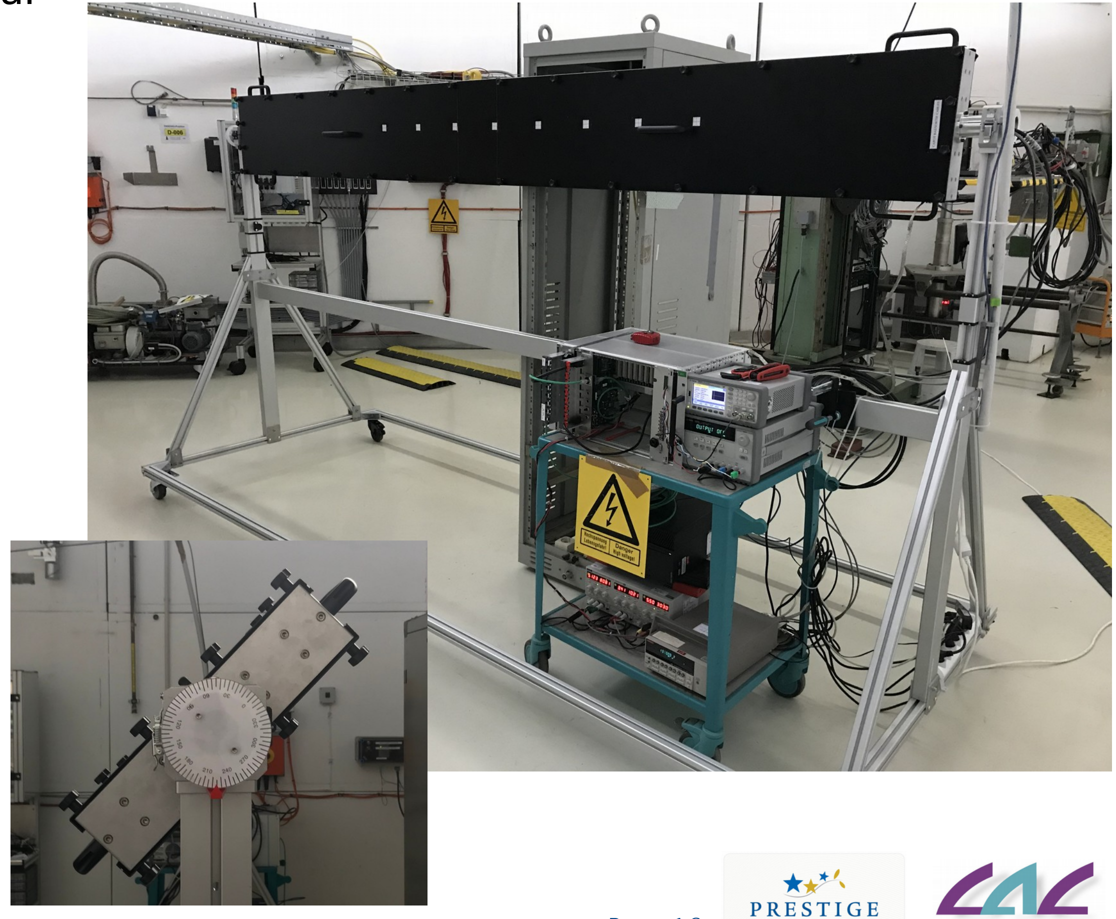
- Daisy chain of 8 ASU (extendable to 12)
- Corresponding to typical barrel length
- Based on FEV12 ASU & SMBv4 (in stock)
- No ILC geometrical constraint (thickness)
- Baby-wafer 4x4 pixels on each ASU

It needed some adaptations:

- HV filtered by RC circuits to reduce noise
- Of the impedance of lines (done afte simulations)

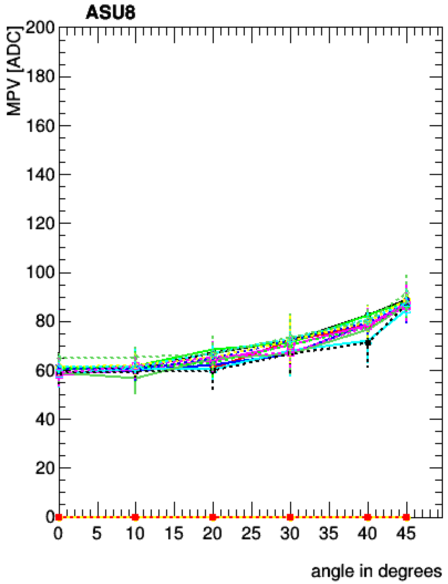
DESY@2018 – Long Slab Setup

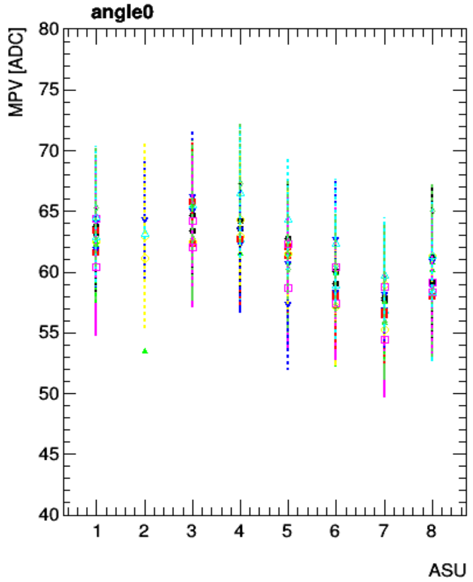
- Mechanical structure with mono-directionnal wheels for precise positionning
- Full rotation system with index
- Black cover for light isolation
- Laser alignment with silicon pads
- Compact DAQ on a wheel table
- 3224mm long
- 8 target accessible in zone 21, only 7 in zone 24

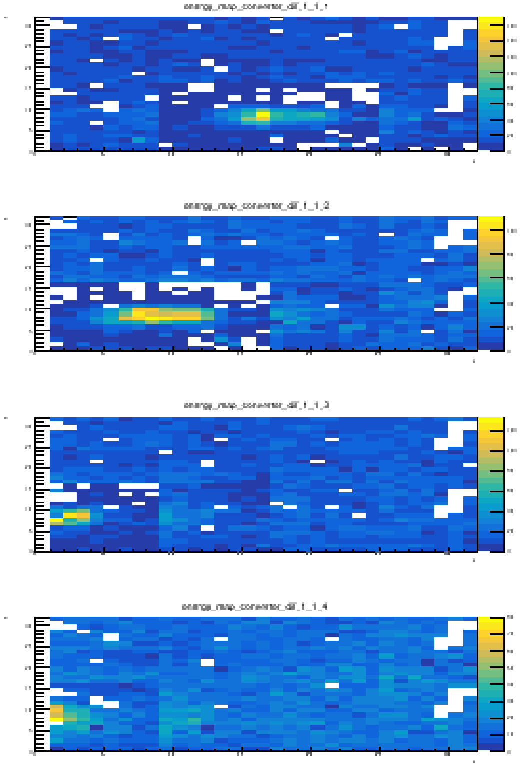


DESY@2018 – long slabs program

- Single cell calibration using 3GeV electrons and orienting the long slab at different angles
  - Calibrate the 8 ASUs
  - With short slabs as reference (running with independent DAQs)
- Long slabs response to showers
  - 5X0 of lead in front of one ASU







Preliminary results: E. Mestre & V. Lohezic

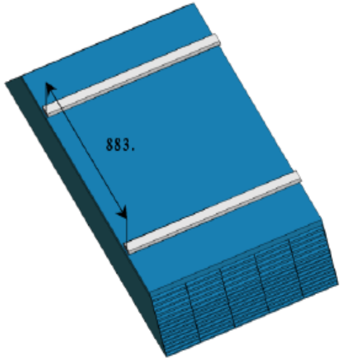
Summary and outlook

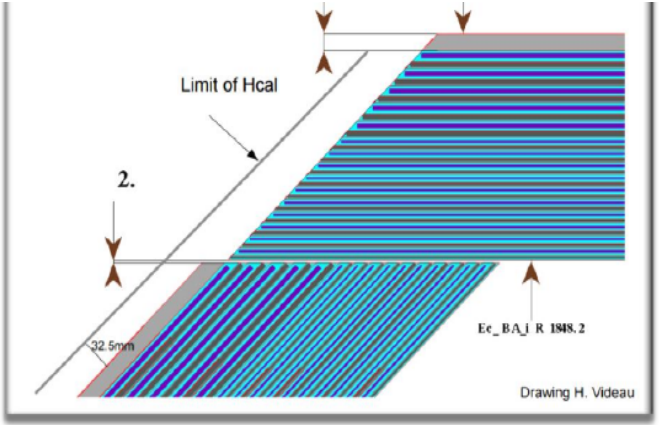
- Successful **construction** and **operation** in beam of the **SiW-ECAL** technological prototype made of **short slabs**…. And a **electrical long slab** (with very good performance)
- Still some work to be done towards realistic ILD prototype. Many challenges being faced at the moment:
  - Long slab: from a electrical prototype to a realistic prototype
  - Compactification of DAQ and active units.
  - Studies for ILD integration.
- Combined beam test with the SDHCAL at CERN in 2018
  - From the 26th September to the 3rd October

Back-up

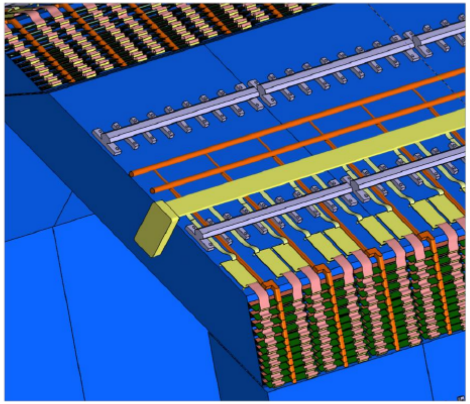
Towards a real detector: challenges

- **Long slabs** : up to ~15 ASU (~3m)
  - Complex object: mechanics and electronics
- **Spatial constraints**:
  - limited space between layers and between ECAL and AHCAL
  - Control & Readout electronics at the extremity of the Slab
  - Signal Integrity over the Slab
- Low power consumption.
- Thermal uniformity
- Mechanical Assembly process





E-CAL Services

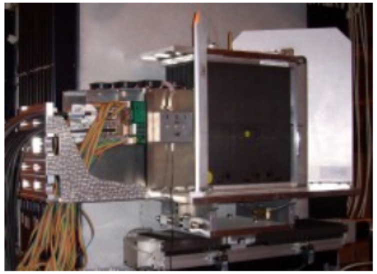


Calorimetry for the International Linear Collider (ILC)

Physics Prototype

Proof of principle

2003 - 2011



Number of channels : 9720

Pixel size: 1x1 cm2

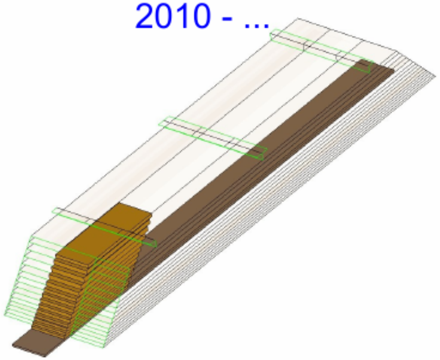
$R_{M,eff}$: ~ 1.5cm

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

2010 - ...



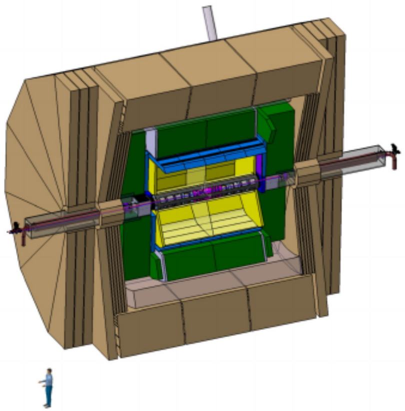
Number of channels : 45360

Pixel size: 0.55x0.55 cm2

$R_{M,eff}$: ~ 1.5cm

Weight : ~ 700 Kg

LC detector



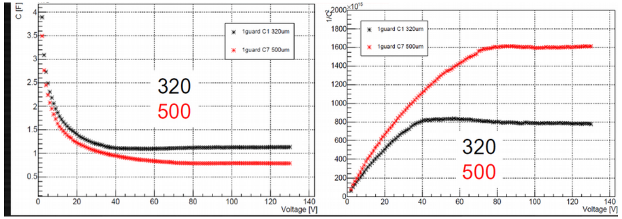
ECAL :

Channels : ~100 10^6

Total Weight : ~130 t

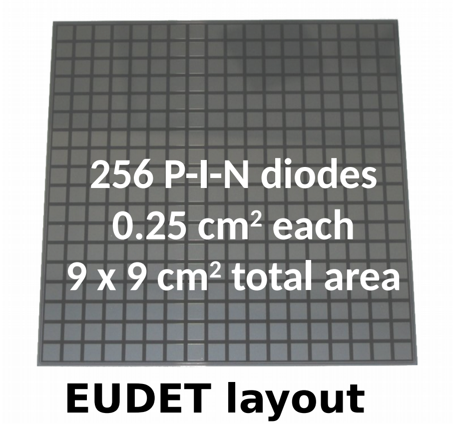
Si wafers

Designed for ILC : **Low cost, 3000 m2**
Minimized number of manufacturing steps
Target is 2.5 EUR/cm2
Now : 10 EUR/cm2 (Japan)



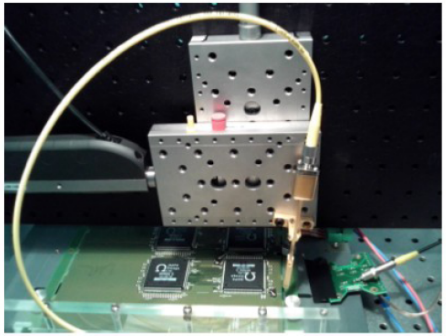
I(V) and C(V) characterization

Breakdown voltage >500V
Current leakage <4 nA/pixel (chip is DC coupled)
Full depletion at <100 V
(~40 V with 320 um, ~70 V with 500um)
Null C(V) slope to avoid dC/dV noise



EUDET layout
Prototype from Hamamatsu

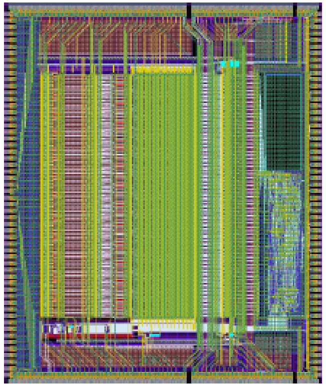
Wafers are glued to PCB (robot, LPNHE)
Segmented guard-rings layout as an option

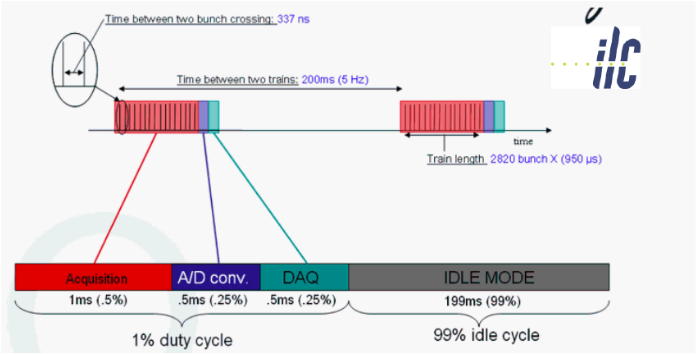


R&D on crosstalk
Segmented guard-rings layout as an option. Systematics studies with laser systems and simulation.

Front end electronics and DAQ

- SKIROC (Silicon Kalorimeter Integrated Read Out Chip)
  - SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
  - High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
  - Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)
  - Auto-trigger at 0.1-0.5 MIP
  - Low Power: (25µW/ch) power pulsing
    switch off electronics bias currents
    during bunch trains

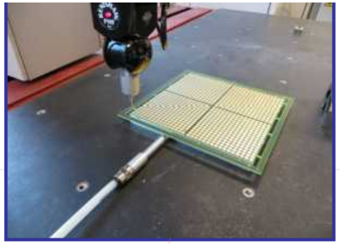


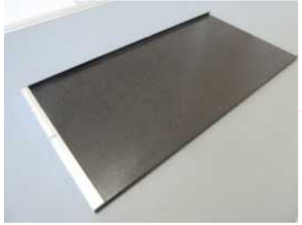


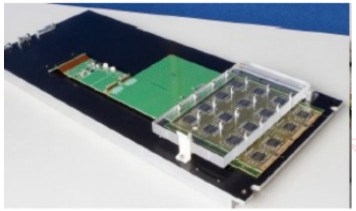
N.B. Final numbers may vary

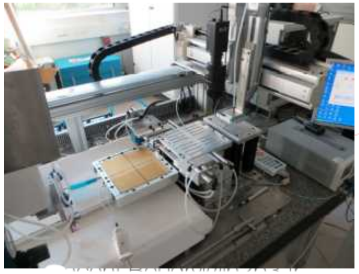
- Prototype version (Skiroc 2 and 2a) for R&D and beam tests
- Definitive version will be optimized for ILC and work in zero supression conditions.

Assembly chain

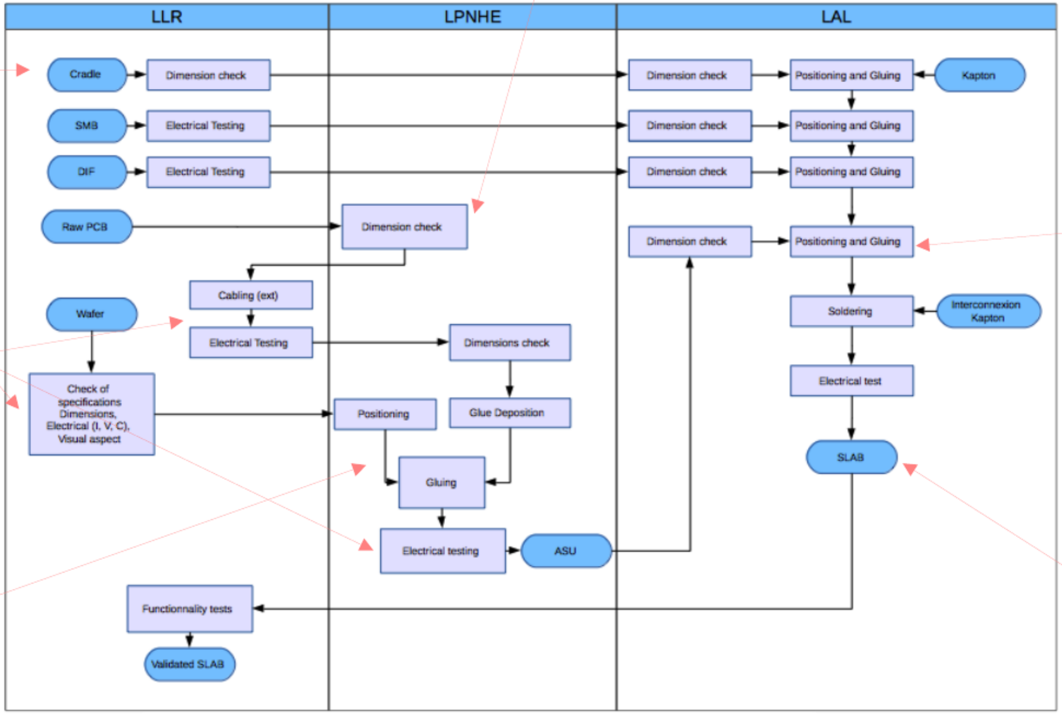


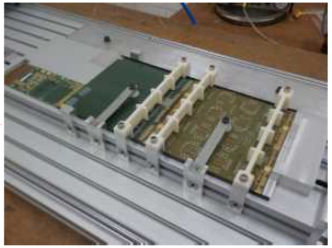






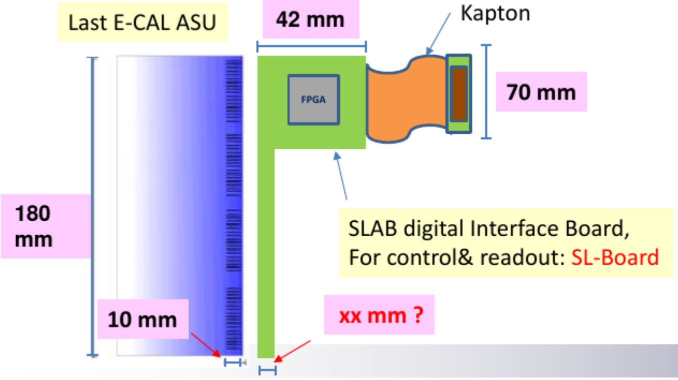
'Simplified view'

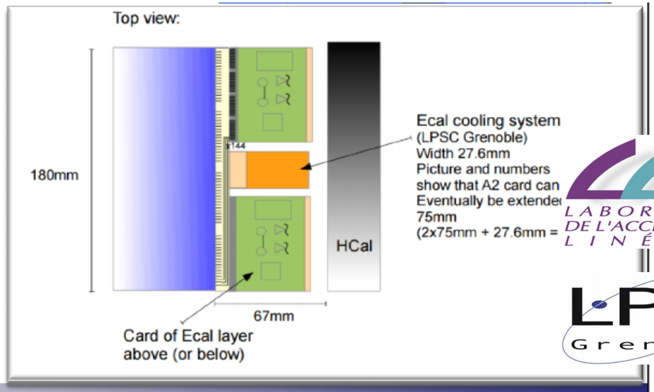




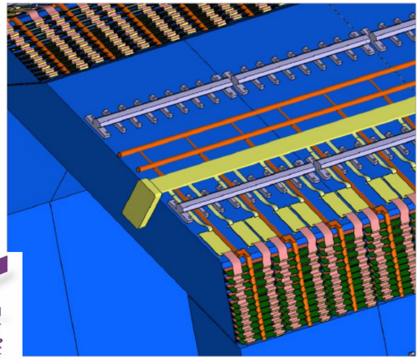
Compactifying the DAQ and passive components of the ASU

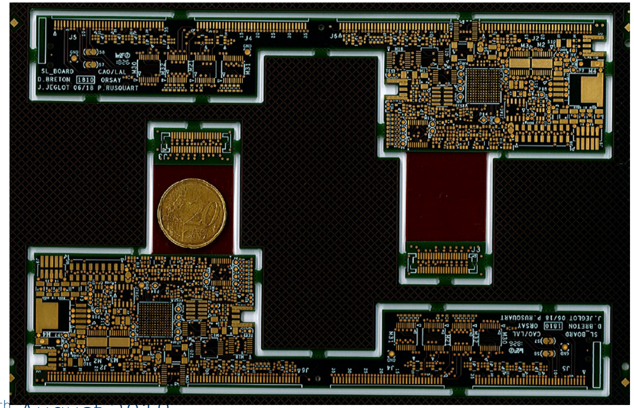
- Space constraints for the Slab Interface Board (SL-Board):
  - Power and signal cables and read-out electronics

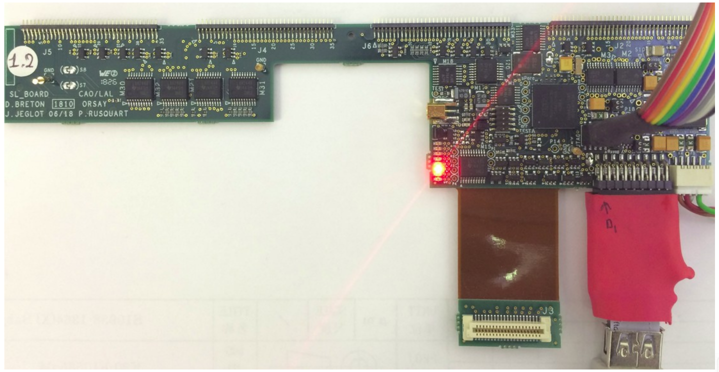




E-CAL Services

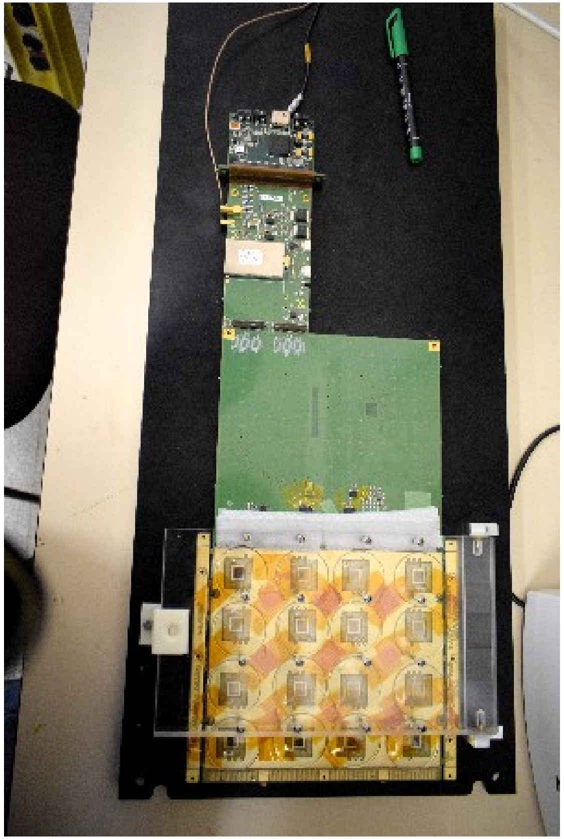


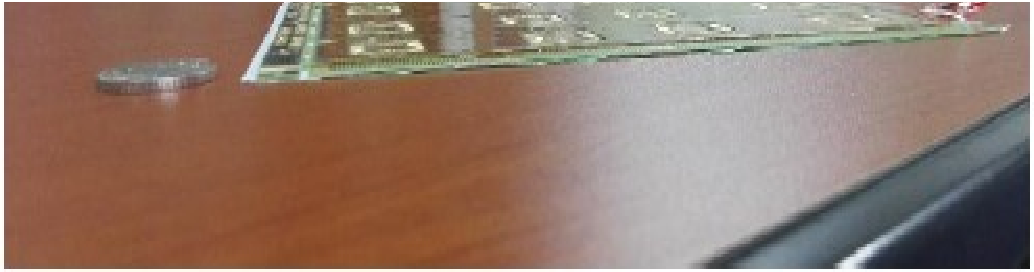




Compactifying the passive components of the ASU

- Investigating **ultra thin PCB**, with chip on board **COB**
  - Semidonductor packaging, wire bonded.
- LAL/OMEGA collaboration with Corean Group of SKKU, EOS company for the PCB and Kale company for the wire bonding)
  - Strong synergies between university and local companies
  - Testbenchs at LAL and SKKU, training of students done at LAL.
- FEV11_COB production ready (**10 boards of 1.1mm,** good planarity and good electrical response). **3 sent to LAL**
  - Baby Wafer gluing + tests ongoing





Compactifying the passive components of the ASU

- New interconnection proposal for the ASU with the SKIROC-BGA option
  - old approach based in flat kapton cables seems not feasible at production scales (see back-up slides)
- Gradconn connector BB02-YN
  https://www.gradconn.com/Products/BoardToBoard/MatingHalves/BB02-YN/BB02-WF
  - 35 pins, Height : 1,5 mm possibly 1,27 mm.
  - Pitch 1mm compatible with existing ASUs
  - Current rating : 1 A., AC 300 Volts

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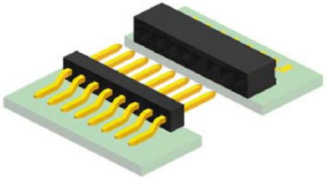
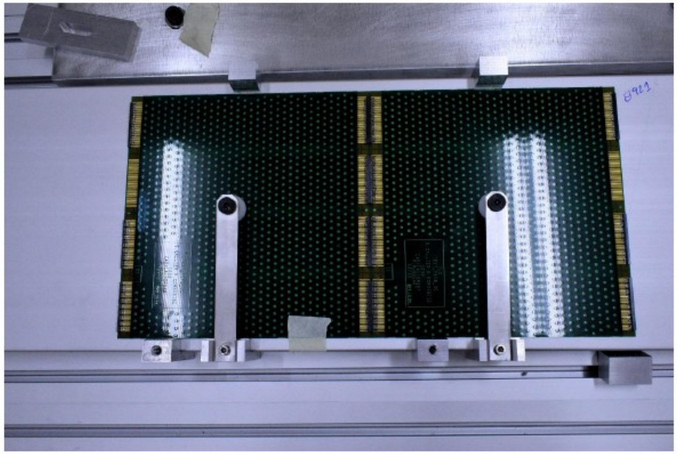
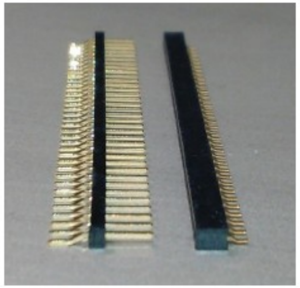
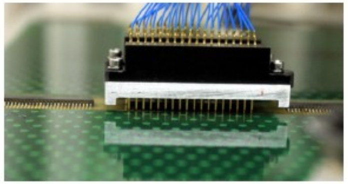
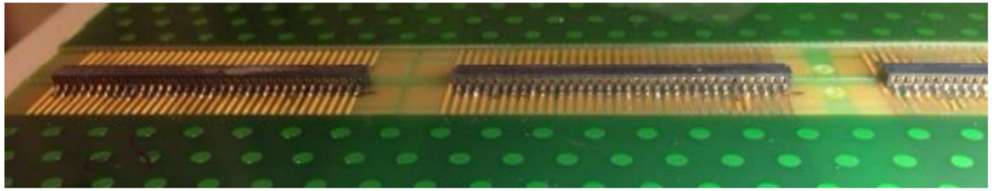






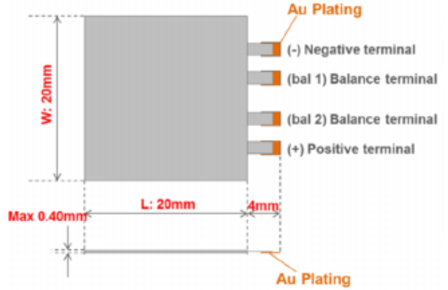


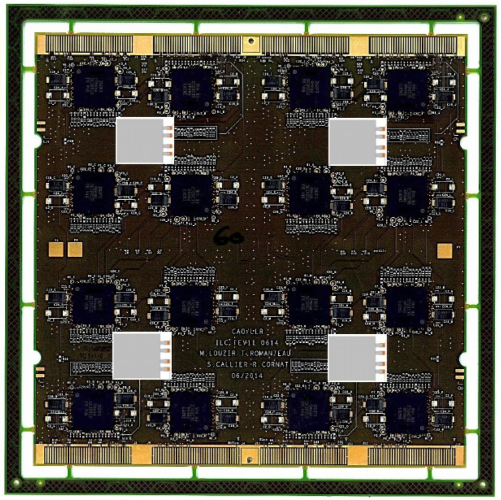


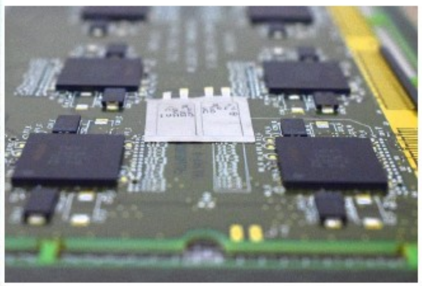
Compactifying the passive components of the ASU

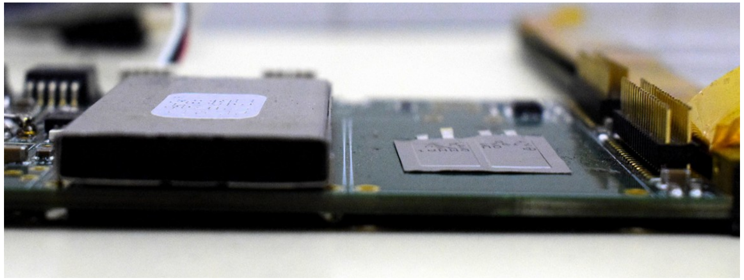
- Proposal to use new ultra-flat capacitors to distribute over the ASUs. This will permit:
  - Peak current reduction: especially through the connectors
  - No more voltage drop along the slab
  - Homogeneous peak power dissipation during power pulsing.
- We go from the 400 mF capacitor/ 12A (peak Current) for the whole SLAB to 140 mF / 1.2 A per ASU.

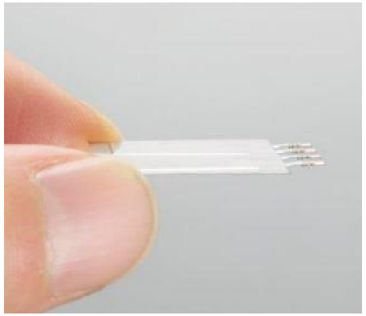
Brand new product, appeared few months ago











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