Studies on the SALT ASIC, a novel front end electronics for the LHCb Upgrade

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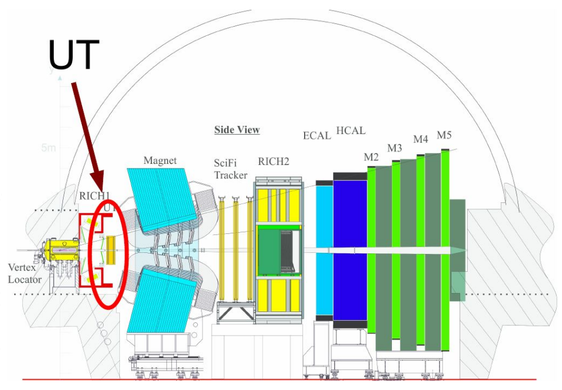
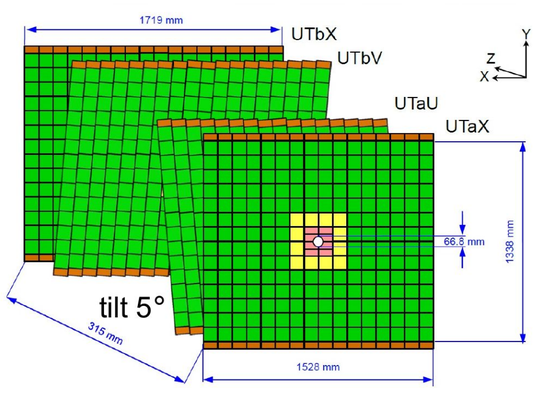
Premises for the development of SALT

The **L**arge **H**adron **C**ollider **B**eauty (LHCb) experiment is one of the four main experiments at the **L**arge **H**adron **C**ollider (LHC). Nevertheless, LHCb was designed to measure CP violation and rare decays of *b* and *c* flavoured hadrons with high precision, it has expanded its programme to a wide range of particle physics topics. Hence, the LHCb experiment benefits from the very large *b* and *c* flavoured hadrons production cross sections at LHC. Following upgrade of the LHC accelerator will allow providing more than one order of magnitude higher luminosity than nowadays used by the LHCb detector.



- LHCb detector is potentially limited by readout electronics and data acquisition architecture.
- An upgrade is needed to run at a higher luminosity while maintaining or increasing the efficiency of selecting signal candidates.
- New faster front-end electronics needed to run at 40 MHz bunch-crossing frequency.

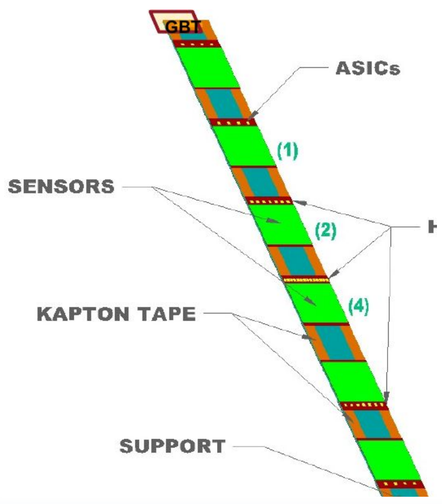
New Upstream Tracker for the LHCb upgrade



- Higher data rates means the detector trigger system needs to be completely redesigned.
- The low-level hardware trigger will be completely removed and the initial filtering of physics events will be passed on to a new flexible software-based trigger.
- The entire tracking system is planned to be upgraded.
- The **U**pstream **T**racker (UT) will be installed upstream to the bending magnet instead of a current tracker, called **T**racking **T**uricensis (TT), making it a central part of the tracking system.

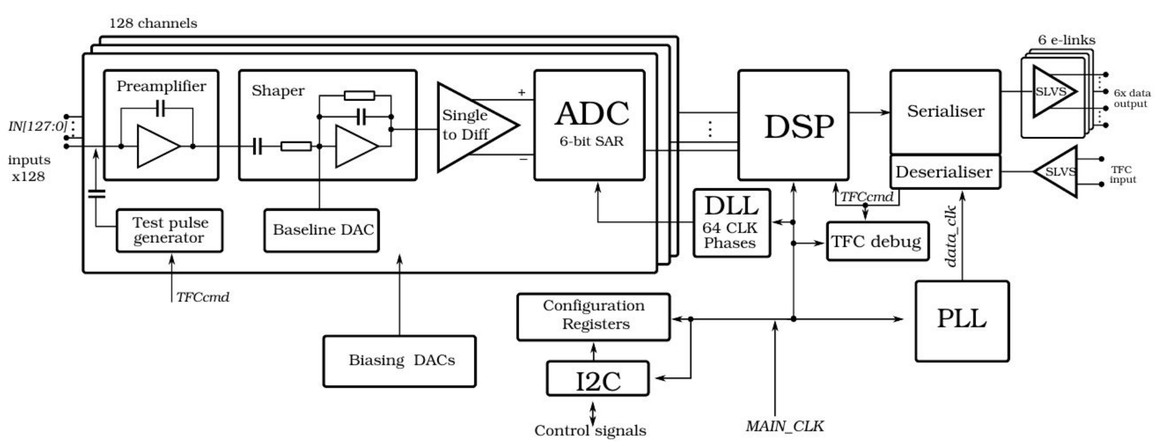
- The UT is built with silicon strip sensors with pitch ~ 95 and 190 μm and two lengths 5 and 10 cm.
- The UT will consist of four planar detection layers covering the full acceptance of the experiment. In total, the detector will use about 1000 silicon sensors.

The full height of the UT acceptance will be covered by 130 cm long staves which are going to host detector modules with 4 or 8 ASICs on it. The staves consist of light-weight foam embedded between two sheets of carbon fibre. Embedded titanium cooling pipes with circulated innovative bi-phase $C0_2$ will be used for cooling of the silicon sensors and the front end electronics. Output signals and control signals, low-voltage power for the front-end chips and bias voltage for the silicon sensors are transported along the staves via kapton flex cables that are glued onto both at sides of the stave. Each of these cables carries up to 120 high-speed differential pairs with a total of 38.4Gbps and 8A of current to power up to 24 ASICs while maintaining a minimal material budget and being easy to manufacture.



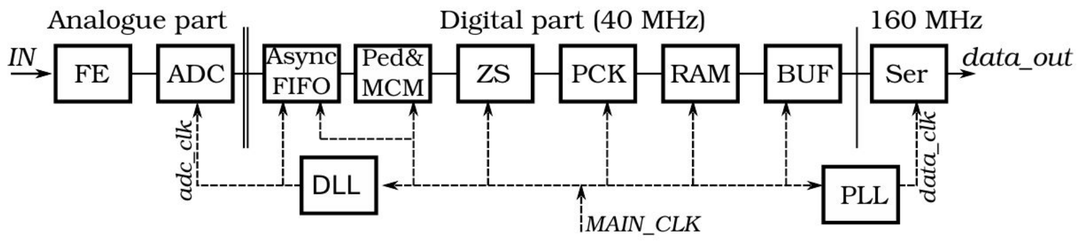
SALT - new readout chip for UT in LHCb

One of the most challenging tasks of the tracking upgrade is to design and implement a new front-end electronics allowing a full detector read-out at 40 MHz. A critical part of the entire UT detector is new readout **A**pplication **S**pecific **I**ntegrated **C**ircuit (ASIC) called SALT (**S**ilicon **A**SIC for **L**HCb **T**racking).



- SALT is designed in 130 nm **C**omplementary **M**etal–**O**xide–**S**emiconductor (CMOS) technology.
- 128 input channels each with an analogue front-end and an ultra-low power fast sampling 6-bit ADC.
- The front-end is adjusted to work with sensors capacitances between 5–20 pF
- Both input signal polarities (p +-in-n and n +-in-p).
- Signal to noise ratio > 10.
- Pulse shape: Tpeak ~25 ns, very short tail: ~5% after 2*Tpeak
- The maximum crosstalk is < 5% between channels.
- DSP functions: pedestal and common mode subtraction, zerosuppression.
- Serialization & Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C

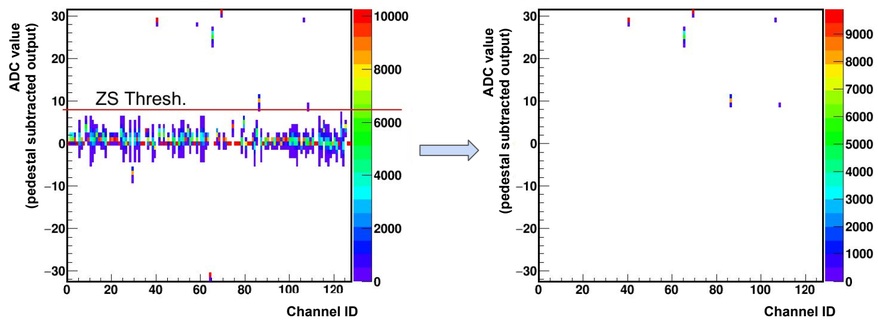
SALT – Silicon ASIC for LHCb Tracking DSP and Data Processing Chain



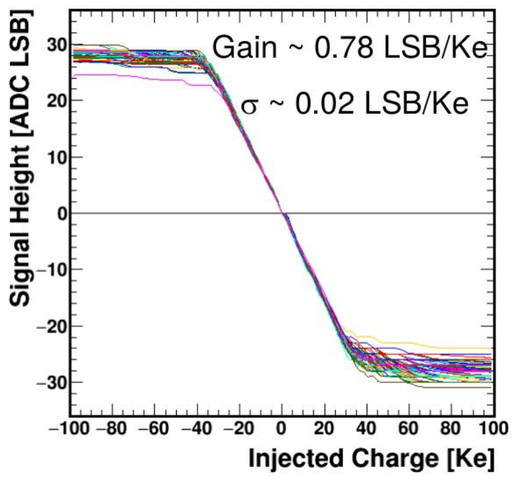
- Input is presented by 6 bits data-stream from ADC (5 bits for each polarity)
- Noisy or dead channels can be masked.
- All channel values can be inverted.
- Pedestal subtraction can be done for each channel with a different value.
- Possibility to subtract Mean Common Mode in each channel.
- Option to send out only channels above some threshold (Zero Suppression).

Tests of the 128-channel prototype

Digital Tests: Zero Suppression

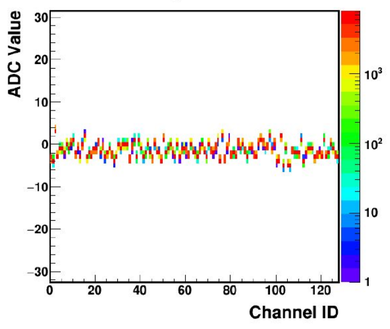


Analogue Tests (using the internal calibration)
Pulse Shape

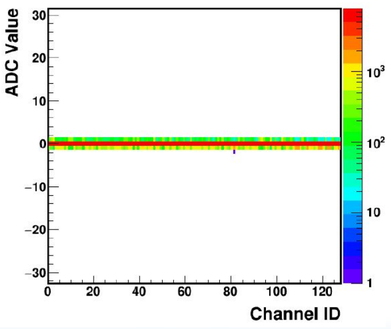


Analogue Tests (using the internal calibration)
Baseline correction

Before adjustment



After adjustment



Summary

The low-power readout 128-channels ASIC for the future Upstream Tracker at the LHCb experiment is mostly developed and tested. The new radiation-hard front end readout chip is based on 130 nm TSCM technology and has built-in DAQ part which incorporates preamplifier, shaper and a fast sampling 6-bit ADC in each channel, pedestal and common-mode subtraction, zero-suppression and data serialization.
The correct expected functionality of different chips' blocks was checked, and the detailed tests of ADC, PLL, DLL have been performed with a fabricated 128-channel prototype.

References

1. P. Campana et al., *LHCb Trigger and Online Upgrade Technical Design Report, CERN*, Geneva, CERN-LHCC-2014-016 (2014).
2. Ch. Parkes et al., *Preliminary Specification of a Silicon Strip Readout Chip for the LHCb Upgrade,* CERN, Geneva, LHCb-PUB-2012-011 (2012).
3. Sz. Bugiel et al., *SALT, a dedicated readout chip for high precision tracking silicon strip detectors at the LHCb Upgrade*, 2016 JINST 11 C02028, 28 September – 02 October 2015