Studies on the SALT ASIC, a novel front end electronics for the LHCb Upgrade

SALT - new readout chip for UT in LHCb

One of the most challenging tasks of the tracking upgrade is to design and implement a new front-end electronics allowing a full detector read-out at 40 MHz. A critical part of the entire UT detector is the new readout, Application Specific Integrated Circuit (ASIC) called SALT (Silicon ASIC for LHCb Tracking).

SALT is designed in 130 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology. 128 input channels each with an analogue front-end and an ultra-low power fast sampling 6-bit ADC. The front-end is adjusted to work with sensors capacitances between 5–20 pF. Both input signal polarities (+ in+n and n + in-p), Pulse shape: Tpeak ~25 ns, very short tail: ~5% after 2*Tpeak, The maximum cross talk is < 5% between channels. DSP functions: pedestal and common mode subtraction, zero suppression. Serialisation & Data transmission: 320 Mbps e-links to GBT, SLVS I/O. Slow control: I2C.

SALT – Silicon ASIC for LHCb Tracking DSP and Data Processing Chain

Tests of the 128-channel prototype

Analogue Tests
(used the internal calibration)

Gain ~0.78 LSB/Ke
σ ~ 0.02 LSB/Ke

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New Upstream Tracker for the LHCb upgrade

The UT will consist of four planar detection layers covering the full acceptance of the experiment. In total, the detector will use about 1000 silicon sensors. For the UT silicon sensors, the sensors are transported along the staves via kapton flex cables that are glued onto both sides of the stave. Each of these cables carries up to 120 high-speed differential pairs with a total of 38 Gbps and 8A of current to power up to 24 ASICs while maintaining a minimal material budget and being easy to manufacture.

Higher data rates means the detector trigger system needs to be completely redesigned. The low-level hardware trigger will be completely removed and the initial filtering of physics events will be passed on to a new flexible software-based trigger. The entire tracking system is planned to be upgraded. The Upstream Tracker (UT) will be installed upstream to the bending magnet instead of a current tracker, called Tracking Turicensis (TT), making it a central part of the tracking system.

Premises for the development of SALT

The Large Hadron Collider Beauty (LHCb) experiment is one of the four main experiments at the Large Hadron Collider (LHC). SALT was designed to measure CP violation and rare decays of b and c flavoured hadrons with high precision. It has expanded its programme to a wide range of particle physics topics. Hence, the LHCb experiment benefits from the very large b and c flavoured hadrons production cross sections at LHC. Following upgrade of the LHC accelerator will allow providing more than one order of magnitude higher luminosity than nowadays used by the LHCb detector.

LHCb detector is potentially limited by readout electronics and data acquisition architecture. An upgrade is needed to run at a higher luminosity while maintaining or increasing the efficiency of selecting signal candidates. New faster front-end electronics needed to run at 40 MHz bunch-crossing frequency.

Summary

The low-power readout 128-channels ASIC for the future Upstream Tracker at the LHCb experiment is mostly developed and tested. The new radiation-hard front end readout chip is based on 130 nm TSGM technology and has built-in DAQ part which incorporates preamplifier, shaper and a fast sampling 6-bit ADC in each channel, pedestal and common-mode subtraction, zero-suppression and data serialization. The correct expected functionality of different chips’ blocks was checked, and the detailed tests of ADC, PLL, DLL have been performed with a fabricated 128-channel prototype.

References