The timing system of the TOTEM experiment

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(on behalf of the TOTEM collaboration)

4th Elba Workshop on Forward Physics @ LHC Energy
OUTLINE:

- Experiment overview
- Timing detectors - UFSD
- SAMPIC integration
- Project status
- Preliminary results

TOTEM experiment

TOTEM RP stations (>200 m from IP)
Roman Pots stations

- Vacuum vessel entering the beam pipe, can be equipped with many types of detectors.
- Scattered protons with very-low $|t|$ can be detected
- Standard units composed of 3 RP (2 vertical, 1 horizontal)

Distance from IP5 200-220 m

4 different detector technologies are actually hosted by the TOTEM RPs:
- Silicon strip (tracker)
- Silicon pixel (tracker)
- Diamond detector (timing)
- UFSD detector (timing)
LHC Optics

- Special LHC optics (high-$\beta^*$, low beam div.) has been developed to measure elastic scattering at low $|t|$.
- Parallel to point focusing is particularly effective to reduce primary vertex uncertainty impact on the scattering angle resolution.

$\sigma_{\theta^*_y}$ limited by beam divergence
$\sigma(\theta^*_y) < 1\mu\text{rad}$

$\sigma_{\theta^*_y}$ limited by beam divergence $\oplus$
detector res.
$\sigma(\theta^*_x) \sim 10\mu\text{rad}$

Data taking in standard (high luminosity) run also possible with the horizontal pot $\rightarrow$ PPS project.
RP configuration for High $\beta^*$ runs

- 6 Vertical RPs
- 2 Horizontal RPs (only alignment)

- 4 Tracking (strip)
- 2 Timing (UFSD)
- 2 Tracking (pixel)
CMS and TOTEM works together to performs CEP studies. Trigger information are exchanged and data can be offline merged.

- Comparison/prediction from forward (TOTEM) to central (CMS) system: $M_{PP}$, $p_{T,z}$, vertex

With CMS data central exclusive production can be investigated with strong BG rejection.

For CEP studies in standard LHC condition the PPS detector (based on TOTEM RP system) has been developed.

$M_{PP} \sim \sqrt{\xi_1 \xi_2 s}$

$\Delta \eta_{1,2} = -\ln \xi_{1,2}$

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Timing detectors

Higher the LHC luminosity, higher the probability to have more than one simultaneous pp interaction (with mean $\mu$)

Reconstruction of primary vertex of detected protons with TOTEM Roman Pots (RPs) limited $\rightarrow$ difficult if $\mu > 0.1$

Max luminosity mandatory to access low cross-sections ($\mu \sim 1$ for 90 m run, much higher in standard runs)

Measure of the proton time of flight in the two arms:

$Z_{PP} = c\Delta t/2$

With few tens of ps resolution (for MIP)

sCVD Diamond and UFSD detectors developed. Both technologies actually used in the RP.
Timing resolution

\[ \sigma_{tot}^2 = \sigma_{jitter}^2 + \sigma_{walk}^2 + \sigma_{digi}^2 \]

Requirements for a good timing:

- High SNR and slew rate of the sensor signal
- Signal shape must be constant
- Possibility to perform time walk correction
  
- Time over Threshold
- CFD
- Signal charge measurement

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- CFD
- Signal charge measurement
- Signal sampling

Sampling allows sophisticated offline algorithm (CFD and more)
UFSD sensors

UFSD are LGAD (Low Gain Avalanche Detector) optimized for timing:

- Reduced sensor thickness (~50 um)
- High (E~300 kV/cm in the multiplication region) and uniform electric field
- Small size to keep capacitance low

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<th>Surface [mm²]</th>
<th>Capacitance [pF]</th>
<th>HV [V]</th>
<th>Time precision [ps]</th>
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</tbody>
</table>

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Detector assembly

(UFSD, Si-ultrafast) from Torino (FBK)

One RP hosts 4 detector planes.

Factor 2 improvement in timing performances

Each sensor is divided in 12 sectors, with geometry optimized:
- Uniform occupancy with 90 m optics
- Double hit probability negligible
- Low number of channels
Both Diamond and UFSD sensor have similar characteristics of the output signal:

- Rise time $\sim 0.5 – 1.5$ ns
- SNR $\sim 30 – 50$
- Amplitude $\sim 300$-700 mV

Why SAMPIC:

- To achieve maximum resolution a fast sampling (5-10 Gsa/s) of the signal is needed.
- Low channel dead time and high input rate are also needed, even for $\mu \sim 1$.
- Low cost/channel ($\sim$200)

Fast sampler (SAMPIC)

ToT Discriminator + TDC (NINO+HPTDC)

Used in CT-PPS due to the input rate ($\sim$ 1 MHz/channel).
16 channel/chip
64 sample/hit @ 6.4 GSa/s
1.5 GHz bandwidth
8-11 bit resolution
0.25-1.6 µs channel dead time

• Self trigger (2ns max latency on central)
• No event building
• Each sampled signal sent out

Sampic
LHC test

Tested in the LHC tunnel in 2015:

- sCVD diamond detector with ~90 ps intrinsic resolution (sensor + amplifier)
- Standard module from LAL
- 6.4 GSa/s with 11 bit ADC resolution
- No loss of resolution compared to oscilloscope!

\[ \sigma_t \sim 90 \text{ ps} \]

AGILENT DSO9254A (2.5 GHz BW; 20 GSa/s)

No resolution loss!

\[ \sigma_t = 91 \text{ ps} \]
Special needs for the SAMPIC for real data taking:

- Chip configuration with I²C
- Readout with optical link (GOL chip)
- Compatibility with the high precision clock distribution
- USB interface for debugging and test beam
Digitizer board developed to integrate SAMPIC or HPTDC mezzanine in TOTEM/CMS environment.

All functionality are handled by the a radiation tolerant FPGA (Microsemi Smartfusion M2S150)
TOTEM TOF system

Each RP hosts 4 detection planes

One arm of the TOTEM timing system

48 channel

48 channel
Trigger latency ~ 6 us
1 Frame for each trigger
No frame if no trigger
Max frame size ~ 350 B
Trigger rate up to 100kHz

Hit selection, frame building and data reduction to be done inside Digitizer central FPGA (Microsemi SF2)
Frame Filter

- Delay of incoming frames
- Check frame integrity (header, trailer, WC)
- Timestamp reconstruction and matching with trigger list
- Event rejected or send to channel FIFO
- USB readout available
Event builder

- Selection of up to 7 matching channels
- Event built after ~100 us from trigger arrival to collect all frames
- Assembly of global event info
- Data reduction (factor ~ 0.5)
- Serialization of the event stream
- GOH output (16 bit data bus)

Actual SAMPIC configuration:

7.8 Gsa/s @ 8 bit resolution
24 samples
Clock system

- LHC clock is derived from CMS TCDS (Timing Control Distribution System)
- System delay changes over optical path is constantly monitored -> 1 measurement every 10 min.
- Data stored to files in csv format file rotation system -> 1 file per day.
- Clock jitter measured at RP receiver <2ps

New clock source based on Silicon Lab 5344 chip:
• Zero delay mode \(\rightarrow\) constant phase delay between input and output
• Clock phase will be tuneable in \(~18ps\) steps.
Lab test & operation in LHC

UFSDs were tested (IV, noise, Sr90, ...)

SAMPIC and firmware were tested in the lab thanks to the possibility to configure and read the Digitizer Board using USB. SAMPIC modules optimized (sampling frequency, LV, baseline).

- All detector package installed during YETS 2018
- 2/3 of the electronics installed in YETS 2018, completion during TS1

Operation:

- Low-β alignment
- LHC luminosity rump-up (13 pb\(^{-1}\) during 75b fill)
- 900 GeV test run

Not the right optics but many checks performed:

- Sensors (the ones readout)
- Electronics and firmware
- DQM
- XDAQ for slow control
First results : tomography

Tomography

Timing Detector

Strip Tracking Detector
First results : tomography

X-Y given by the tracker, color given by the timing channel number

✓ Mapping checked
✓ Synchronization with the tracker system verified
First results: Hit Map

Hit maps for the fully equipped diagonal
Baseline: linear fit on the first samples
Baseline is subtracted to remove low frequency noise
Smoothing: low pass filter
Offline Constant Fraction Discriminator

Other algorithms tested, better performance with CFD

ADC and INL calibrations to be done
Conclusions

• Timing sensor based on UFSD technology has been realized for the TOTEM-CMS special run that will be done after TS1 (end of June)
• Sensors shows a resolution in the range 30-100 ps (depending on pixel size). 4 detection plane can be fitted in one RP
• The 4 vertical timing RP has been assembled and installed in YETS 2018

• Sensor readout will be done through the SAMPIC chip, a fast sampler.
• Dedicated firmware and digitizer board have been developed to integrate the chip in the TOTEM-CMS environment
• Part of the electronics installed in YETS 2018 and commissioned during the first LHC fill and RP alignment run. System will be completed during TS1.

• Preliminary results shows good quality waveform acquired with the SAMPIC readout.
• Synchronization with the tracker system verified
• Timing performance under study.
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