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Serial powering for pixels

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University of Bonn

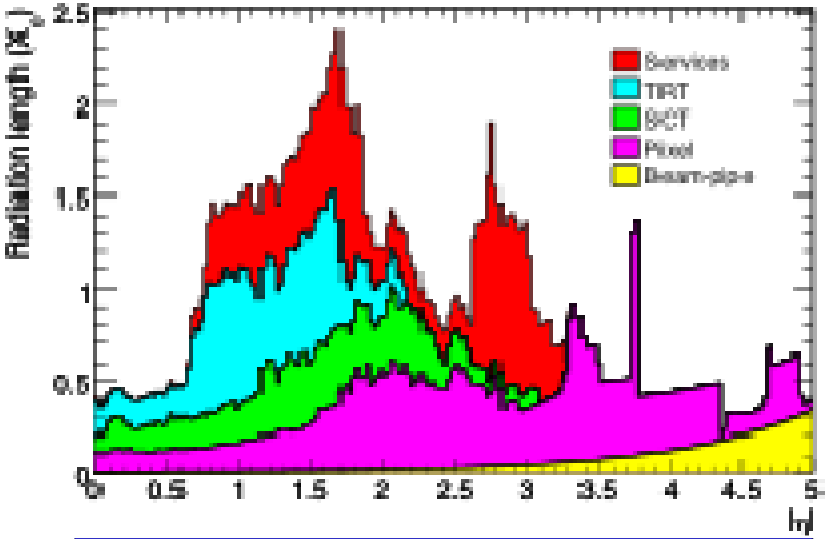
Outline

- Introduction
- Serial Powering concept
- Serial Powering for ATLAS Pixel
  - Power Converters & Regulators
  - Protection Issues
  - System Aspects

Pixel powering for sLHC

- Current ATLAS Pixel Tracker burns 70% power in cables!
  - ASIC supply voltages: 2.0V & 1.7V.
  - Total front-end power: 6kW.
  - Total current: 3.5kA
  - Loss in cables: 17kW.
- Situation is getting worse at SLHC since total cable cross section is fixed:
  - Services are dominating the material budget in certain areas and no more space for cables left.
  - FE power stays roughly the same while current is going up (130nm technology).
  - Cable loss scales with *current*^{2}.

→ need to transmit power at lower current!

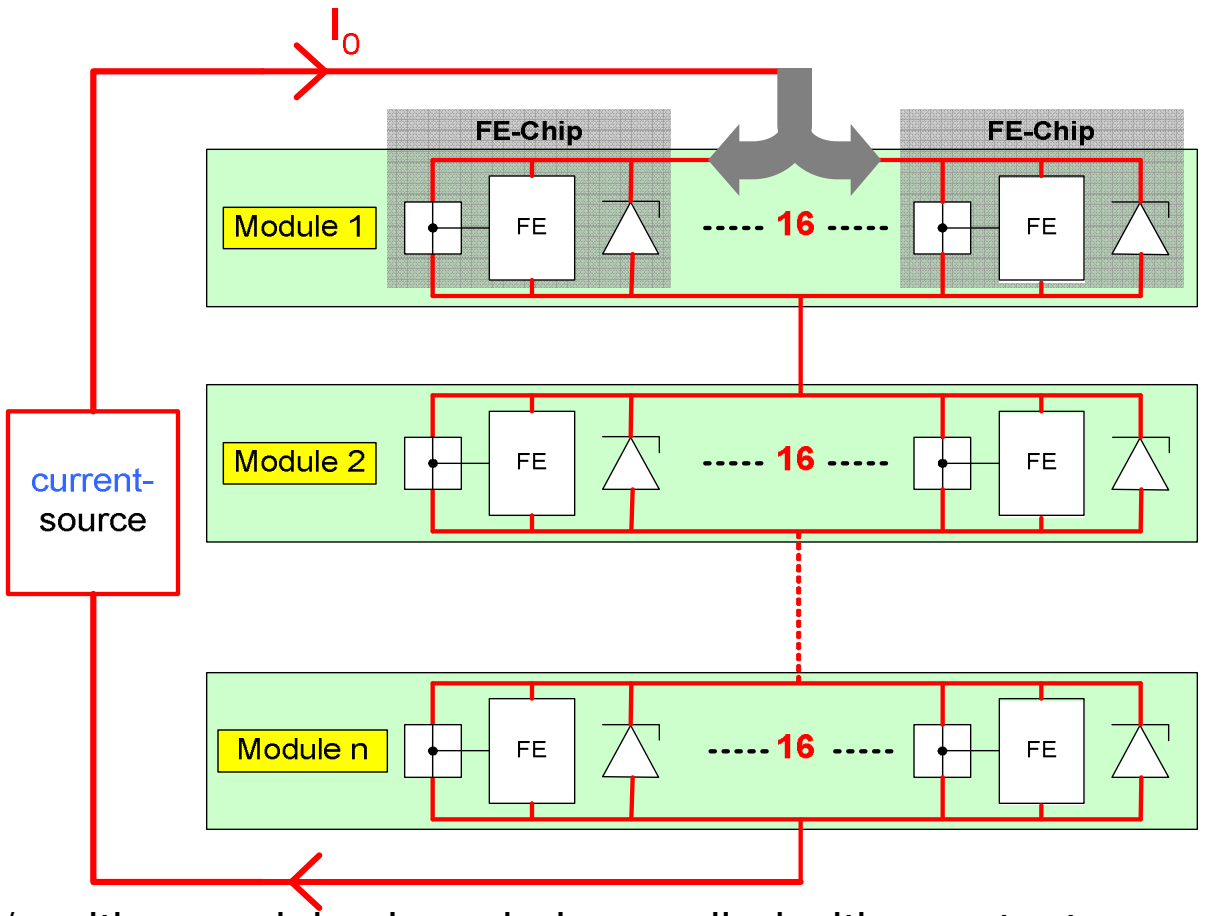


ATLAS Inner Det. Material Distribution

ATLAS Inner Det. Cables

ATLAS pixel detector services

Serial Powering Concept

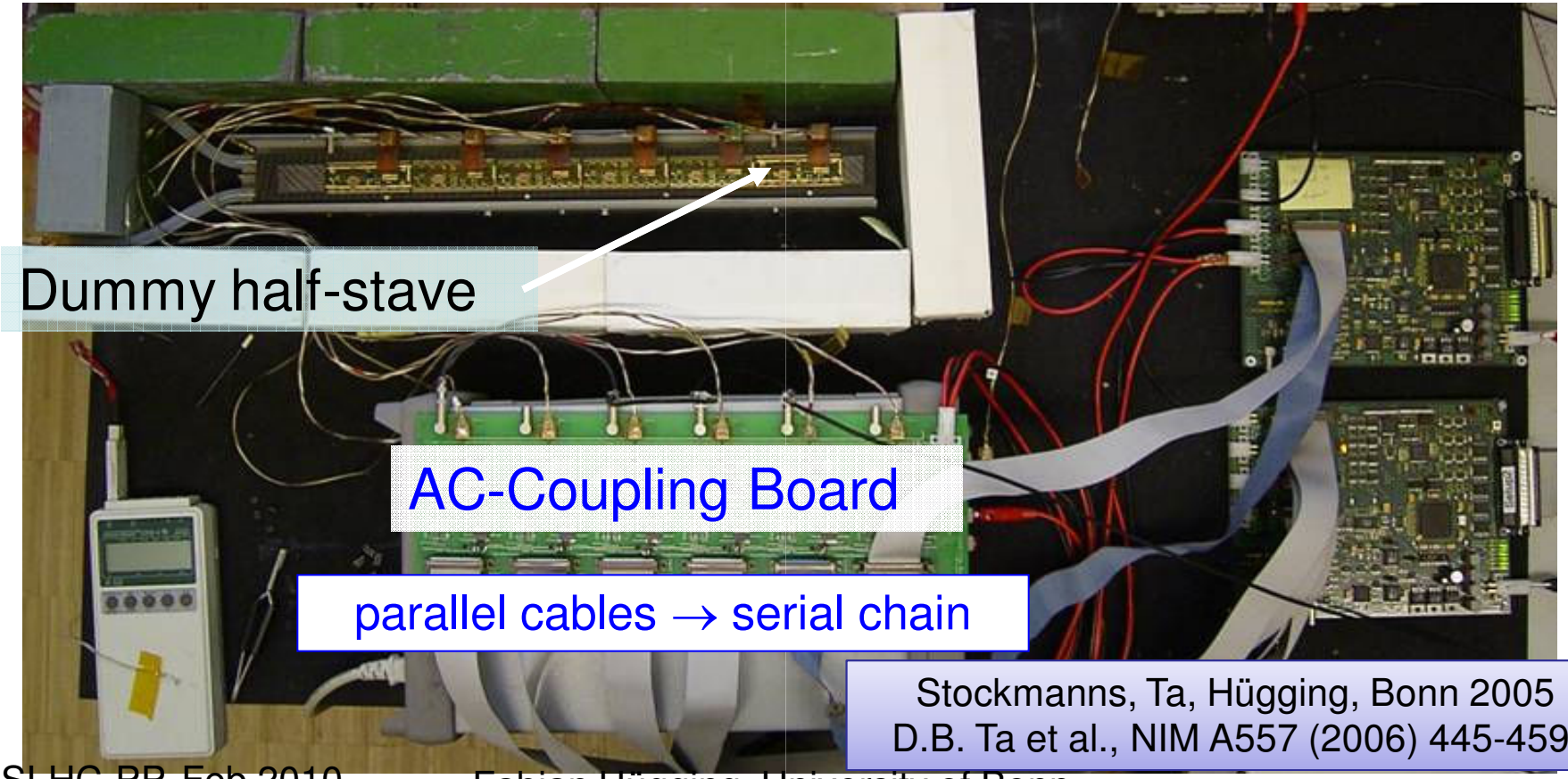


- V_{mod} = V/n with n modules in a chain supplied with constant current I_{mod}.
- Current through cables only $I = I_{mod}$ instead of $I = nI_{mod}$.

→ $P_{cable}(\text{serial powering})/P_{cable}(\text{parallel powering}) = R_{cable}I_{mod}^2/R_{cable}(nI_{mod})^2 = 1/n^2$

Serial Powering: proof of principle for pixels

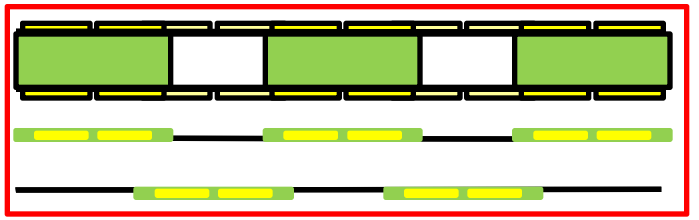
- Proof of principle has been demonstrated with a serially powered dummy half stave of the ATLAS Pixel Detector using 6 production like FE-I3 modules with internal shunt and linear regulators.
  - No performance degradation w.r.t. the parallel powering
  - High rejection capability against noise pickup injected into chain

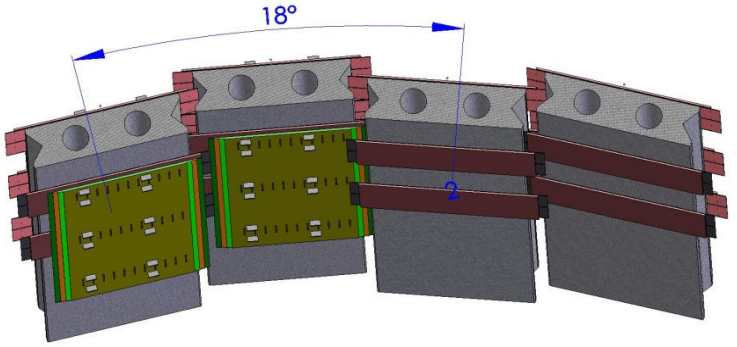


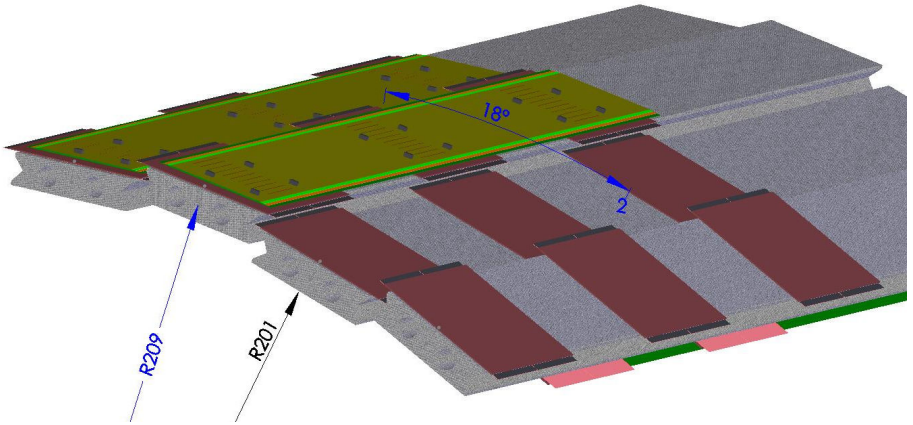
Stockmanns, Ta, Hügging, Bonn 2005
D.B. Ta et al., NIM A557 (2006) 445-459

SP for ATLAS Pixel at sLHC

- sLHC outer layers baseline:
  - 32 4-chip-modules using the new FE-I4 chip.
  - Modules are arranged on both sides of the stave.
  - 8 modules (half stave on one side) connected to a 1 End-of-Stave card.
- Serial power module group of 8 (could be 16 or 32 modules depending on the needs).
- Power is provided together with the signals on one flex hybrid which serves as module HDI as well.

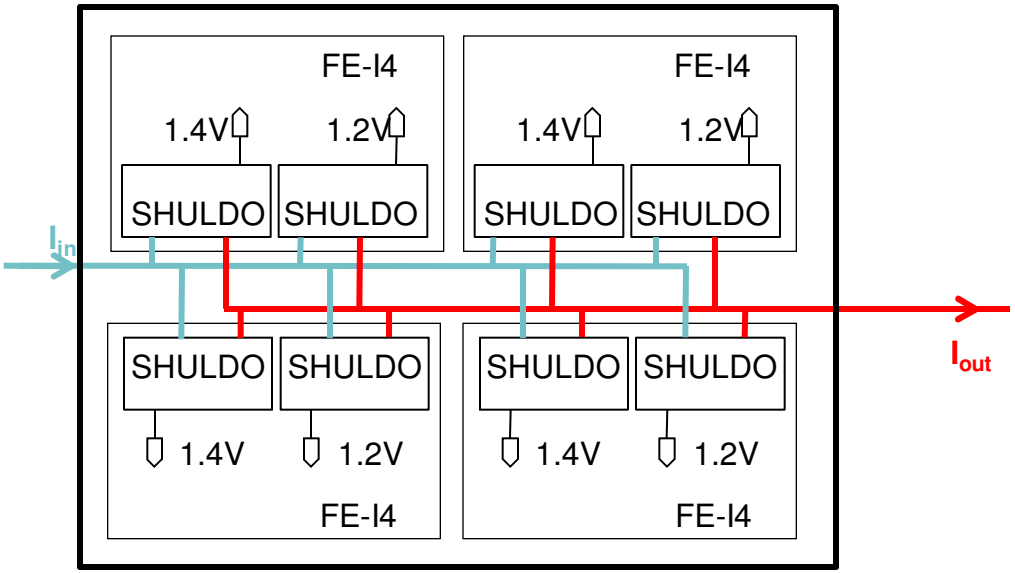






Module electrical Requirements

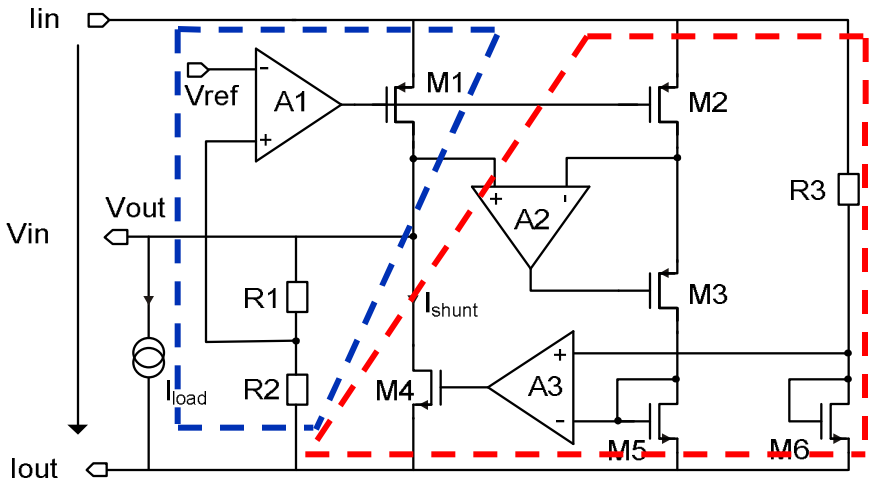
- FE-I4 power needs:
  - VDA = 1.4V
  - VDD = 1.2V
  - I = 600mA
- voltage regulators to generate a constant voltage out of the current supply.
- integrated regulation circuitry in every FE-I4.
  - avoid additional components on the module.
- 4-chip-module uses 8 regulators in parallel.
  - Redundancy.



- 2 SHULDOs/FE-I4
  - can operate in parallel and generate 2 different output voltages at the same time

ShuntLDO: Working Principle

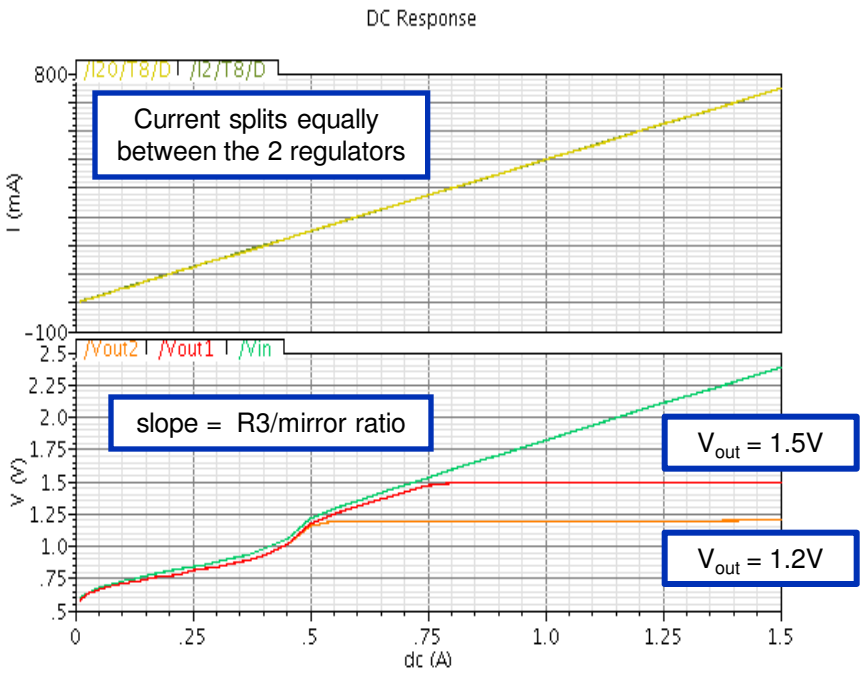
- combination of a LDO and a shunt transistor:
  - R_{slope} of the shunt is replaced by the LDO power transistor.
  - shunt transistor is part of the LDO load.
- shunt regulation circuitry ensures constant I_{load}:
  - I_{ref} set by R3, depends on V_{in} (→ I_{in}).
  - I_{M1} mirrored and drained in M5.
  - I_{M1} and I_{ref} compared in A3.
  - M4 shunts the current not drawn by the load.
- LDO regulation loop sets constant output voltage V_{out}:
  - LDO compensates output potential difference.



ShuntLDO: Features

- ShuntLDO regulators having different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution.
  - resistor R3 mismatch will lead to some variation of shunt current (10-20%) but will not destroy the regulator.
- ShuntLDO can cope with an increased supply current if one FE-I4 does not contribute to the regulation e.g. disconnected wire bond.
  - I_{shunt} will increase
- can be used as an ordinary LDO when shunt is disabled.
- test results and more details: see L. Gonella's talk.

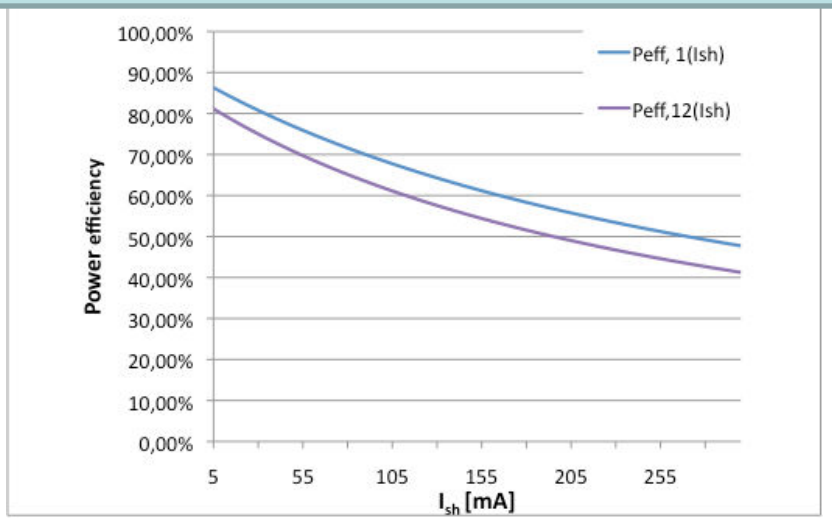
Parallel placed regulators with different output voltages
- simulation results -

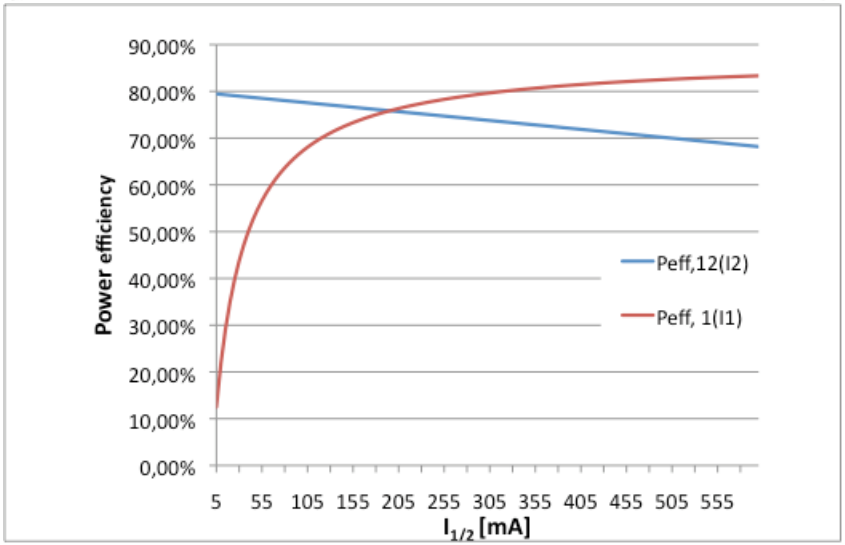


Power Efficiency

- Crucial point for SP is the power efficiency of the power converter.
- For the ShuntLDO 3 sources of inefficiency:
  - Dropout voltage V_{drop}
  - Shunt current I_{shunt}
  - Difference between the 2 output voltages ΔV needed by the FE.
- Calculations with conservative assumptions for ATLAS Pixel:
  - V_{drop}= 200mV, I_{shunt}= 30mA, ΔV= 200mV
  - Total current of the FE is 600mA with 250mV for the digital part at the lower output voltage of 1.2V.
- Power efficiency for single ShuntLDO is around 80% at realistic currents.
- Power efficiency for parallel operation of 2 ShuntLDOs at 1.2 and 1.4V is ~75%.

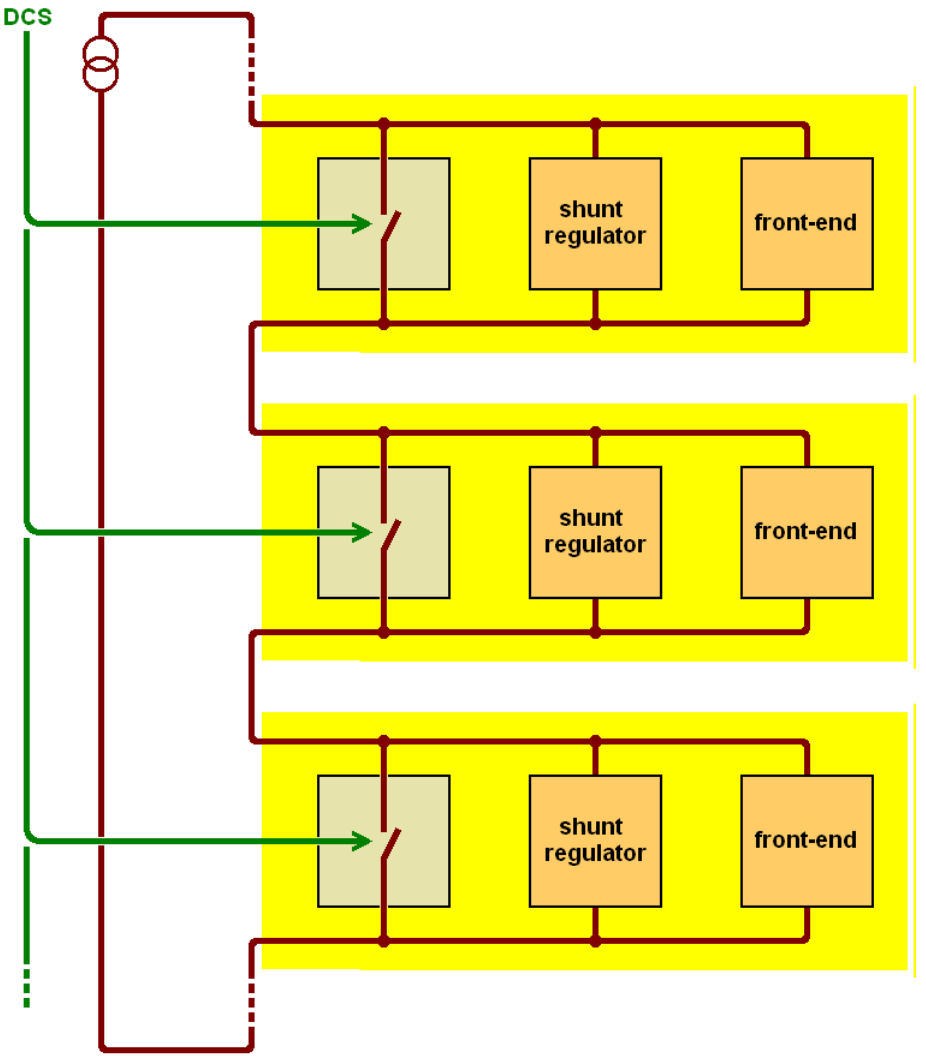
Power Efficiency of 2 parallel ShuntLDOs





Protection for Serially Powered Staves

- Purpose:
  - Assure supply of power to the serially powered chain in case of failures.
    - Broken wire bonds, overvoltage.
  - Allow power to arbitrary selection of modules.
    - Switch off a noisy module.
- Requirements:
  - Slow Control: DCS should be able to switch off selected modules.
  - Fast Response: Over-voltage protection.
  - Residual voltage (when module off) < 100mV
  - During normal operation (module on) protection draws no power.
  - Minimise number of components, area of components and bus-cable lines.
  - Radiation hardness.
- Impementation for Pixel Stave:
  - Module Protection Chip.



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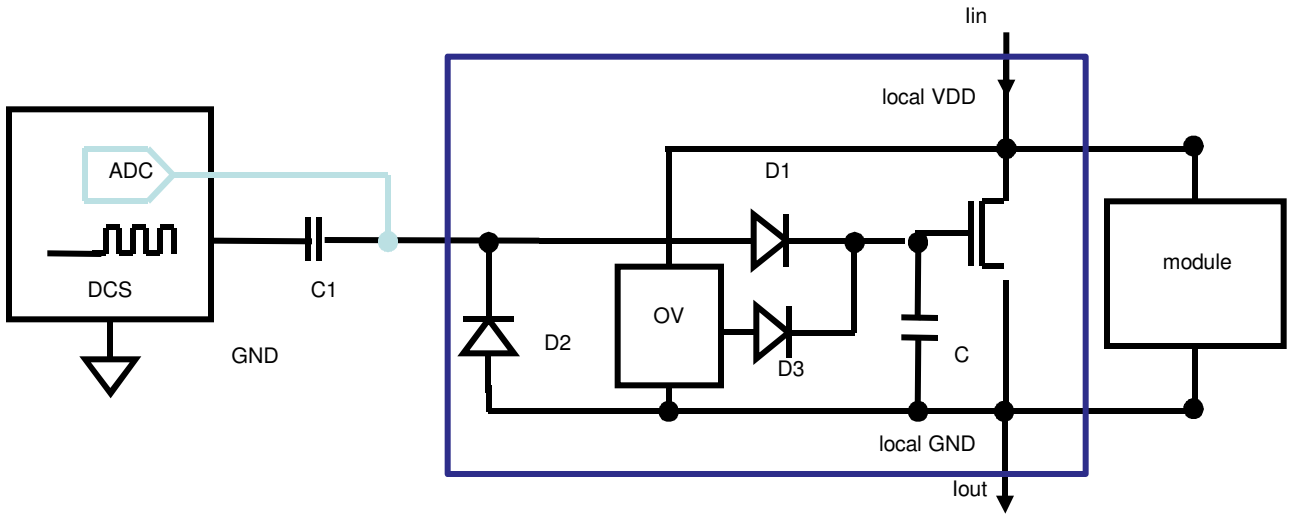
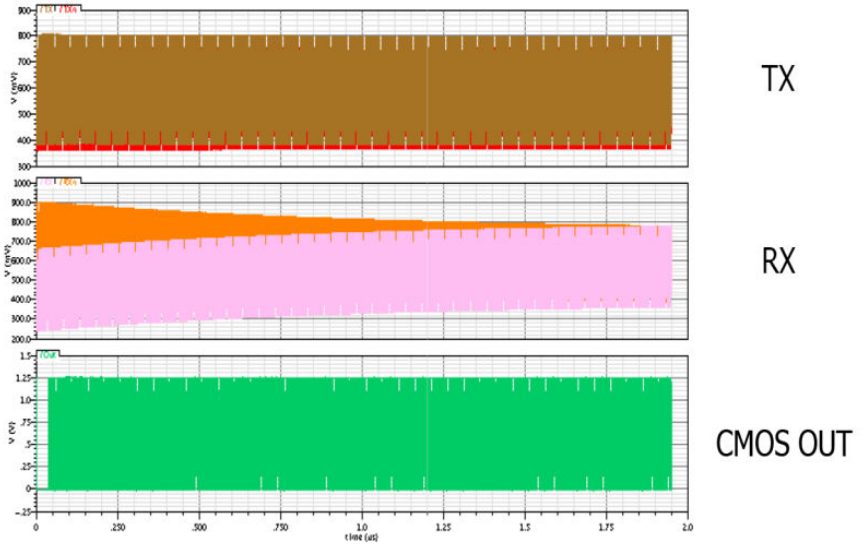
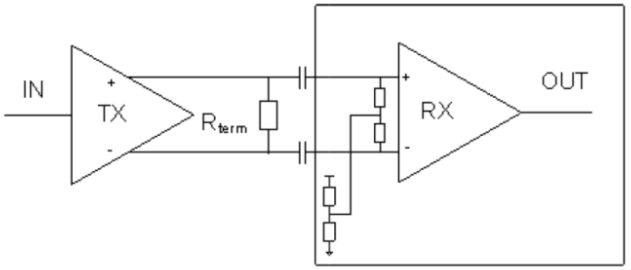


- 130nm CMOS technology.
- bypass transistor.
- AC-coupled slow control line:
  - can be used to monitor module voltage when idle.
- independent over voltage protection circuitry.
- development status (see L. Gonella's talk):
  - bypass transistor and slow control simulations completed.
  - over voltage protection circuitry in development.

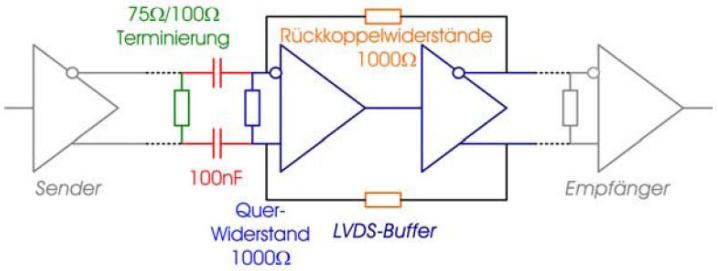
AC coupling

- AC-coupling at LVDS TX/RX level:
  - Simple and less material.
  - Requires DC-balance and self-biased RX inputs.
  - Integrated self-biasing circuitry for LVDS RX input will be added in FE-I4.
    - design finished.



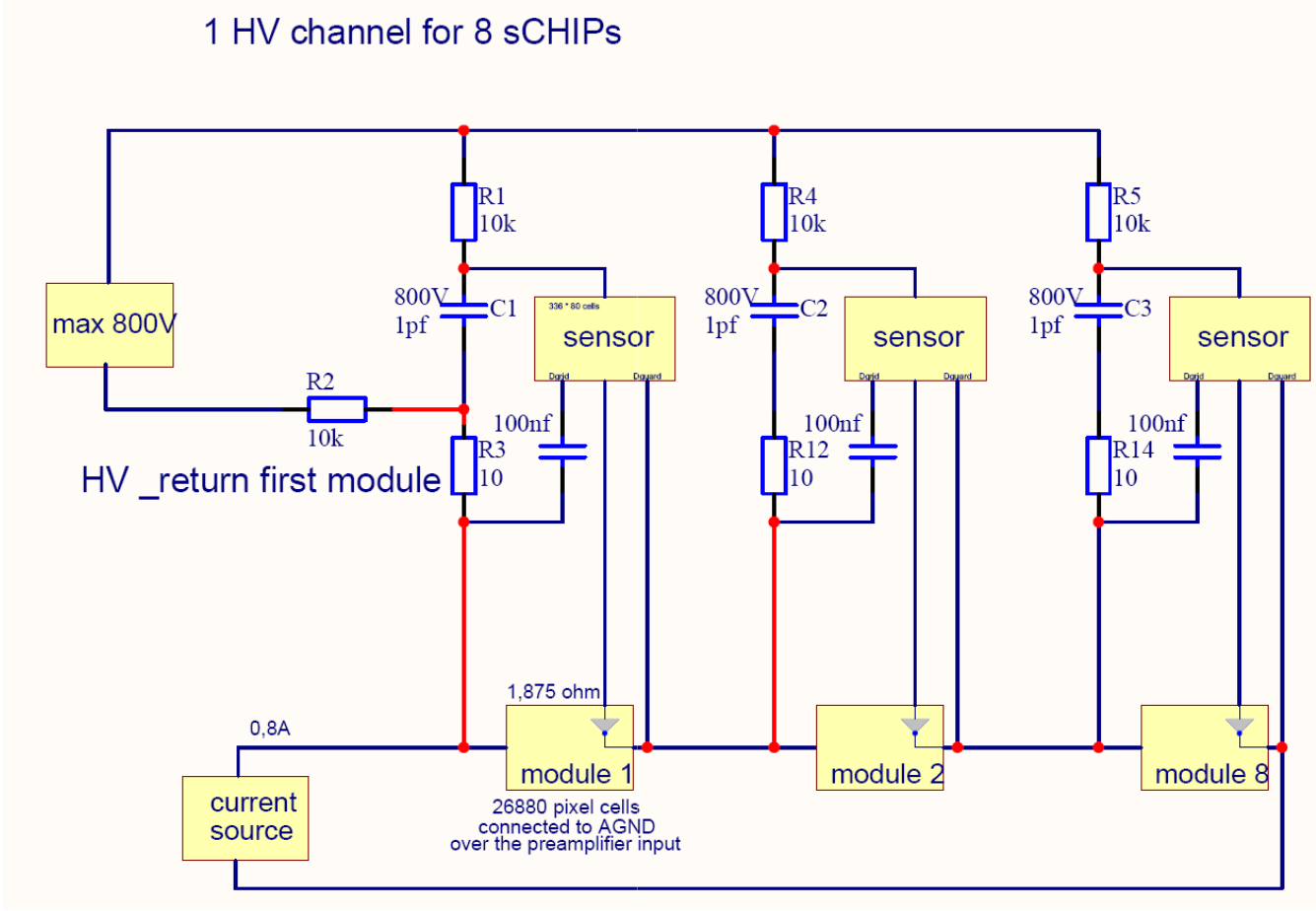


- Otherwise usage of a link with feedback:
  - Used successfully in SP Proof of Principle.
  - No need for DC balancing and self-biasing.
  - Acts also as well as a fail safe (keeps the last state).



HV distribution

- Use one floating HV supply per module → no problem.
- Use 1 HV supply per power group → several schemes possible, e.g. using the serial power line as HV return.



Summary

- A **serial powering scheme** for the ATLAS pixel detector for sLHC is being developed in Bonn:
  - A new regulator concept, the **SHULDO**, has been successfully prototyped and tested, with a **nominal power efficiency of 75%** for 2 SHULDO in parallel generating different output voltages.
  - A **protection scheme** for the SP chain of modules is being developed which includes both slow control and real time response.
  - **AC-coupling** at TX/RX level is preferred and thus a self-biasing LVDS RX input circuitry will be implemented in FE-I4.
  - **HV distribution** options have been proposed and will be tested.

- **Realistic SP system tests** will start as soon as FE-I4 module prototypes are available.

- Systems tests can (and have) already start with the **pixel stave emulator**, see L. Gonella's talk.