Stave Emulator and Regulator Test

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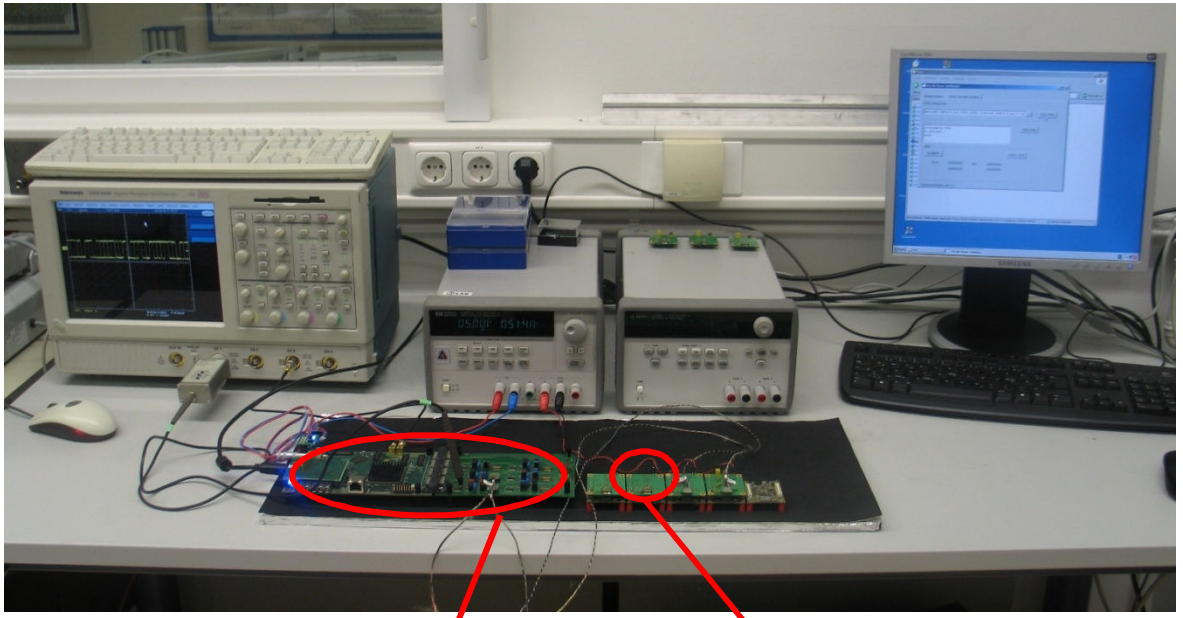
Stave Emulator Test Bench

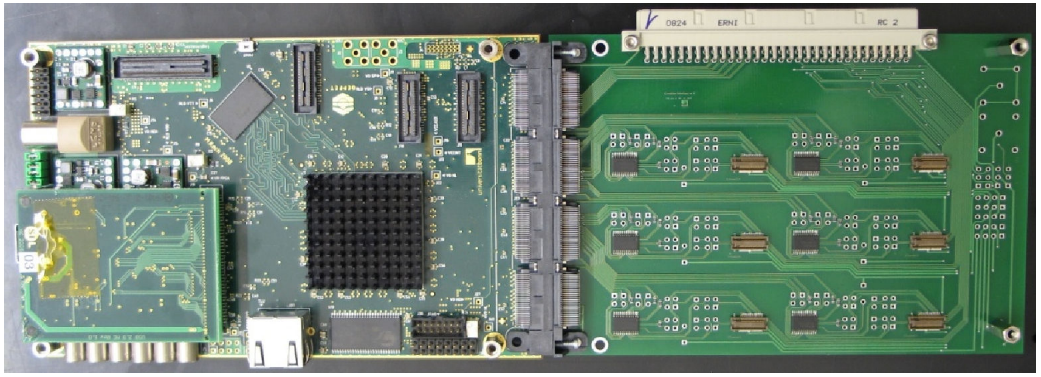
- The stave emulator is a test system which allows to evaluate system aspects and custom developed hardware for the ATLAS Pixel Detector for sLHC, such as
  - physical layer data transmission: LVDS drivers/receivers, cables, connectors, …
  - data coding schemes: raw, 8B/10B, 64B/66B, …
  - powering concepts: serial, dc-dc, switched cap, …
  - DCS concepts: voltage monitoring, control of bypass switch, reset, …
  - data management of the End-Of-Stave controller, ...
  - …
- It uses
  - FPGAs to emulate the modules and the end-of-stave controller
  - interconnection boards to provide support for different cable and connector options, LVDS transceiver chips, power supply options (parallel, DC/DC or SP), AC-coupling
  - a DCS test board (COBOLT) developed in Wuppertal providing multi-channel ADC and GPIO to test DCS functionalities

→ flexible and realistic test bench

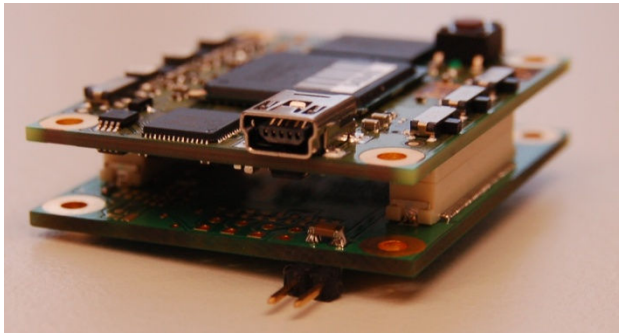
Stave Emulator



End-Of-Stave emulator unit



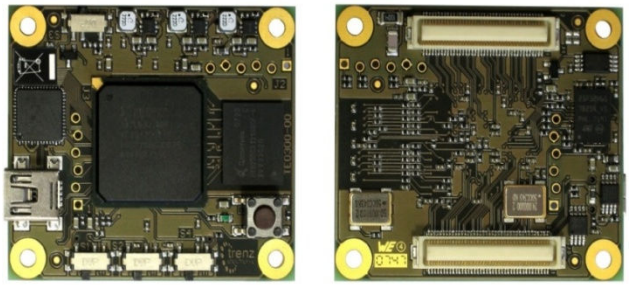
Module emulator unit



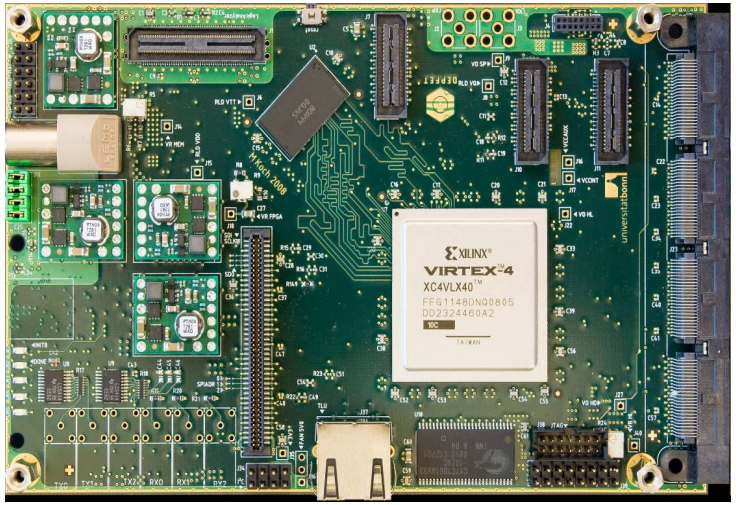
Hardware

- FPGA Boards
  - Module → Spartan 3E FPGA
    - Commercial FPGA board (Trenz TEO300B)
    - Spartan XC3S1600E, 64 Mbyte DDR RAM, 32 Mbit Flash, USB interface
    - Approx. size of a 2x2 FE-I4 module
  - End-Of-Stave Controller → Virtex4 FPGA
    - FPGA board developed in Bonn for read-out of DEPFET modules
    - XILINX Virtex 4 LX40-1148, 288Mbit RLDRAM – Should be able to handle >14.4Gbit/s, µC-based system monitor (ADM1062), USB 2.0 connector, 16Mbit async. SRAM, EUDET TLU connection, Multiple high speed connectors
- Interconnection boards
  - Custom developed
  - Tailor different test wishes (data transmission, powering option, …)
  - Define successive stave emulator versions
    - Iterate the design of interconnection boards to add more functionalities and custom developed hardware when available

Spartan 3E board



VIRTEX4 board

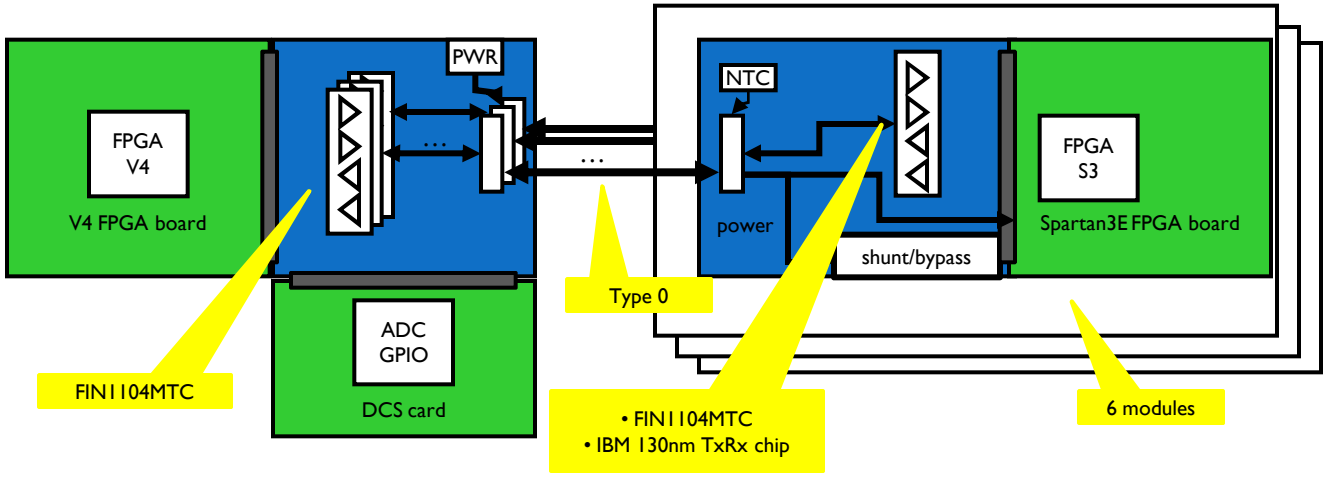


Firmware and Software

- Firmware for data transmission tests
  - PRBS of different length, 8b10b encoded data
  - FE-I4 code for Spartan3E
  - Bit Error Rate firmware for Virtex4
    - uses PRBS;
    - clock frequency synthesized with Digital Clock Manager;
    - compares data out with data in;
    - delay adjustment between data out and data in done in 2 steps: coarse delay = 1clk period, fine delay = 75ps

- Software
  - Application developed with C++ and Qt (GUI) allows to download firmware on the FPGA, read/write data from/to FPGA

Baseline Design



- "6 modules-stave"
- Connection EoS - module using Type 0 cable
- Powering
  - parallel
  - serial using commercial shunt regulator
    - commercial bypass transistor on modules to test protection option
- DC-coupled data transmission with different LVDS transceiver chips
  - on End-Of-Stave side: commercial FIN1104MTC transceiver chip
  - on module side: commercial FIN1104MTC or IBM 130nm transceiver chip (i.e. FE-I4 LVDS TX and RX)
- NTC to measure module temperature

Tests with Baseline Design

- Bit Error Rate Tests
  - study the performance of the LVDS TX and RX for FE-I4
    - Comparison with commercial transceiver chip
    - V_{dd} = 1.2-1.5V
    - I_{bias} higher than nominal
  - parallel powering, DC coupled data transmission, PRBS8-16-24, 160Mbps

  → IBM 130nm transceiver chip runs error free with PRBS24 at 160Mbps with V_{dd} = 1.2V($38e^{12}$ bits transmitted)

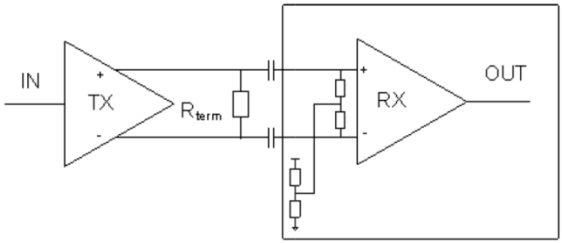
		Nominal	1.2V	1.5V
RX	I_{bn}	-35uA	**-100uA**	**-150uA**
	I_{bp}	35uA	**60uA**	**90uA**
TX	I_{bp}	60uA	**60uA**	**90uA**
	U_{bias}	600mV (1.2V) 750mV (1.5V)	600mV	750mV

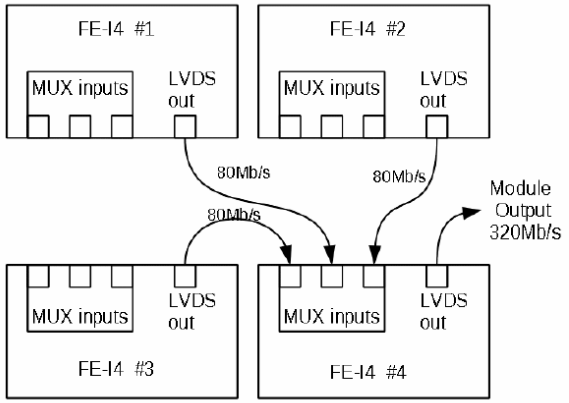
- Tests with COBOLT
  - Serial powering chain
  - Some DCS functionalities have been successfully tested
    - module temperature measuring with NTC
    - control of bypass transistor
    - monitoring of module voltage through bypass control line

Next Stave Emulator Version

- Second version of interconnection board for module emulator unit available
  - more custom-developed hardware
  - IBM 130nm LVDS transceiver chip
    - External biasing circuitry for RX inputs (→ AC-coupled data transmission)
  - IBM 130nm LVDS tri-state driver
  - ShuntLDO regulator
- Test plan
  - AC-coupling at TX/RX level with FEI4 LVDS transceiver chip
  - Multiplexing of data out of different FEs
    - w/ tri-state driver
    - FEs in master-slave configuration
  - Test of ShuntLDO regulator in a real serially powered system
    - Test of ShuntLDO pure LDO regulator operation with shunt capability switched-off

possible RX inputs self-biasing integrated circuit for FE-I4

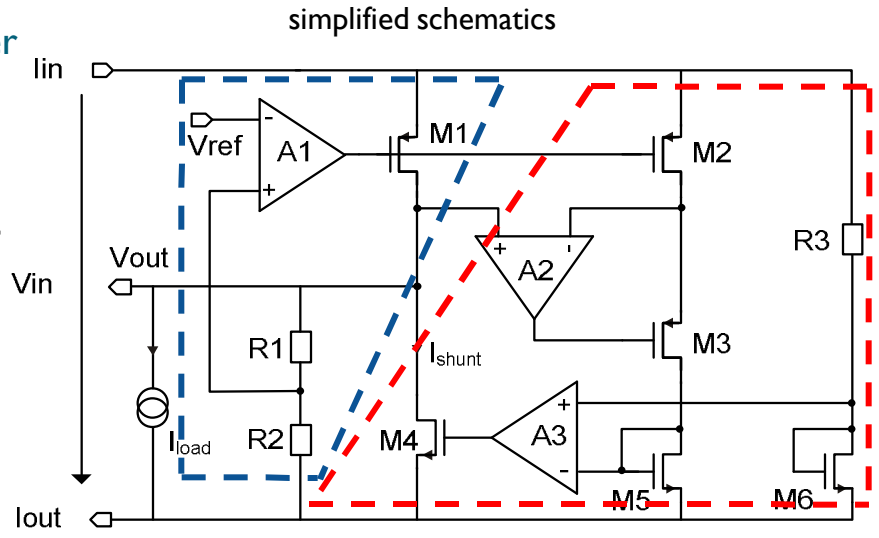




Goal: Set up a serially powered stave with AC-coupled data transmission and FE data output multiplexing, using real FE-I4 components

ShuntLDO: Working Principle

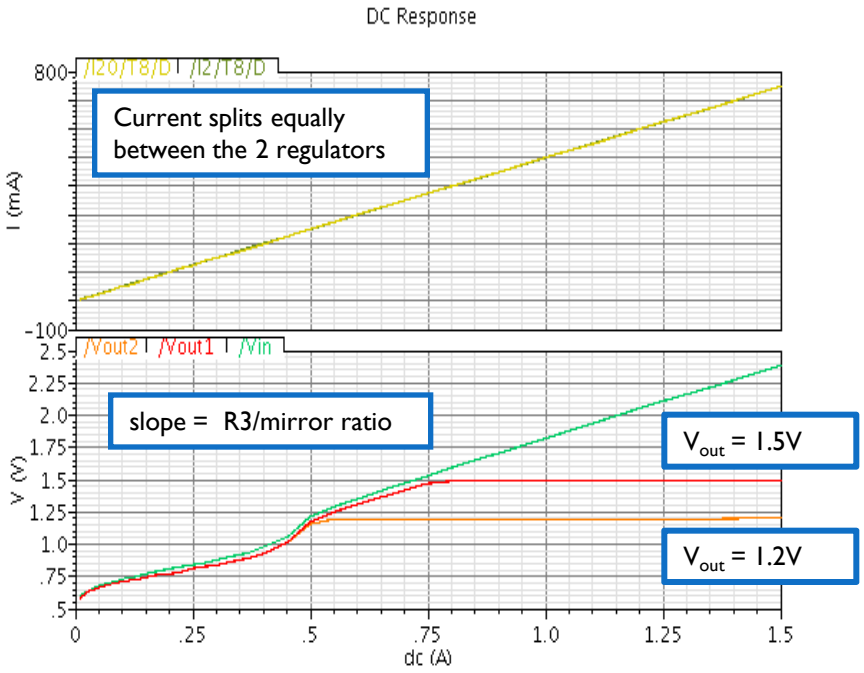
- combination of a LDO and a shunt transistor
  - R_{slope} of the shunt is replaced by the LDO power transistor
  - shunt transistor is part of the LDO load
- shunt regulation circuitry ensures constant I_{load}
  - I_{ref} set by R3, depends on V_{in} ($\rightarrow I_{in}$)
  - I_{M1} mirrored and drained in M5
  - I_{M1} and I_{ref} compared in A3
  - M4 shunts the current not drawn by the load
- LDO regulation loop sets constant output voltage V_{out}
  - LDO compensates output potential difference



ShuntLDO : Features

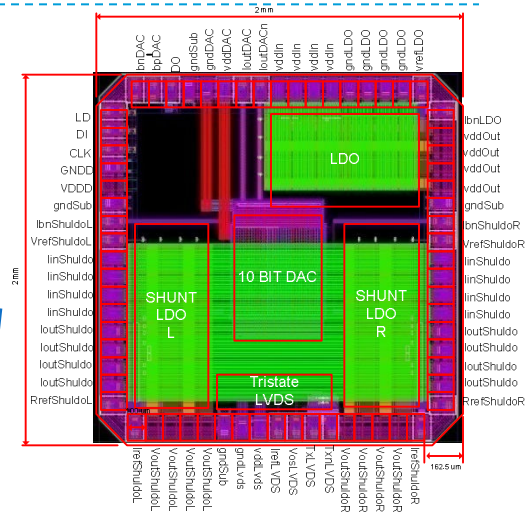
- ShuntLDO regulators having different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
  - resistor R3 mismatch will lead to some variation of shunt current (10-20%) but will not destroy the regulator
- ShuntLDO can cope with an increased supply current if one FE-I4 does not contribute to the regulation e.g. disconnected wire bond
  - I_{shunt} will increase
- can be used as an ordinary LDO when shunt is disabled

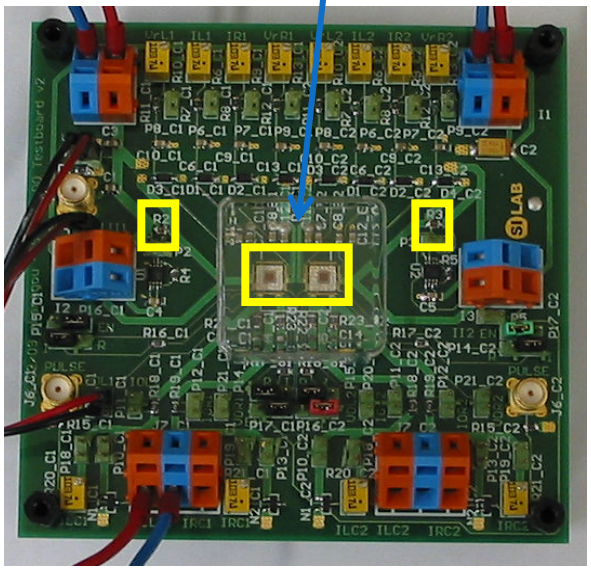
Parallel placed regulators with different output voltages
- simulation results -



ShuntLDO : Prototypes and Test System

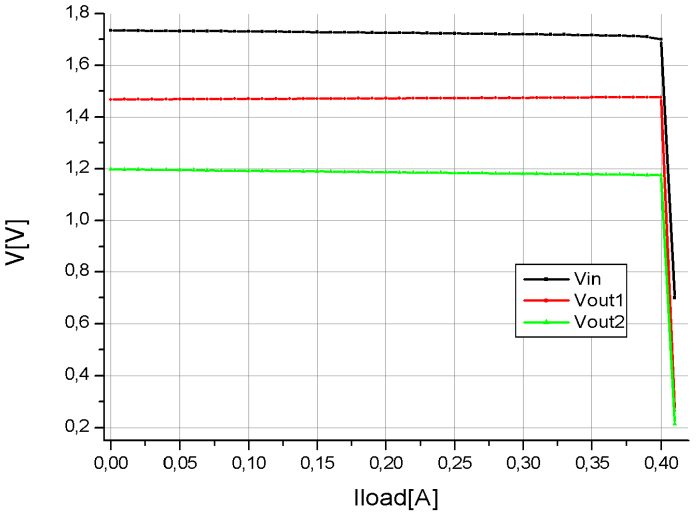
- 2 prototypes submitted and tested
  - September 2008, March 2009
  - V_{out} = 1.2-1.5V, $V_{dropout}$MIN = 200mV, I_{shunt}MAX = 0.5A, R_{in} = 4Ω, R_{out} = 30mΩ
- test setup
  - two ShuntLDO regulators connected in parallel on the PCB
  - biasing & reference voltage is provided externally
  - input & load current is provided by programmable Keithley sourcemeter
  - input & output voltages are measured automatically using a Labview based system
  - shunt current is measured by 10mΩ series resistors and instrumentation opamp



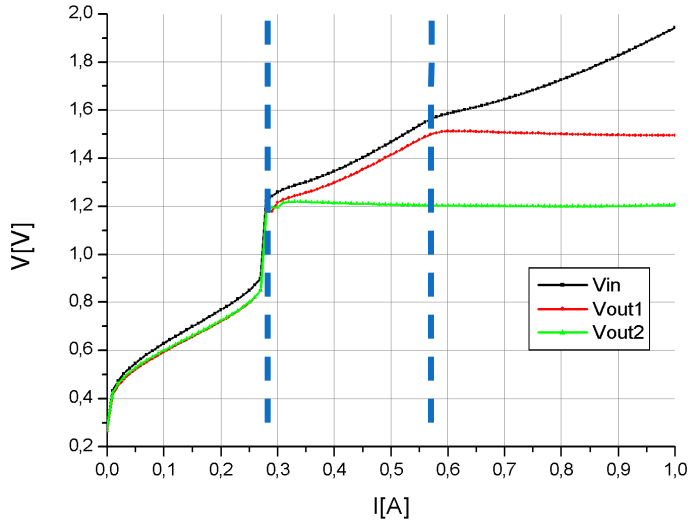


2 ShuntLDO in Parallel

- Load Regulation Measurement
  - 1.5(1.2)V output sees fix I_{load} = 0.4A
  - 1.2(1.5)V output has variable I_{load}
  - V_{in} and V_{out} collapse when the overall I_{load} reaches I_{supply} (= 0.8A)
  - effective output impedance R = 60mΩ (incl. wire bonds and PCB traces)



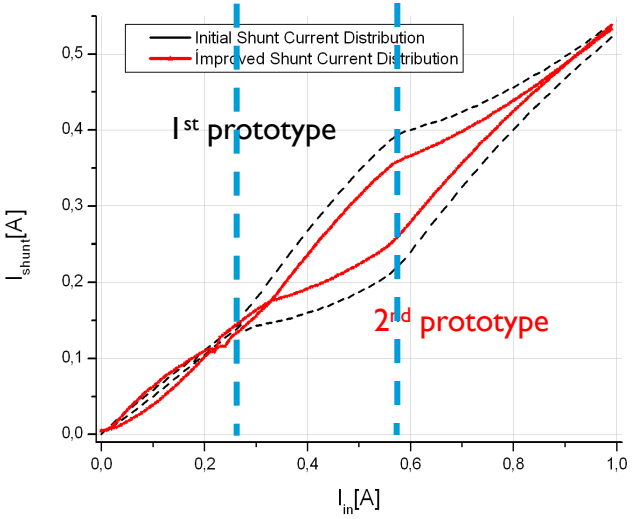
- Generation of different V_{out}
  - V_{out} settles at different potentials
  - V_{out1} and V_{out2} slightly decrease with rising input current (V drop on ground rails leads to smaller effective reference voltages)
  - non constant slope of V_{in}
  - R_{in} ≈ 2Ω (after saturation)



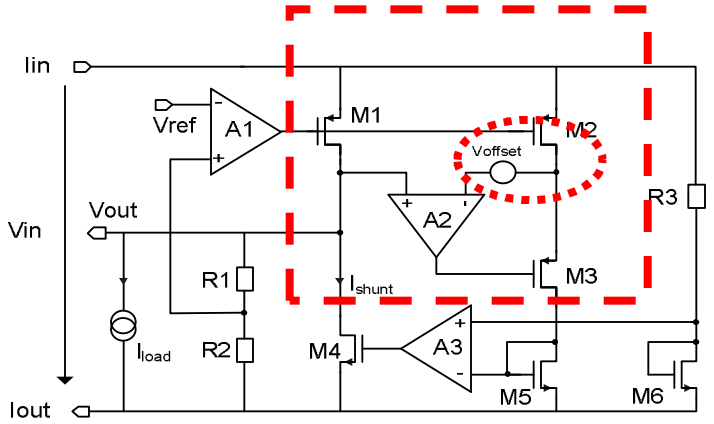
Shunt Current Distribution at Start-Up

- unbalanced I_{shunt} distribution at start-up
  - more I_{shunt} flows to the regulator which saturates first (i.e. to the regulator with lower V_{out})
  - however I_{shunt}MAX is not exceed
- improvement of shunt distribution as soon as both transistors are saturated
- non - constant slope of V_{in} closely related to I_{shunt} distribution

2 SHULDOs in parallel with different V_{out}



- bad mirroring accuracy for non saturated transistors due to offset at the input of A2
  - wrong current is compared to the reference
- hypothesis confirmed by simulations and second prototype
  - scaling of input transistor of A2 by factor 4 halves the unbalance

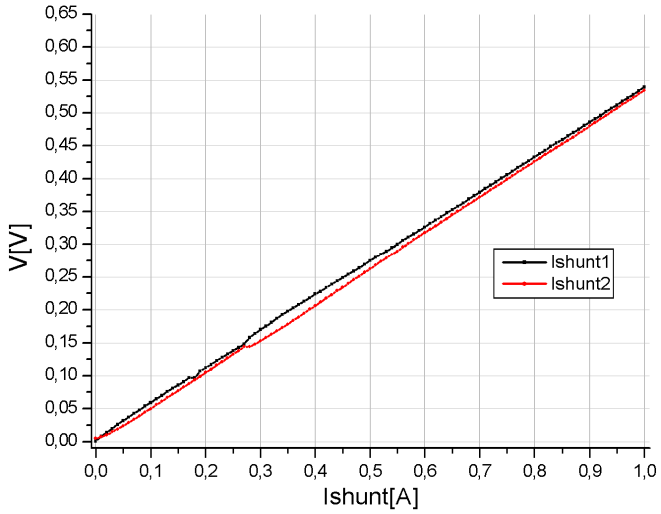


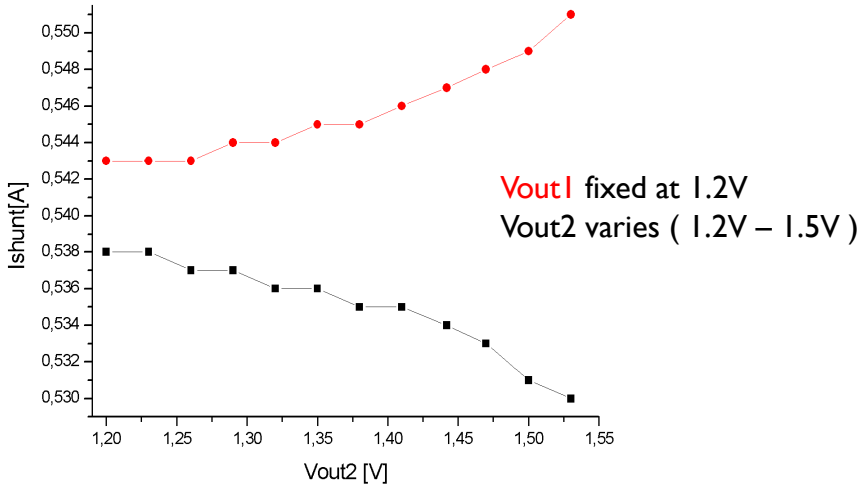
Shunt Current Distribution

- no problem at start-up if the 2 ShuntLDOs generate the same V_{out}
  - they saturate at the same time
- if V_{out} is changed with both regulators being saturated the shunt current changes of about 1.4%

→ Unbalanced I_{shunt} at start-up can be avoided completely by choosing the same V_{out} at start-up and setting different V_{out} afterwards

2 ShuntLDOs in parallel with same V_{out} at start-up

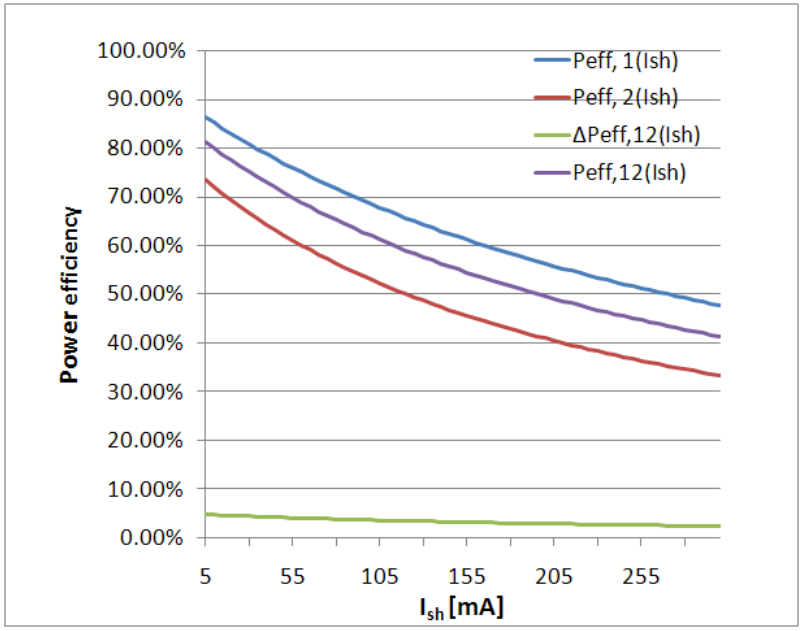




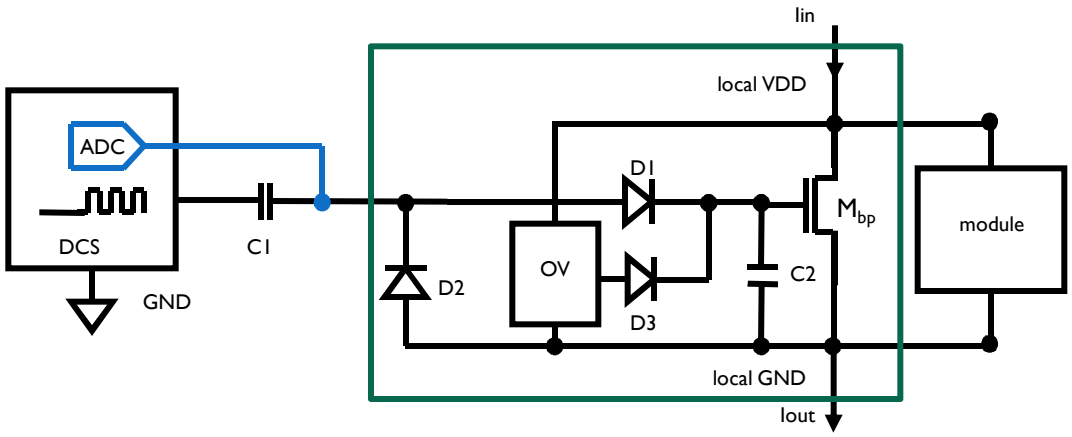
ShuntLDO Efficiency

- Crucial point for SP is the power efficiency of the power converter
- 3 possible sources of inefficiency for the ShuntLDO
  - Dropout voltage V_{drop}
  - Shunt current I_{shunt}
  - ΔV between the 2 V_{out} needed by the FE
- Calculation for ATLAS Pixels

	nominal	worst case	best
V_{out1} [V]	1.4	1.4	1.4
V_{out2} [V]	1.2	1.2	1.2
I_{out1} [A]	0.36	0.4	0.36
I_{out2} [A]	0.24	0.27	0.24
V_{drop} [V]	0.2	0.2	0.1
I_{shunt}[A]	0.03	0.05	0.01
ΔU [V]	0.2	0.3	0.2
I_{TOT} [A]	0.6	0.67	0.6
P_eff, 1	80.77%	77.78%	90.81%
P_eff, 2	66.67%	59.56%	76.80%
P_eff, 1-2	79.55%	76.14%	90.32%
ΔP_eff,1-2	4.55%	6.57%	5.16%
P_eff,1-2g	75.00%	69.56%	85.16%



Module Protection Chip

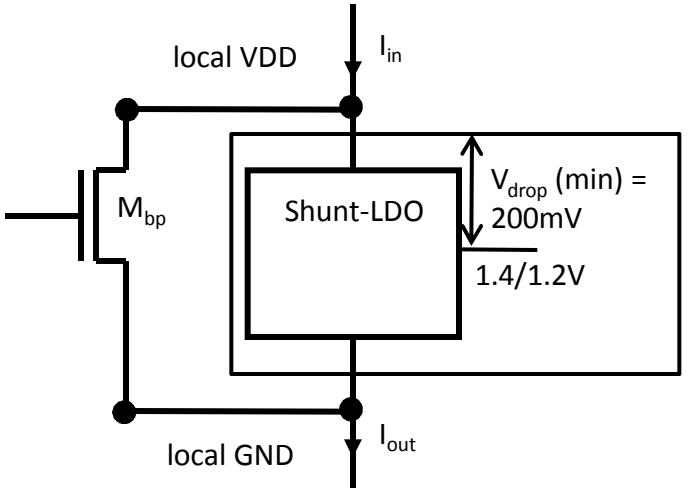


- 130nm CMOS technology
- Bypass transistor
- AC-coupled slow control line
  - can be used to monitor V_{mod} when idle
- Independent over voltage protection circuitry
- Specs for 4-chip FE-I4 module(*)
  - I_{nom} = 2.4A, I_{MAX} = 3.5A
  - AC-signal frequency = 100k – 1MHz
  - AC-signal amplitude = V_{gs} bypass
  - OV protection threshold: V_{thMIN} = 2V – V_{thMAX} = 2.5V
  - OV protection time response = 100ns

(*) preliminary

Bypass Transistor

- I = 3.5A, V ≥ 1.6V (max 2.5V)
  → DG NMOS
- Radiation hardness
  - ELT to cut leakage current path
  - Positive V_{th} shift at TID ≥ 1Mrad
    - Account for ΔV_{th} = 200mV in simulations
- Operational temperature
  - Not yet defined, will depend on the sensor
  - Simulations with T = (-27 ÷ +27)°C
- Low power consumption when on
- Process Corners
  → W = 48mm, L = 0.24µm

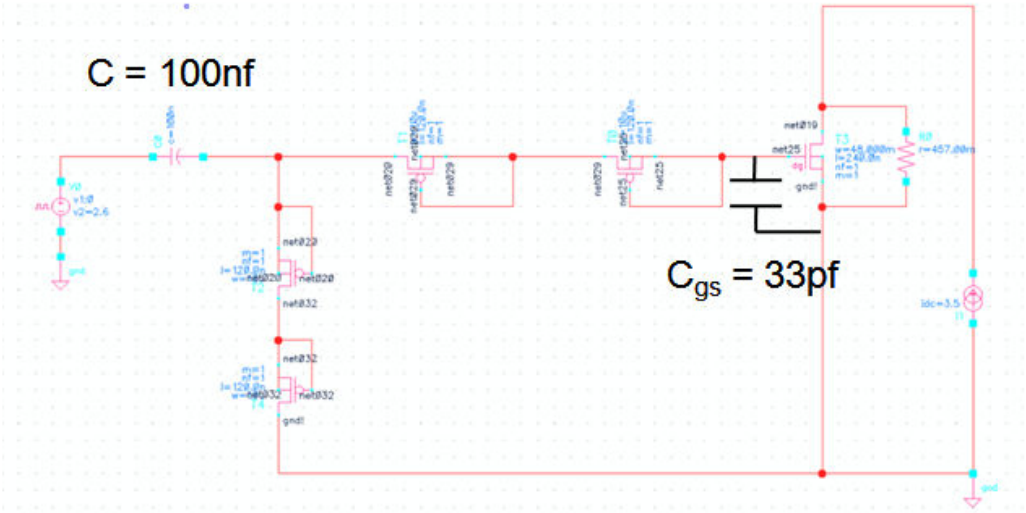


- Power consumption (worst case)
  - Bypass on → 335.1mW
  - Bypass off → 25µW

Control Line

- Rectifier
  - In a diode connected MOSFET $V_{ds} = V_{gs} \approx V_{th}$
  - To increase the power conversion efficiency
    - $V_{sb} < 0$ when diode is forward biased → V_{th} smaller → V_{ds} smaller
    - $V_{sb} > 0$ when diode is reversed biased → V_{th} higher → smaller leakage current

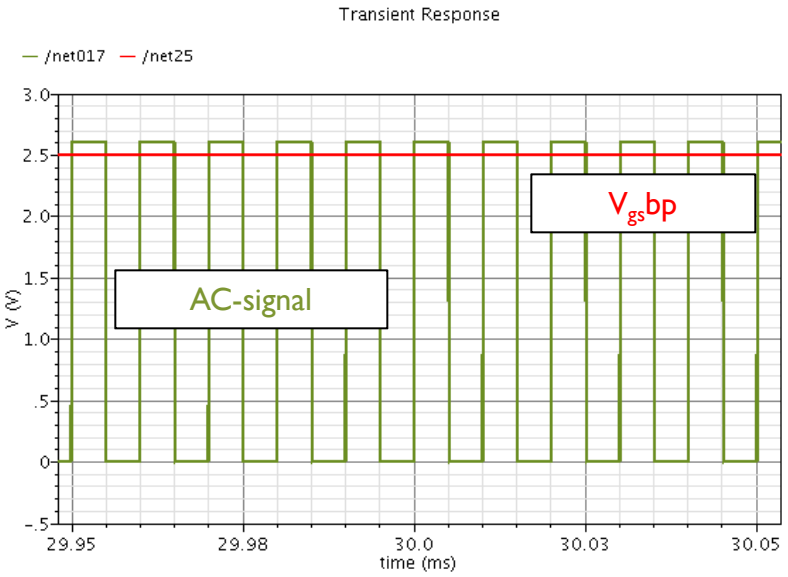
    → use PMOS or triple well NMOS (allow to connect bulk in the "forward direction")
  - Thin oxide transistor
    - W = 10µm for radiation hardness
    - 2 PMOS in series to avoid gate oxide breakdown (AC-signal amplitude > 2.5V)

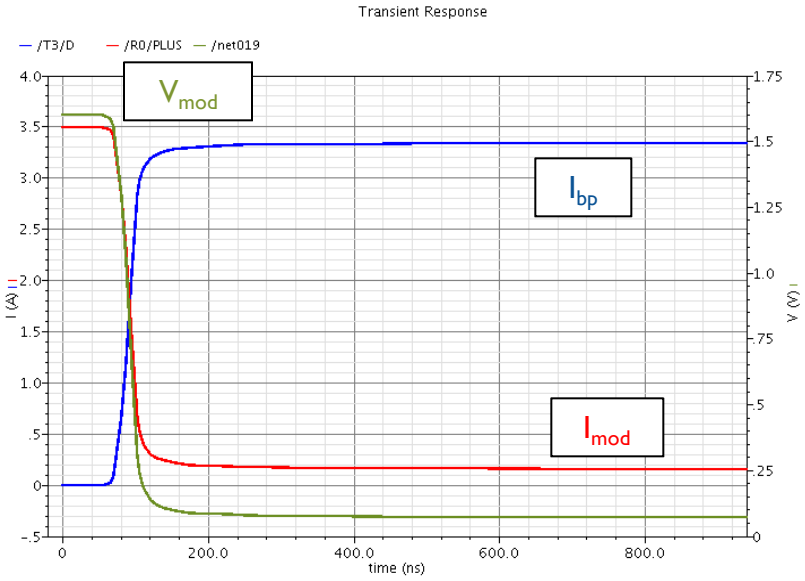


Control Line: Simulation Results

- AC-signal: 2.6V, f = 100k – 1MHz
  - V_{gs} bypass: 2.5V
  - V_{mod}: 1.6V → ~60mV
  - I_{mod}: 3.5A → ~100mA

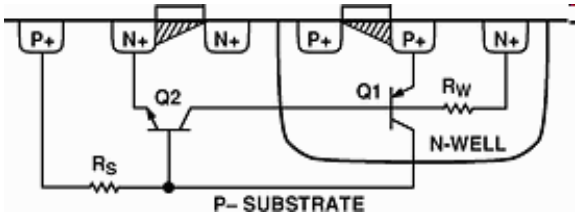
  → Control from DCS works fine

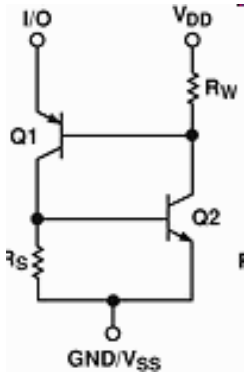




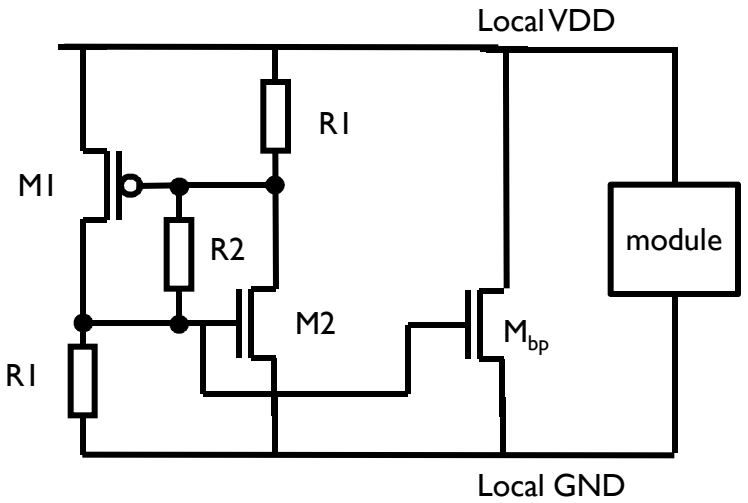
Over-Voltage Protection

- Silicon Controlled Rectifier
  - Parasitic elements (BJTs) in CMOS technologies (inverter in IO pads)
  - Latch-up condition: I/O voltage (U_E^{Q1}) > VDD
    - Q1 begins to conduct → Q2 switches on → Q1 draws even more current
  - Shorts the supply rails when triggered
  - That is exactly what we want!



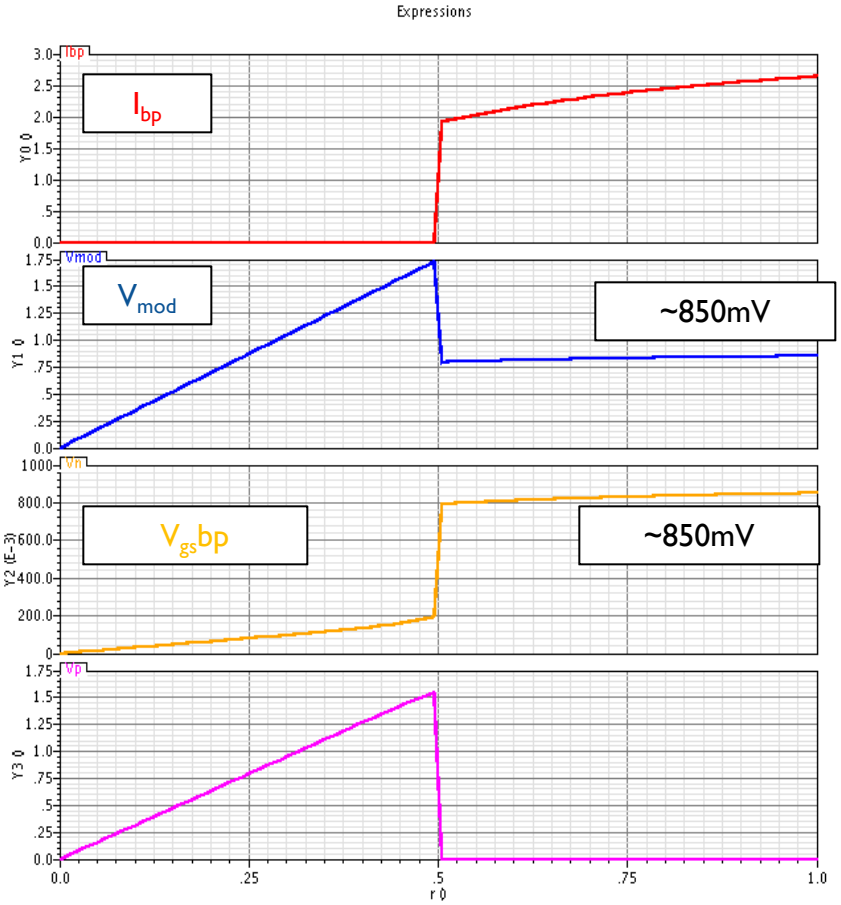


- Use MOSFETS instead of parasitic BJTs for better control of operation parameters
- Trigger threshold defined by R2/R1
- Want to draw high currents
  - R1 small
  - or use additional 'power' NMOS → bypass



SCR: Simulation Results

- Sweep of R_{mod} → V_{mod} increases, I_{mod} constant
- The voltage across the module is effectively clamped down when the SCR activates, however
  - $V_{ds}bp = V_{gs}bp$ → impossible to get V_{mod} = 100mV and $V_{gs}bp$ = 2.5V
  - V_{mod} = 850mV & $I_{bp} \approx$ 3A → too high power density
- A SCR is not the optimal solution for our needs and a different OV protection scheme has to be studied

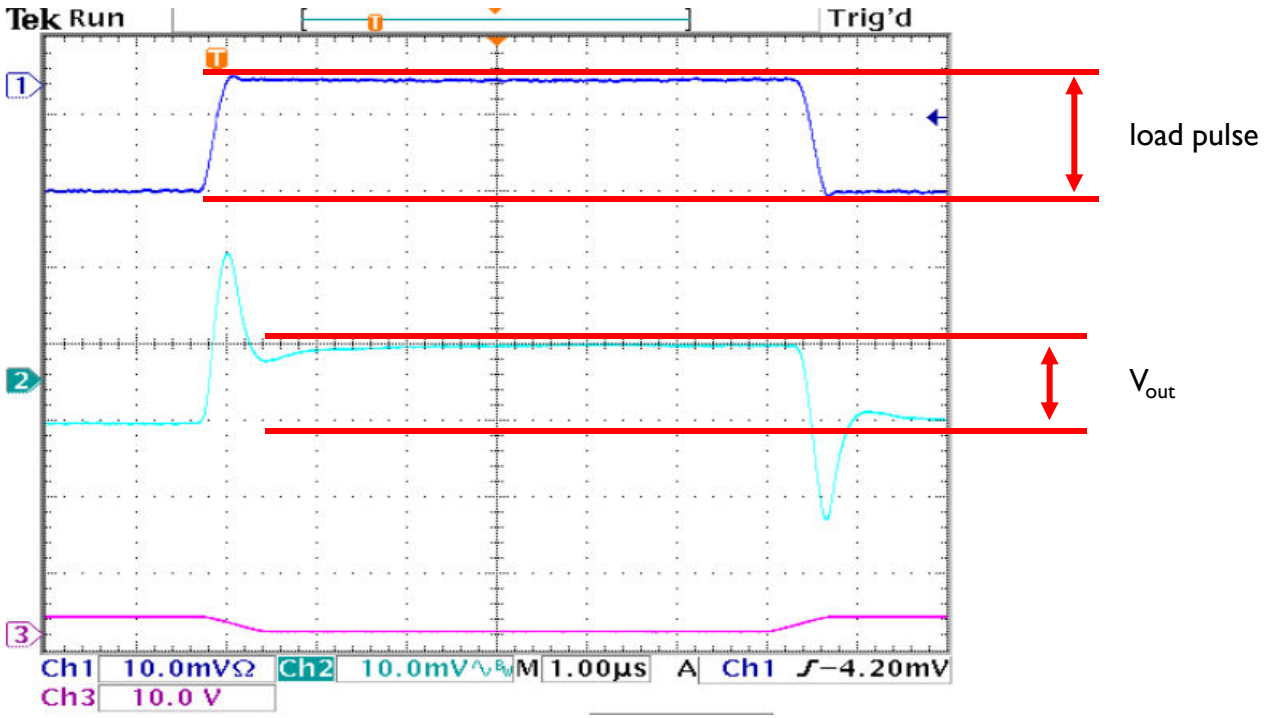


Summary

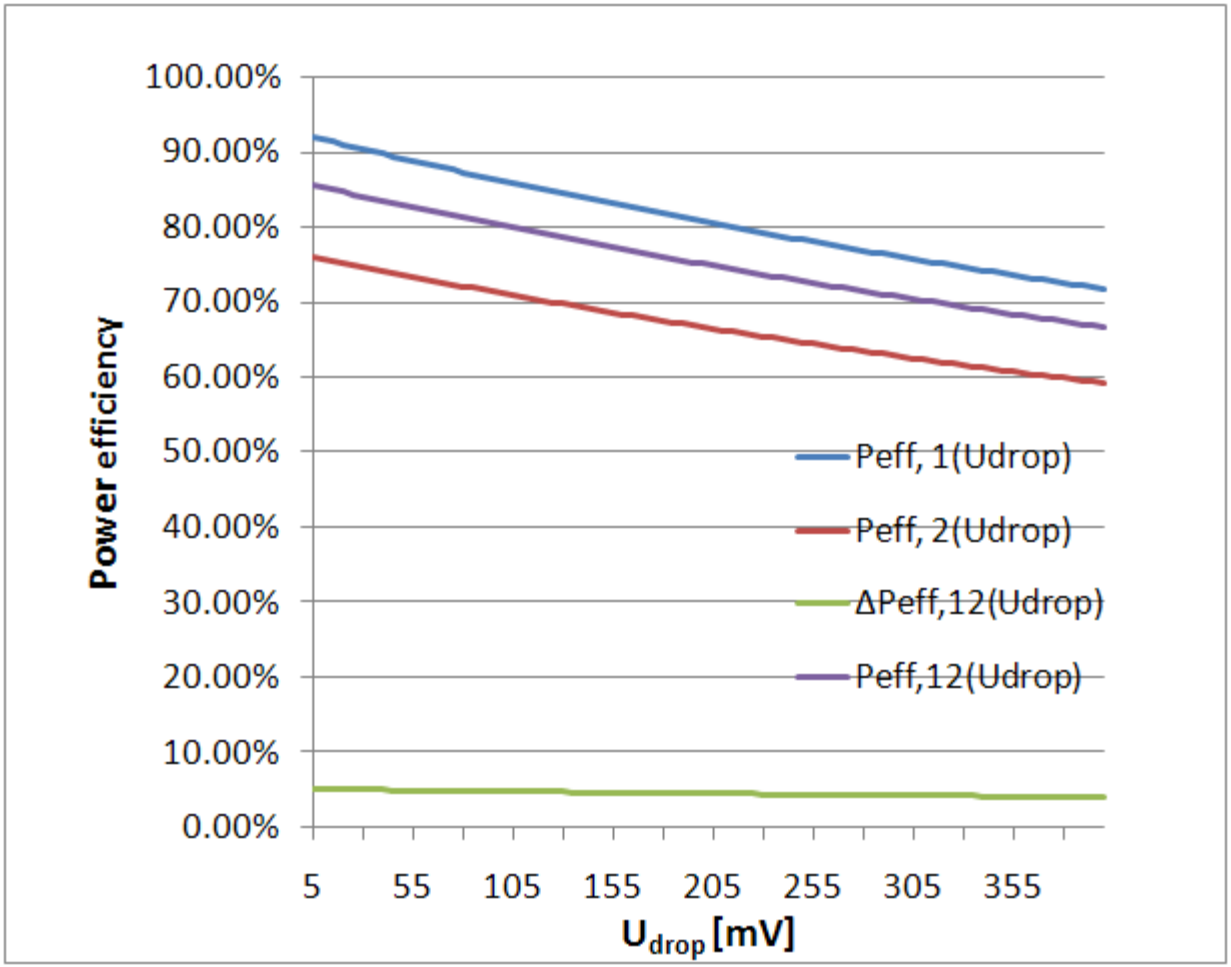
- A stave emulator has been developed which allows study of system aspects related to serial powering
  - A baseline design has been set up and the FE-I4 LVDS transceiver has been tested, as well as some DCS functionalities
  - A serial powered emulator stave is under development to study ShuntLDO performance and AC-coupled data transmission
- Characterization of the ShuntLDO has been performed on single devices, with nominal current and voltage values
  - Results show that the ShuntLDO performs according to specifications with a nominal power efficiency of 75%
  - Problems with shunt current distribution have been understood and corrected in next version
- Work is ongoing on the Module Protection Chip

SHULDO: Load Transient Behavior

- I_{load} pulse of 150mA (15mV measured across 100mΩ)
- 10mV output voltage change



SHULDO Efficiency



SHULDO Efficiency