Status of WP8

Tracking detector power distribution

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5 Feb 2010

**SLHC-PP Annual Meeting
4-5 February 2009**

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Outline

**SLHC-PP Annual Meeting
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Overview of WP8

Progress on DC-DC converters

DC-DC option for CMS strip tracker

Serial powering for ATLAS pixel tracker

Serial powering for ATLAS strip tracker

Summary

WP8 Collaboration

Participants:

AGH-UST Krakow

CERN

PSI

RWTH Aachen

STFC-RAL

Universität Bonn

Material for the report delivered by:

Georges Blanche (CERN)

Lutz Feld and Katja Klein (RWTH Aachen)

Laura Gonella (Universität Bonn)

Fabian Hügging (Universität Bonn)

Giulio Villani (STFC, RAL)

Tracking detector power distribution

Task 8.1: DC-DC conversion

"Evaluation phase"

An evaluation of different conversion approaches will be made, singling out the critical difficulties and developing conceptual solutions to overcome them. Exploration of partnerships with industry.

"Prototype phase"

Development of prototype converters for the alternative solutions. The on-chip DC-DC converter, integrated in modern CMOS technologies, will also be prototyped to assess the feasibility of this solution. Prototypes will be integrated in detector modules and tested at the system level. A report will detail the performance of the prototypes, with conclusions on the final viability of each conversion approach and recommendation for LHC upgrades.

Task 8.2: Serial Powering

" Generic studies"

Specification and development of AC-coupling or opto-decoupling elements; investigation of grounding and shielding techniques for serial powering schemes; system evaluation of serial powering systems based on commercial shunt regulators.

"Development of custom radiation-hard power electronics"

Design, submission and characterization of custom radiation-hard shunt regulators, power devices and AC–coupling circuitry. Several design iterations in different technologies are foreseen. The concept of a generic high-current serial powering ASIC, with various protection and slow-control features, capable of powering S-ATLAS and CMS2 pixel and strip detectors, will be evaluated.

"System design and characterization of super-modules"

Implementation of custom electronics in tracking detector super-modules. A super-module will consist of a significant number of detector modules powered in series. The super-module performance will be fully characterized.

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Deliverables

SLHC-PP
Project number 212114
Date: February 1st 2008

Deliverables task 8.1	Description	Nature	Delivery date
8.1.1	Evaluation report on DC-DC conversion technologies	R	M12
8.1.2	Prototypes and viability report	P, R	M30
8.1.3	Integration in full-scale detector modules	D	M36

Deliverables task 8. 2	Description	Nature	Delivery date
8.2.1	Evaluation report on generic serial powering studies and specification of serial powering components	R	M12
8.2.2	Custom serial powering circuitry and evaluation of generic high-current serial powering ASIC	P,R	M24
8.2.3	Full-scale super-module with custom serial powering circuitry	D	M36

Why powering becomes a problem?

ATLAS Inner Det. Cables

ATLAS pixel detector services
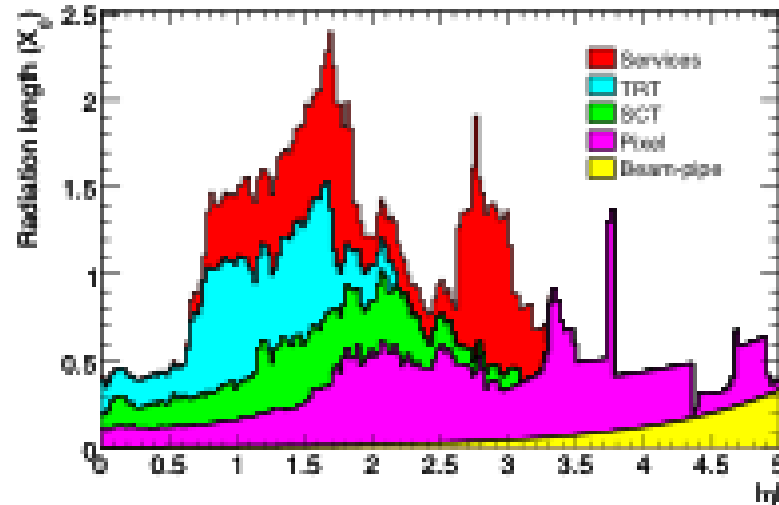
ATLAS Inner Det. Material Distribution

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SLHC-PP WP8

Status of DC/DC Converters Developments at CERN

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DC/DC Developments at CERN

CERN is involved in the development of radiation and magnetic field tolerant DC/DC converters for the Trackers Upgrade at SLHC.

➢ Last year we reported that:
- Several DC/DC topologies were studied.
- A powering scheme was proposed, using a Buck DC/DC topology combined with Switched Capacitors embedded in the front-end chips.

➢ In 2009 important milestones have been achieved:
- Radiation tolerant ASIC technologies were selected.
- Several prototypes were built and tested.
- Air-core inductors were developed and tested.
- System tests were carried out to investigate the compatibility between front-end modules and DC/DC prototypes.

ASIC Technology

Five technologies were characterized for their radiation tolerance up to levels required at SLHC Trackers: · up to 250Mrad in Total Ionizing Doze (TID) and 2.5 10^{15} n/cm^2 (1MeV neutron equivalent) for Displacement Damage.

Technology	Tech. node	Transistor type	Max Vds [V]	Max Vgs [V]	Before Irradiation R_{on} [kΩ·µm]	Displacement Damage R_{on} @ 5·10^{15} p$^+$/cm^2 [kΩ·µm]	Total Ionizing Dose R_{on} @ 100 Mrad [kΩ·µm]
A	0.35µm	Vertical N	80	3.3	16.9	>1000	17
		LDMOS N	14	3.3	7.1	10.5	7.5
		LDMOS P	80	3.3	41.3	66.4	50
B	0.25µm	LDMOS N	22	2.5	4.1	6.5	4.8
		LDMOS P	16	2.5	12.2	21.1	15.3
C	0.18µm	LDMOS N	20	5.5	4.1	14.7	4.7
		LDMOS P	20	5.5	11.2	140.9	47.7
D	0.18µm	LDMOS N	20	1.8	11.4	992	14
		LDMOS P	20	1.8	26	298	33
		LDMOS N	50	1.8	23.5	>1000	N.A.
		LDMOS P	50	1.8	40.1	446	N.A.
		LDMOS N	25	5	13.1	N.A.	20
		LDMOS P	25	5	25.5	N.A.	39
E	0.13µm	LDMOS N	20	4.5	7.1	49.6	10.7
		LDMOS P	20	4.5	17.4	177.2	28.7
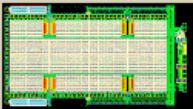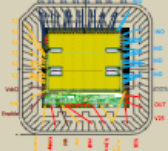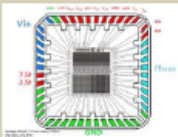
Technology B (IHP 0.25µm) was selected as first choice for its good performance up to the required doses for both P and N type transistors.

Technology A (AMIS 0.35µm) was selected as backup technology for the good tolerance of its N type transistors.

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ASIC Prototypes

Prototype	AMIS1	AMIS2	IHP1
ASIC			
Techno	AMIS 0.35	AMIS 0.35	IHP 0.25
Package	QFN48	QFN48 QFN32	QFN48 QFN32
PCB			
Vin	3.3V to 15V	3.3V-12V	2.5V to 12V
Vout	Programmable	Presets at 1.2/1.8/2.5/3/5V	Programmable
Iout	2A	3A	3A
Fsw	1 MHz	1 MHz	2.0 MHz
Efficiency	< 80%	82%	87%
Gate Delay	Fixed	Programmable	Adaptative
Comment	First Prototype. Required an external sawtooth generator and regulators.	Second Prototype. Programmable gate delay improves efficiency. Sawtooth generator integrated, still requires external regulator.	Third Prototype. Adaptative gate delay further improves efficiency.

3 ASIC Prototypes were produced:

<u>AMIS Technology:</u>

- First sample with core DC/DC functions.
- Second sample, now fully functionnal.

<u>IHP technology:</u>

- Fully functional DCDC.

Regulators for control circuitry are still external: they will be integrated in the next IHP sample (in production).

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AMIS2 Performance
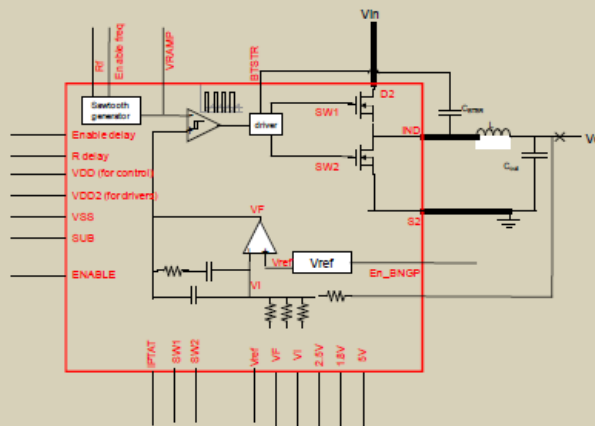
Vout=2.5V L=538nH
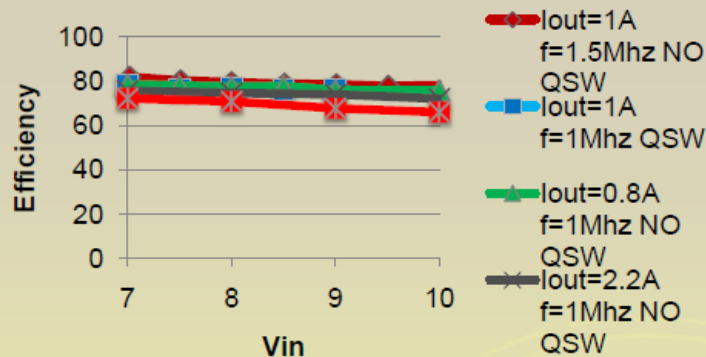
- Irradiation (TID test) has been performed with X-rays on AMIS2 DCDC board biased in working conditions.
- Efficiency drop correlates well with leakage current of LDMOS transistors. This effect is moderated when irradiation is performed at lower dose rate (such as in the real application)
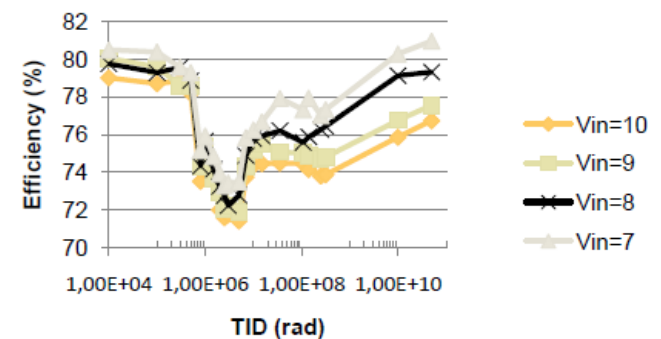
IHP1 Performance

➤ Estimation of losses:
  - Estimated losses match measured losses.
  - IHP1 prototype tuned for 2.5V output at 2A reaches an efficiency of 84%.

➤ Regulation properties:
  - Both line and load regulation characteristics are very good: better than 15 mV output volatge variation within the whole range of Vin and Iout explored.

➤ Operating range:
  - The converter operates in stable conditions over a wide range of input voltage (5V to 11V), output voltage (tested from 0.9V to 3.3V) and output current (tested up to 3.0A).

Best efficiency at 2A, Vin=10V

Line regulation for Vin=10V, f=1.73MHz, L=460nH
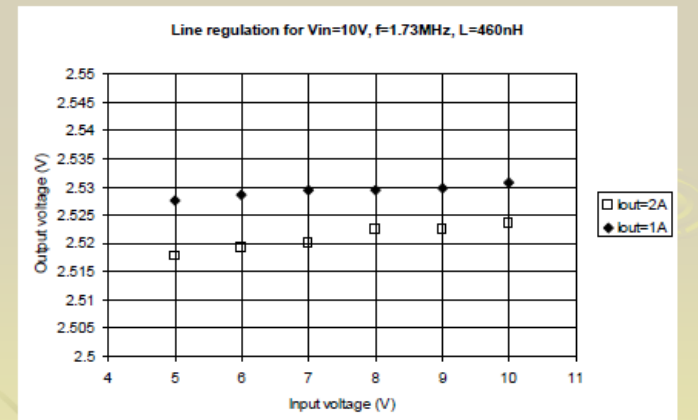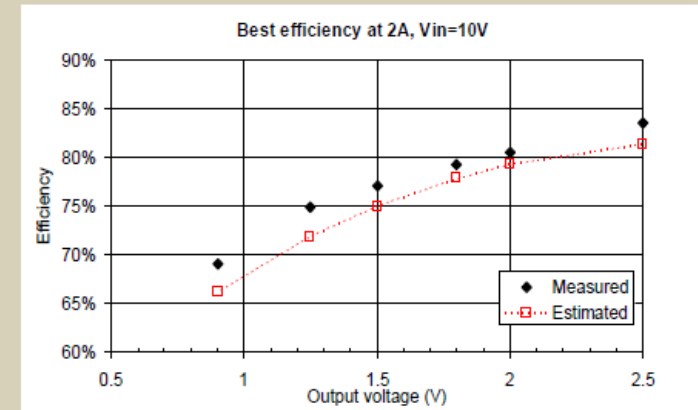
Inductors

➤ **Tolerance to B field for SST imposes air core coils.**
- Air core typical inductance values: 500 nH MAX, currently using 200 nH.
- Low inductance value compensated with high switch frequencies.
- Air core coils are larger than equivalent coils that use magnetic cores.
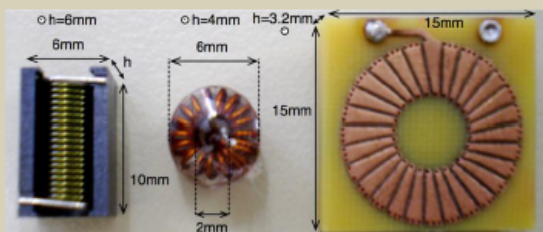
The field radiated by various air core coils was measured and was compared with the field emitted by a shorted wire.

The toroidal structure is best for reducing the emission of field; it also enables shielding. The best performance is found with a shielded PCB toroid.

The wounded toroid seems a good compromise in terms of size, emitted field and manufacturability.
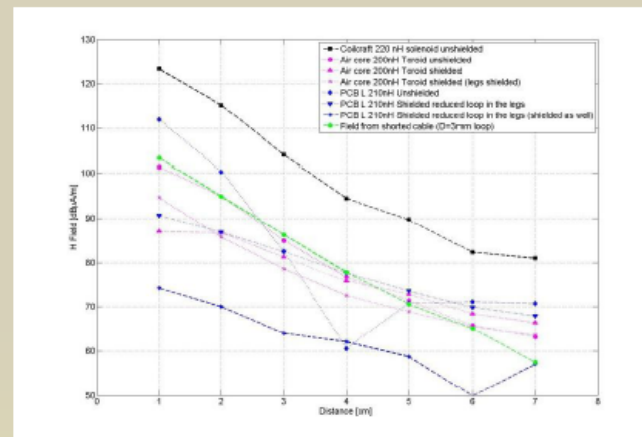
Task 8.1: DC-DC conversion

System tests

Tracker modules have been powered successfully with DCDC prototypes.

➢ Emission of noise of DCDC :
- Noise measured in lab.
- Conducted noise strongly reduced now.
- DCDC emits E and H fields, that have been reduced but are still present.

Proto2 *Proto5*

Reduction of conducted noise.
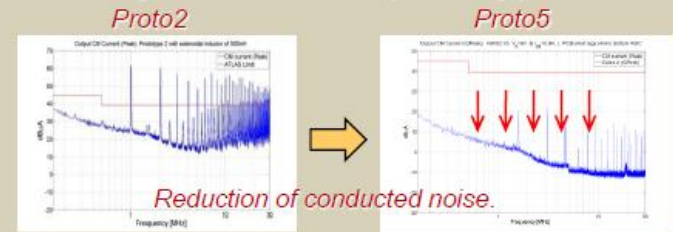
➢ Susceptibility of hybrids
- Susceptibility measured at Liverpool hybrids setup.
- Hybrids were found to be sensitive to E and H fields, not sensitive to conducted noise.
- Shielding of DCDC will be required.
  - Thin foils are sufficient to limit the coupling.
- Susceptibility bandwidth characterized.

Shield

ENC>1000 *ENC<700*
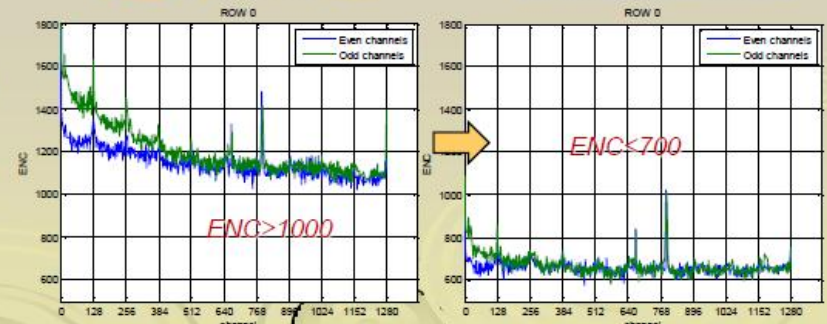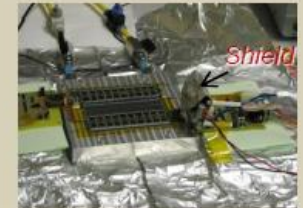
Reduction of E/H field couplings with thin foil shield

Next Steps

Technology issues are now cleared, and the coupling between the hybrid front-end and the DC/DC converter is now understood: system integration issues can now be addressed.

➢ <u>IHP2 prototype:</u> fully integrated features, in production now.

➢ <u>Reduction of board size using IHP2</u>:
- ASIC package size reduction: alternatives to QFN32 under study.
- Integration of reference voltage and control circuit regulators will clear board space.
- Miniature power connector to be used.
- Final prototype will be smaller than the actual AMIS2 board (18x25 mm2).

➢ <u>Control of noise</u>:
- Shield cover is under development.

➢ <u>Cooling:</u>
- A thermal interface will be provided on next prototypes.

DC-DC Conversion Powering for the CMS Tracker at SLHC

Lutz Feld, Rüdiger Jussen, Waclaw Karpinski,
Katja Klein, Jennifer Merz, Jan Sammet
(RWTH Aachen University)

SLHC-PP Annual Meeting

Madrid, 4./5. 2. 2010

Strategy

- **P=U·I =(nU)·(I/n)**
  → supply power at higher voltage i.e. lower current
  → cable loss $P_{loss}=R\cdot I^2$ is reduced by factor n^2!

- two schemes: **DC-DC Conversion** and **Serial Powering**

- CMS task force recommended in early 2009 DC-DC conversion:
  - while both schemes seemed feasible, a DC-DC conversion system is simpler, closer to the current system, with less interdependencies
  - serial powering should be kept as a back-up

- DC-DC "buck" converters switch current at ~MHz, store energy in inductor, regulate voltage via pulse width modulation

- challenges with DC-DC conversion:
  - switching noise of converters could be conducted and/or radiated into detector modules
  - air core inductors required due to 4 Tesla field
  - radiation hard ASIC needs to switch rather high voltages (~10V)
  - useful only if efficiency is high (~80%)
  - total material budget should be reduced by addition of converters

12mm
19mm
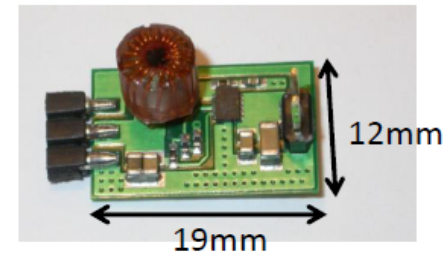
Task 8.1: DC-DC conversion

Our R&D Program

1. Test set-ups to measure
   - efficiency
   - noise spectra (conductive and radiative)
   - system noise (CMS Tracker End-Cap Petal)
   - conductive and radiative coupling mechanisms
   - magnetic field tolerance
   - thermal performance
   - material budget (simulation)

   done

2. Measurements with commercial converters
   - optimize converter board layout
   - understand noise coupling mechanisms and develop counter-measures
   - develop (non-rad hard) converter prototype which does not introduce significant extra noise

   ~done

3. Development of radiation hard converters
   - in collaboration with CERN (F. Faccio et al.)

   ongoing

4. Application of DC-DC converters in Pixel Upgrade
   - prototyping, system tests and integration studies for phase I upgrade of the Pixel System

   started

Task 8.1: DC-DC conversion

http://cern.ch/SLHC-PP

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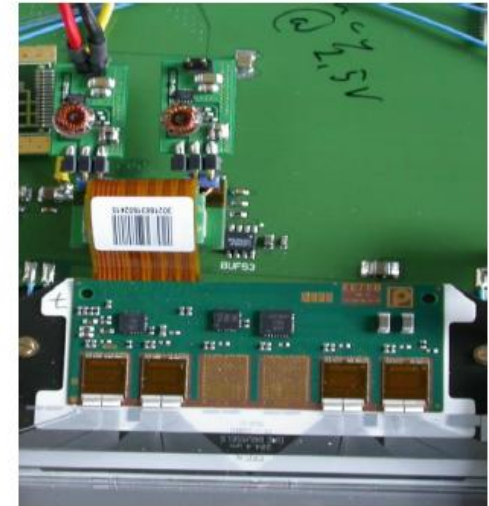
Results with Commercial Converter ASIC

Chip: Enpirion EQ5382D
V_{in} = 2.4-5.5V(rec.)/7.0V(max.)
$I_{out} \leq 0.8A$
$f_s \approx 4MHz$

Air-core inductor:
Custom-made toroid, $\varnothing \approx 6mm$
L = 200nH or 600nH

12mm

19mm
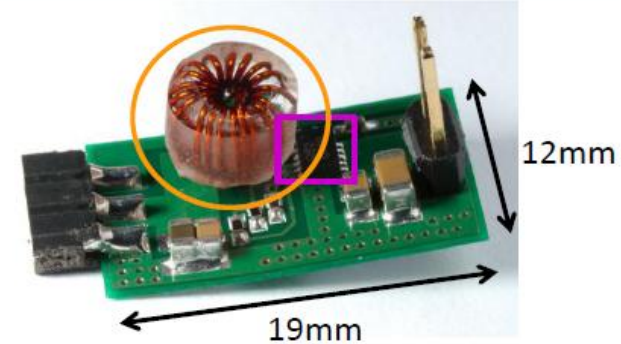
- noise measurement with CMS tracker strip modules

- no excess noise with optimized PCB and pi filter (no shielding)

Commercial converters with air core toroids

1st version

2nd version

2nd version with pi filter

noise level
w/o converter

Noise of edge strips [ADC counts]

Input voltage [V]

Task 8.1: DC-DC conversion

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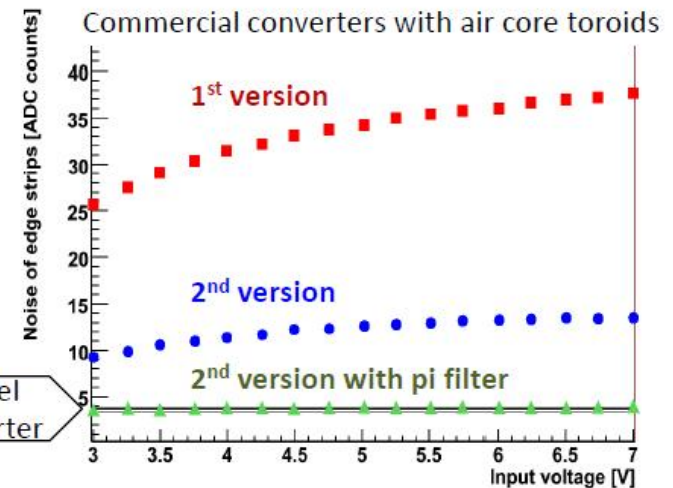
Results with AMIS ASIC

- ASIC developed by CERN group (Faccio et al.) in AMIS I3T80 technology

- when operated under same conditions as commercial ASIC
  - freq=4MHz
  - pi filter (which adds also a ~cm of distance)

  similar noise values are obtained, i.e. no significant extra noise due to the converter

- noise level depends on frequency and conversion ratio

19mm

25mm

Legend:
- No converter
- 10V
- 10V, external pi filter
- 5.5V
- 5.5V, external pi filter

Noise of edge strips [ADC counts]

f = 1MHz   f = 4MHz

Task 8.1: DC-DC conversion

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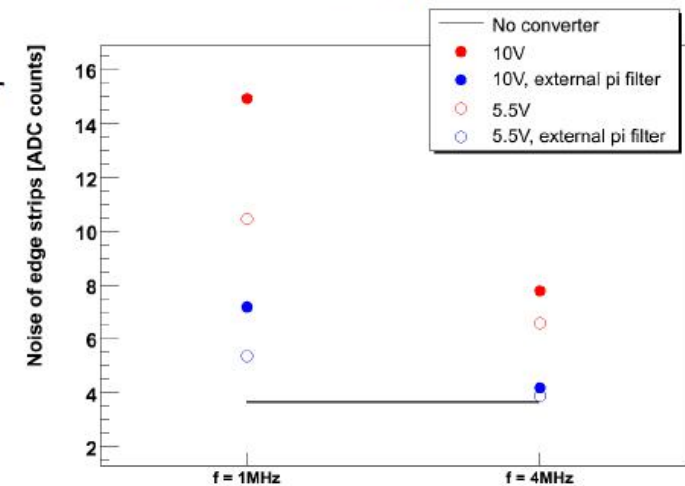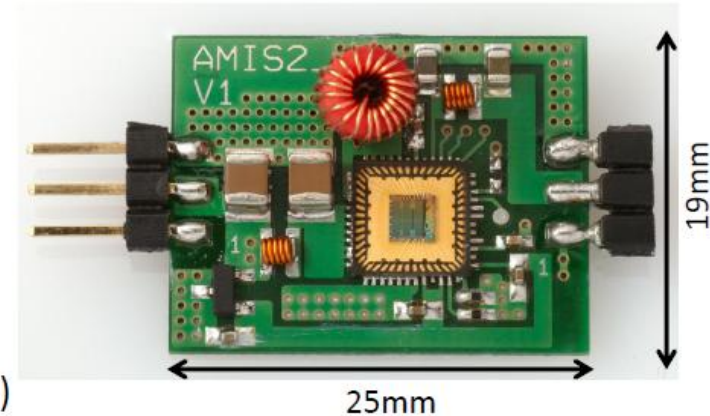
Where are we today?

- non-rad hard converter prototype with commercial components in hand with 75-85% efficiency, I=0.8 A, conversion ration ~4, low mass (~10% of strip module), small size (19x12 mm^2), magnetic field tolerance

- simulations show that total material budget can be reduced in a DC-DC conversion powering scheme (e.g. by 8% for tracker end-cap (as example) in a certain scenario)

- radiative and conductive noise is an issue, but can be controlled by filtering, board design, shielding, distance, conversion ratio, switching frequency

- results of measurements with AMIS ASIC are encouraging

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DC-DC conversion R&D - highlights

ASICs for serial powering schemes Radiation resistant technology identified and proven, new ASIC in production

Design of DC-DC converter stage in 130 nm technology elaborated

Much progress on reducing material budget

Much progress on understanding system noise

Work on integration on detector modules has started

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SI LAB
Silizium Labor Bonn

Serial powering for pixels

<u>F. Hügging</u>, D. Arutinov, M. Barbero, A. Eyring, L. Gonella, M. Karagounis, H. Krüger, N. Wermes

SLHC-PP Annual Meeting,
CIEMAT, Madrid, 04-Feb-2010

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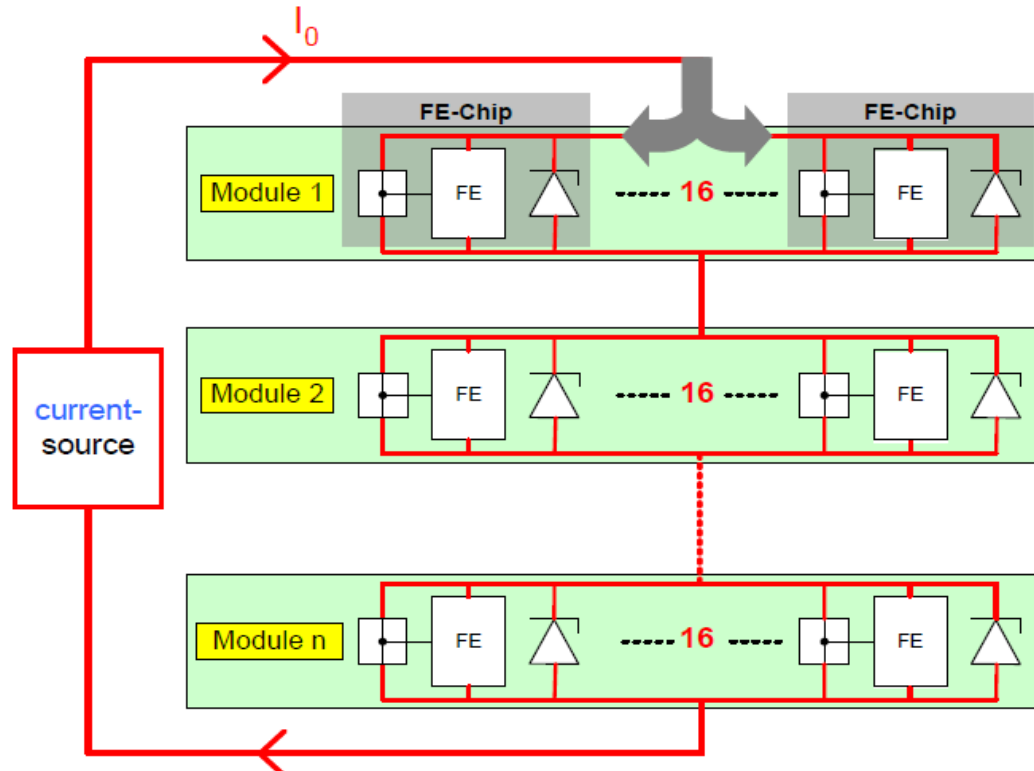
- $V_{mod} = V/n$ with n modules in a chain supplied with constant current I_{mod}.
- Current through cables only $I = I_{mod}$ instead of $I = nI_{mod}$.

→ P_{cable}(serial powering)/P_{cable}(parallel powering) = $R_{cable}I_{mod}^2/R_{cable}(nI_{mod})^2 = 1/n^2$

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Task 8.2: Serial powering

Module electrical Requirements

- FE-I4 power needs:
  - VDA = 1.4V
  - VDD = 1.2V
  - I = 600mA
- voltage regulators to generate a constant voltage out of the current supply.
- integrated regulation circuitry in every FE-I4.
  - avoid additional components on the module.
- 4-chip-module uses 8 regulators in parallel.
  - Redundancy.
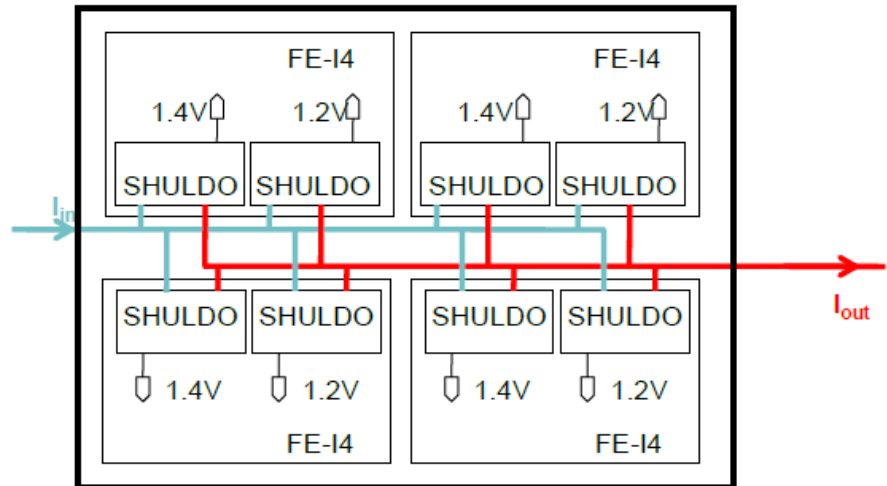
- 2 SHULDOs/FE-I4
  - can operate in parallel and generate 2 different output voltages at the same time

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universität**bonn** **ShuntLDO: Working Principle**

- combination of a LDO and a shunt transistor:
  - R_{slope} of the shunt is replaced by the LDO power transistor.
  - shunt transistor is part of the LDO load.

- shunt regulation circuitry ensures constant I_{load}:
  - I_{ref} set by R3, depends on V_{in} ($\rightarrow I_{in}$).
  - I_{M1} mirrored and drained in M5.
  - I_{M1} and I_{ref} compared in A3.
  - M4 shunts the current not drawn by the load.

- LDO regulation loop sets constant output voltage V_{out}:
  - LDO compensates output potential difference.
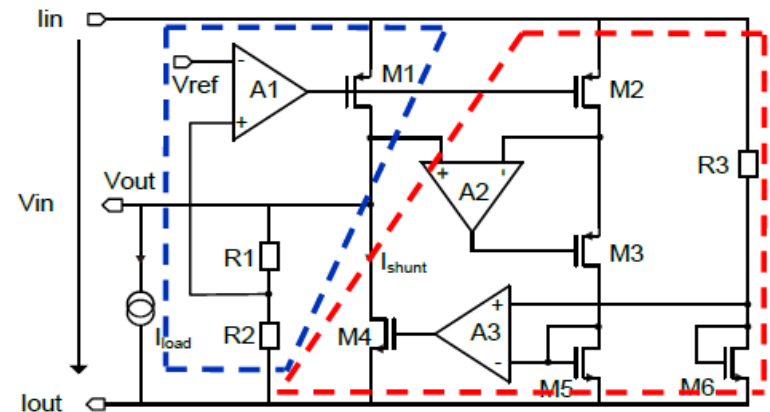
Task 8.2: Serial powering

SHULDO: Prototypes and Test System

- ▶ 2 prototypes submitted and tested
  - ▶ September 2008, March 2009
  - ▶ V_{out} = 1.2-1.5V, $V_{dropout}MIN$ = 200mV, $I_{shunt}MAX$ = 0.5A, R_{in} = 4Ω, R_{out} = 30mΩ

- ▶ test setup
  - ▶ two SHULDO regulators connected in parallel on the PCB
  - ▶ biasing & reference voltage is provided externally
  - ▶ input & load current is provided by programmable Keithley sourcemeter
  - ▶ input & output voltages are measured automatically using a Labview based system
  - ▶ shunt current is measured by 10mΩ series resistors and instrumentation opamp

▶ 8

L. Gonella - ATLAS Upgrade Week - Nov. 2009
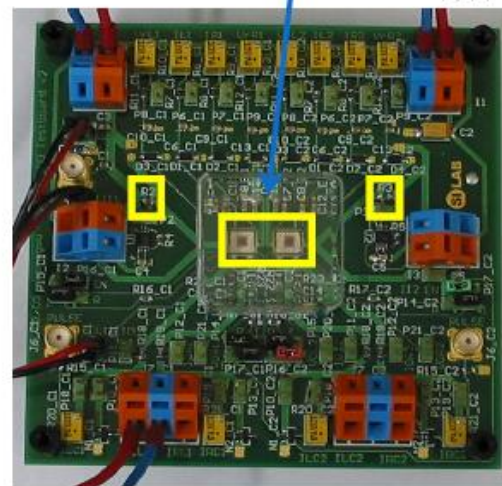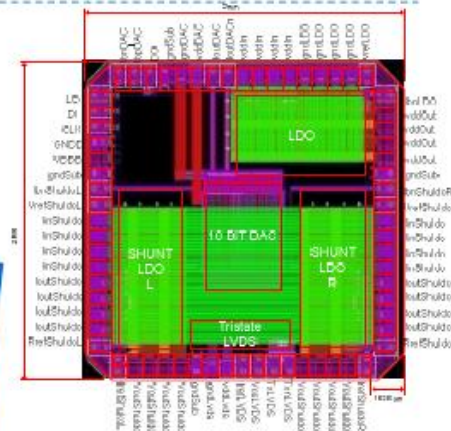
ShuntLDO: Features

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- ShuntLDO regulators having different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution.
  - resistor R3 mismatch will lead to some variation of shunt current (10-20%) but will not destroy the regulator.
- ShuntLDO can cope with an increased supply current if one FE-I4 does not contribute to the regulation e.g. disconnected wire bond.
  - I_{shunt} will increase
- can be used as an ordinary LDO when shunt is disabled.
- test results and more details: see L. Gonella's talk.

Parallel placed regulators with different output voltages
- simulation results -

DC Response

Current splits equally between the 2 regulators

slope = R3/mirror ratio

V_{out} = 1.5V

V_{out} = 1.2V

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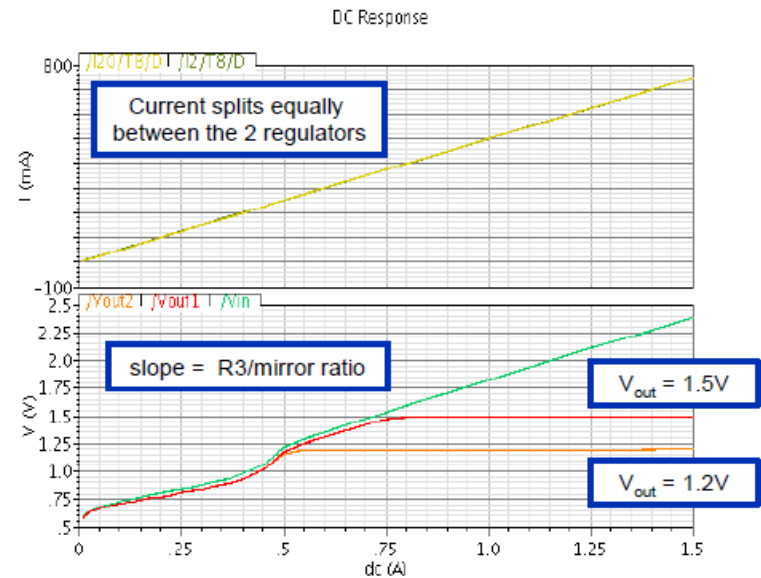
universität**bonn** # Power Efficiency

- Crucial point for SP is the power efficiency of the power converter.
- For the ShuntLDO 3 sources of inefficiency:
  - Dropout voltage V_{drop}
  - Shunt current I_{shunt}
  - Difference between the 2 output voltages ΔV needed by the FE.
- Calculations with conservative assumptions for ATLAS Pixel:
  - V_{drop}= 200mV, I_{shunt}= 30mA, ΔV= 200mV
  - Total current of the FE is 600mA with 250mV for the digital part at the lower output voltage of 1.2V.
- Power efficiency for single ShuntLDO is around 80% at realistic currents.
- Power efficiency for parallel operation of 2 ShuntLDOs at 1.2 and 1.4V is ~75%.

Power Efficiency of 2 parallel ShuntLDOs

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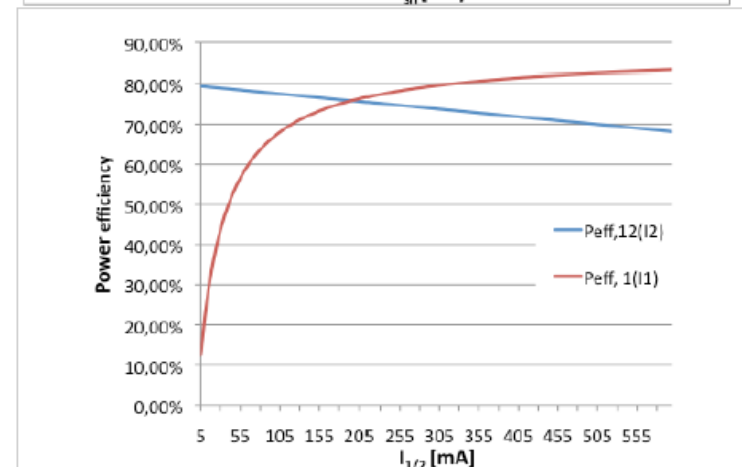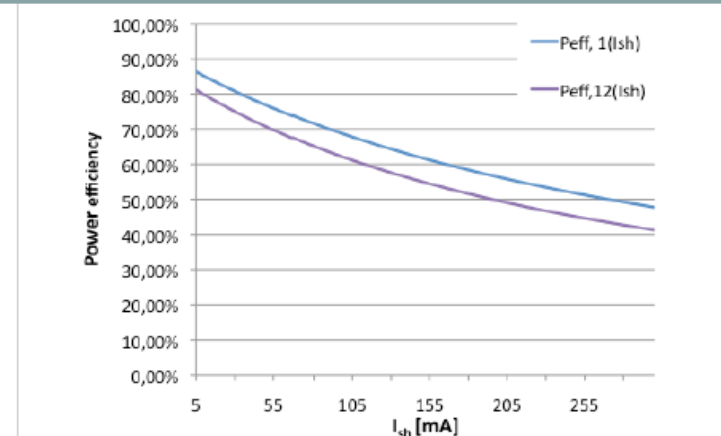
universität**bonn** Protection for Serially Powered Staves

- Purpose:
  - Assure supply of power to the serially powered chain in case of failures.
    - Broken wire bonds, overvoltage.
  - Allow power to arbitrary selection of modules.
    - Switch off a noisy module.
- Requirements:
  - Slow Control: DCS should be able to switch off selected modules.
  - Fast Response: Over-voltage protection.
  - Residual voltage (when module off) < 100mV
  - During normal operation (module on) protection draws no power.
  - Minimise number of components, area of components and bus-cable lines.
  - Radiation hardness.
- Impementation for Pixel Stave:
  - Module Protection Chip.

SLHC-PP, Feb 2010   Fabian Hügging, University of Bonn   11
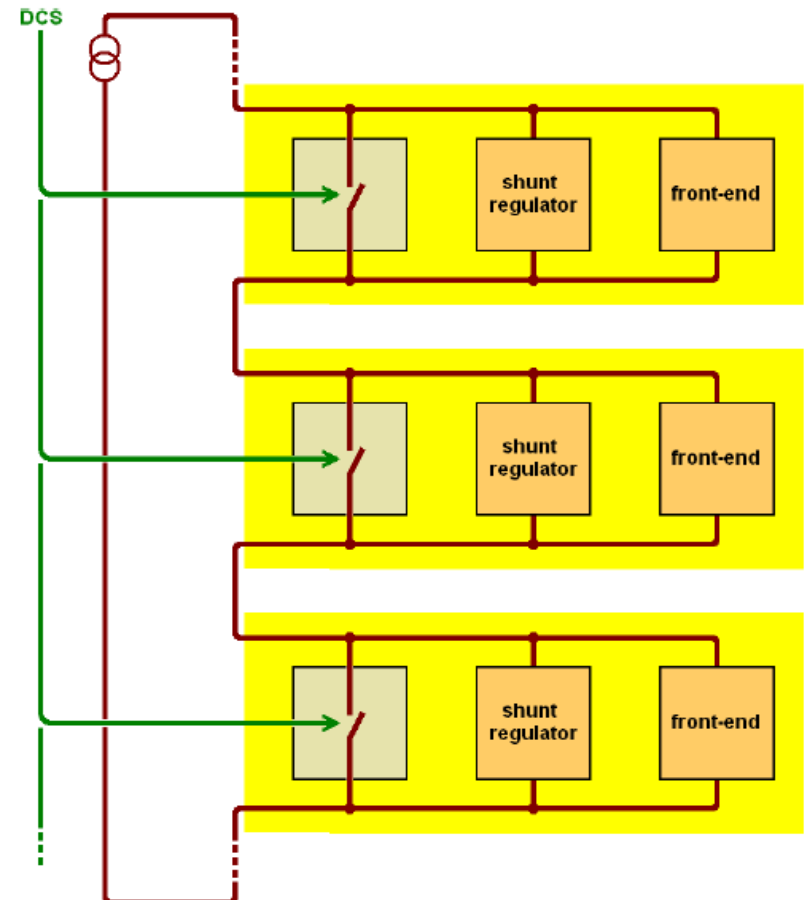
Protection for Serially Powered Staves
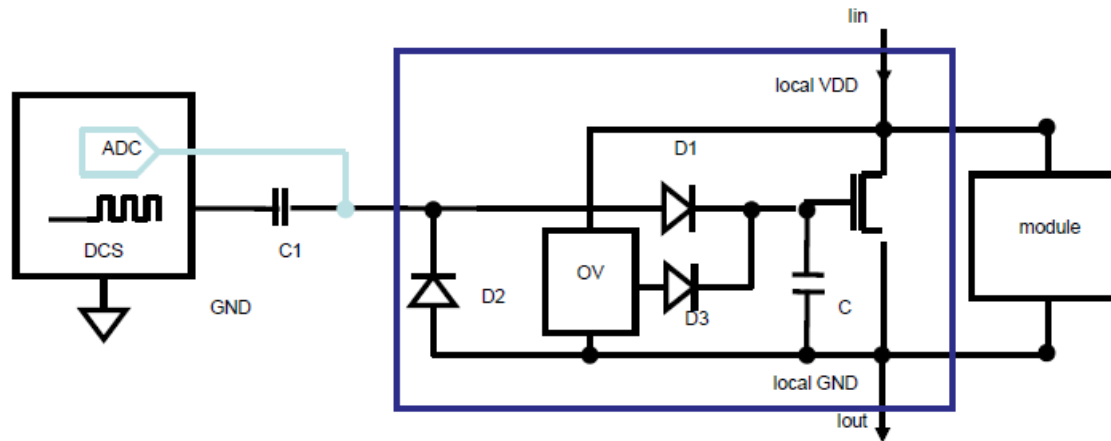
- 130nm CMOS technology.
- bypass transistor.
- AC-coupled slow control line:
  - can be used to monitor module voltage when idle.
- independent over voltage protection circuitry.
- development status (see L. Gonella's talk):
  - bypass transistor and slow control simulations completed.
  - over voltage protection circuitry in development.

universität**bonn** **AC coupling**

- AC-coupling at LVDS TX/RX level:
    - Simple and less material.
    - Requires DC-balance and self-biased RX inputs.
    - Integrated self-biasing circuitry for LVDS RX input will be added in FE-I4.
        - design finished.
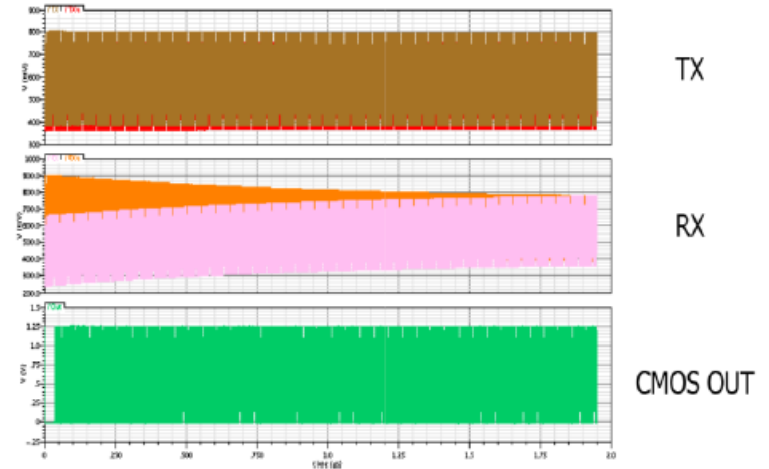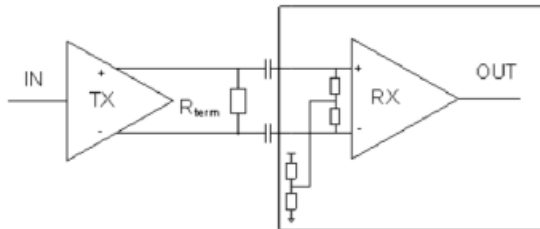
- Otherwise usage of a link with feedback:
    - Used successfully in SP Proof of Principle.
    - No need for DC balancing and self-biasing.
    - Acts also as well as a fail safe (keeps the last state).
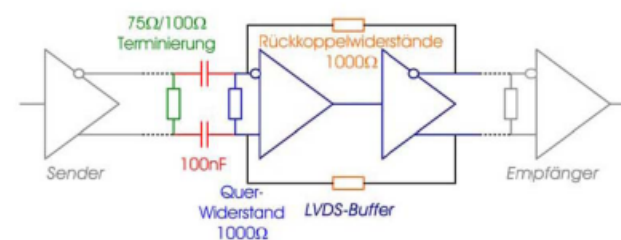
1 HV channel for 8 sCHIPs
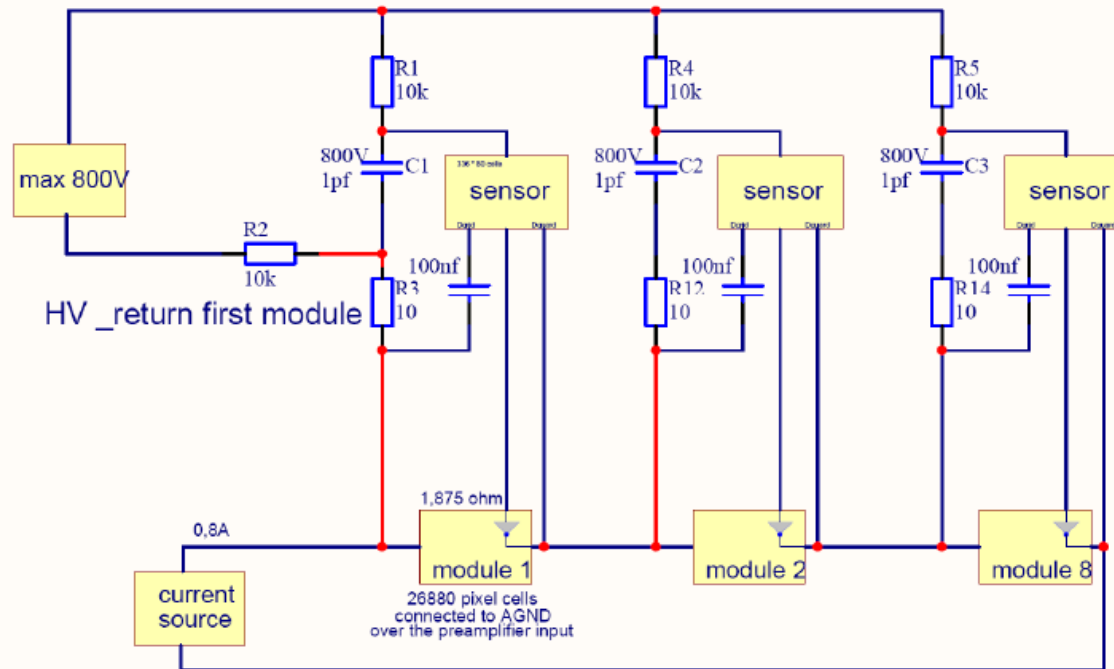
Stave Emulator Test Bench

▶ The stave emulator is a test system which allows to evaluate system aspects and custom developed hardware for the ATLAS Pixel Detector for sLHC, such as

- ▶ physical layer data transmission: LVDS drivers/receivers, cables, connectors, …
- ▶ data coding schemes: raw, 8B/10B, 64B/66B, …
- ▶ powering concepts: serial, dc-dc, switched cap, …
- ▶ DCS concepts: voltage monitoring, control of bypass switch, reset, …
- ▶ data management of the End-Of-Stave controller, …
- ▶ …

▶ It uses

- ▶ FPGAs to emulate the modules and the end-of-stave controller
- ▶ interconnection boards to provide support for different cable and connector options, LVDS transceiver chips, power supply options (parallel, DC/DC or SP), AC-coupling
- ▶ a DCS test board (COBOLT) developed in Wuppertal providing multi-channel ADC and GPIO to test DCS functionalities

→ flexible and realistic test bench
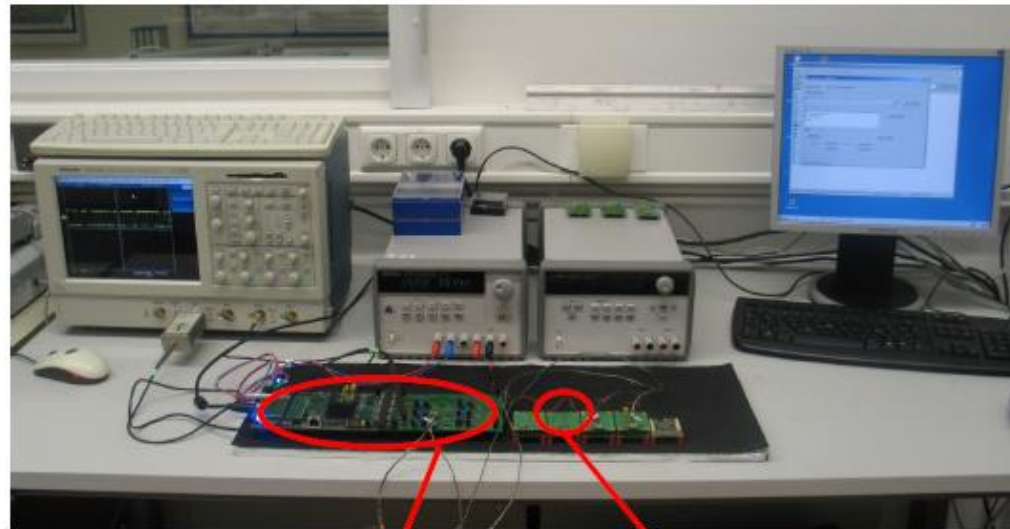
Stave Emulator

End-Of-Stave emulator unit

Module emulator unit

▶ 3

L. Gonella - SLHC-PP Annual Meeting - Feb. 2010

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Baseline Design
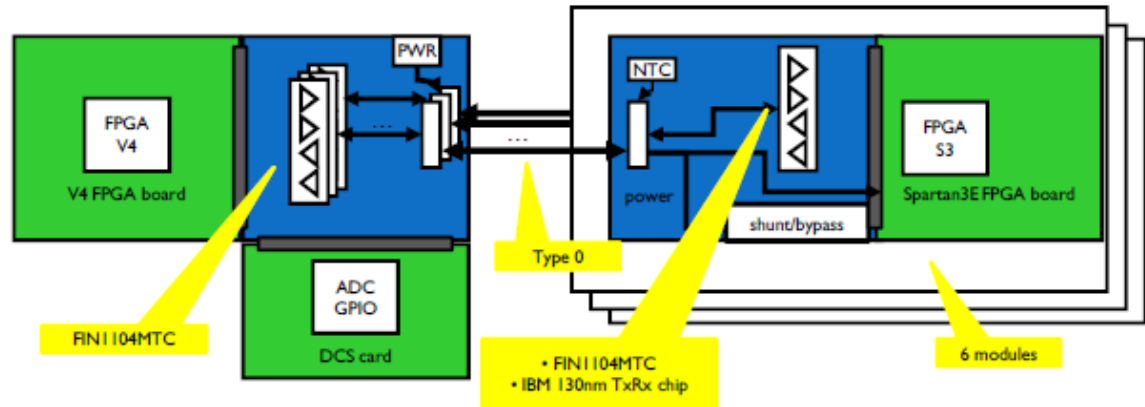
▸ "6 modules-stave"

▸ Connection EoS - module using Type 0 cable

▸ Powering

  ▸ parallel

  ▸ serial using commercial shunt regulator

    ▸ commercial bypass transistor on modules to test protection option

▸ DC-coupled data transmission with different LVDS transceiver chips

  ▸ on End-Of-Stave side: commercial FIN1104MTC transceiver chip

  ▸ on module side: commercial FIN1104MTC or IBM 130nm transceiver chip (i.e. FE-I4 LVDS TX and RX)

▸ NTC to measure module temperature

▸ 6

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The SP scheme
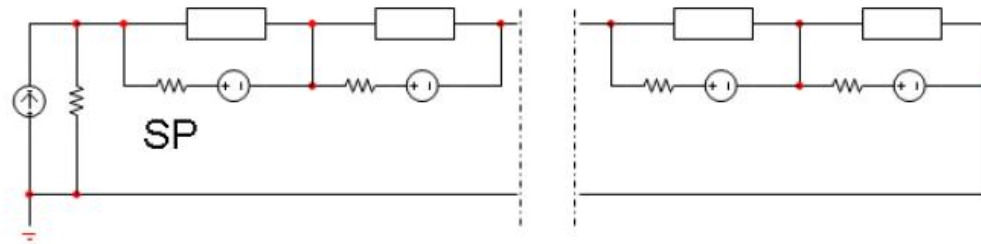
The Serial arrangement is Norton equivalent to the Parallel one
At system level, the power to the chain of loads is provided by a **current source**

I_{src}

Serial Powering

> 50m

I_s

Module
Module
Module

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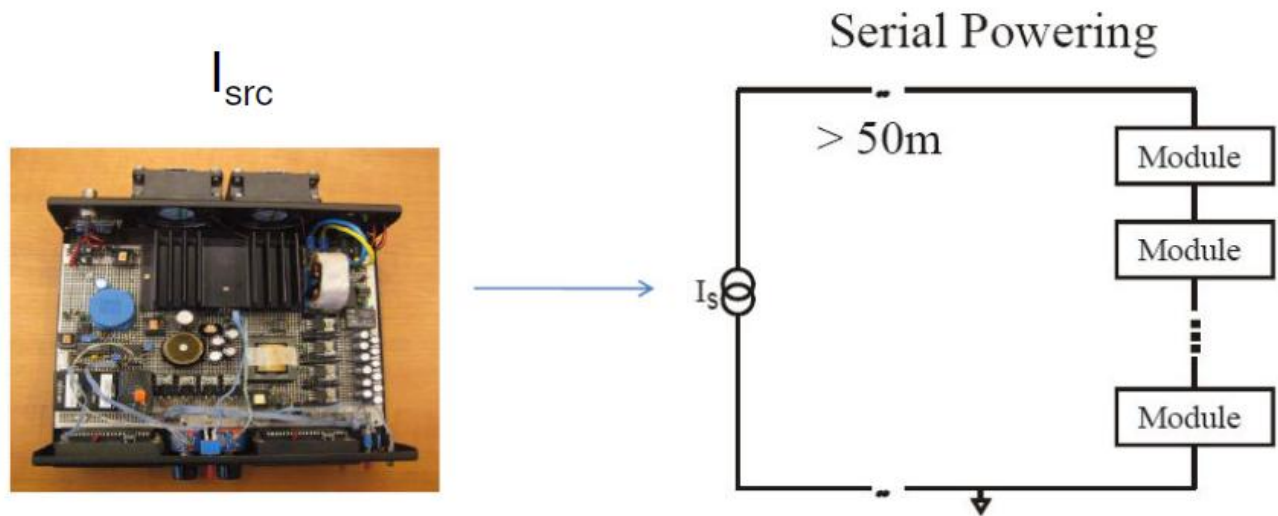
The Current Source

PS prototype@3A&32V dynamic impedance
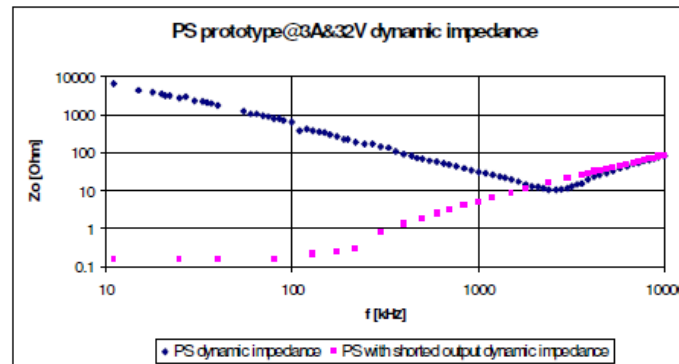
First current source prototype
(J.Stastny, ASCR)

• initially a standard power supply, configured in CC was used

• the first **current source prototype performed well**

• a much more flexible **programmable CS** has been specified and is being prototyped
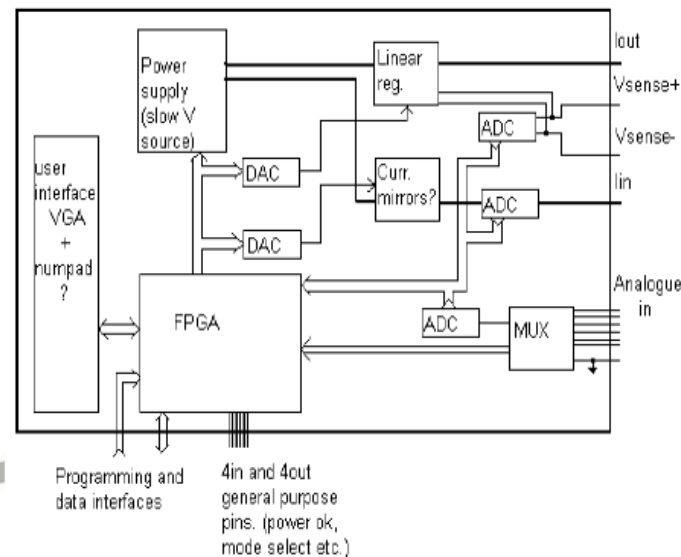
The SP stave for upgraded SCT
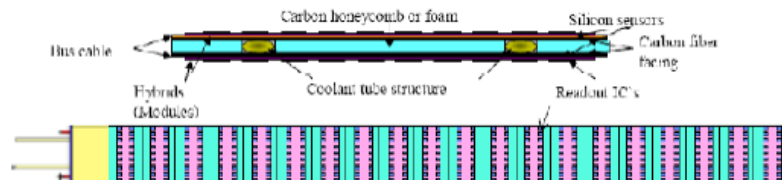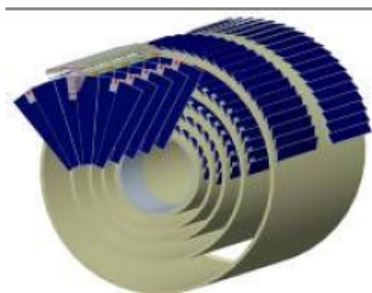
detector staves arranged into barrels
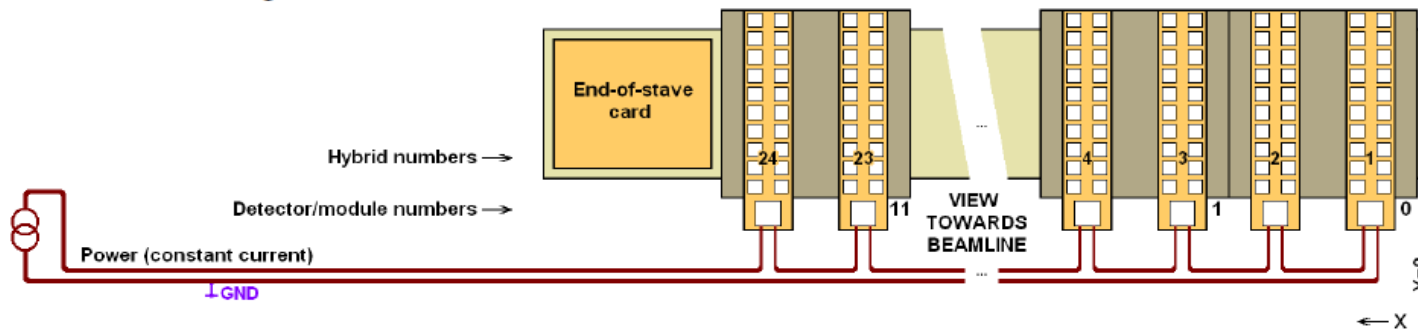
The staves carry 12 detectors, 24 readout hybrids on each side
each hybrid carries 20 ABCn ROICs
In the Serial Powering option each hybrid implements a **shunt regulator** based power supply

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Task 8.2: Serial powering

http://cern.ch/SLHC-PP

Stave load
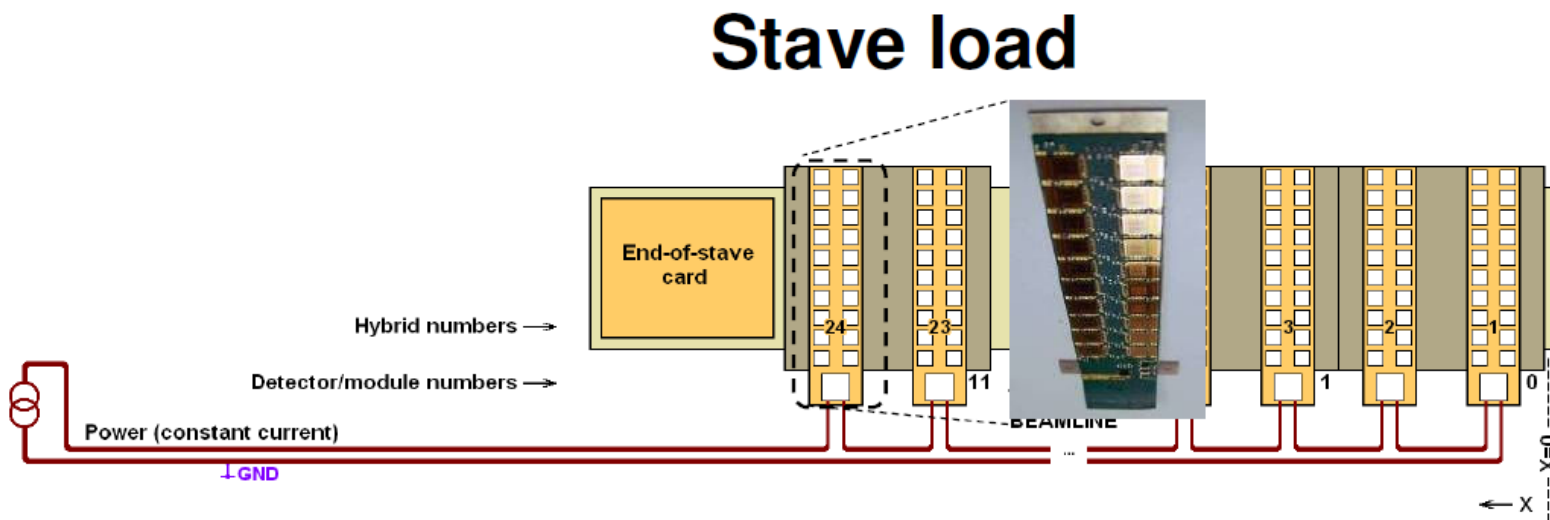
- Each load is represented by 20 **ABCN25 on hybrid**

- ABCN-25 is 0.25 µm CMOS ROIC prototype

- Hybrid to serve 100 mm x 100 mm sensors

- Prototype for ATLAS SLHC short strip tracker

RAL single chip PCB and Liverpool Hybrid

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ABCN25 hybrid

- **strong variations** of **current** are unexpected feature of ABCN-25

- cause still under investigation

- hybrid current has sharp peaks (~1.5 A over ~ms) ⇔ **challenging test of SP circuitry**

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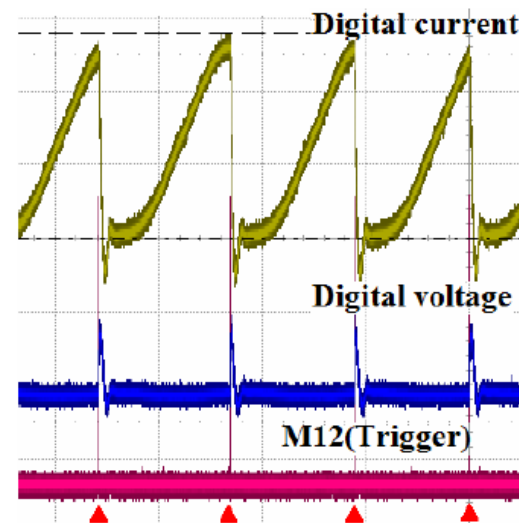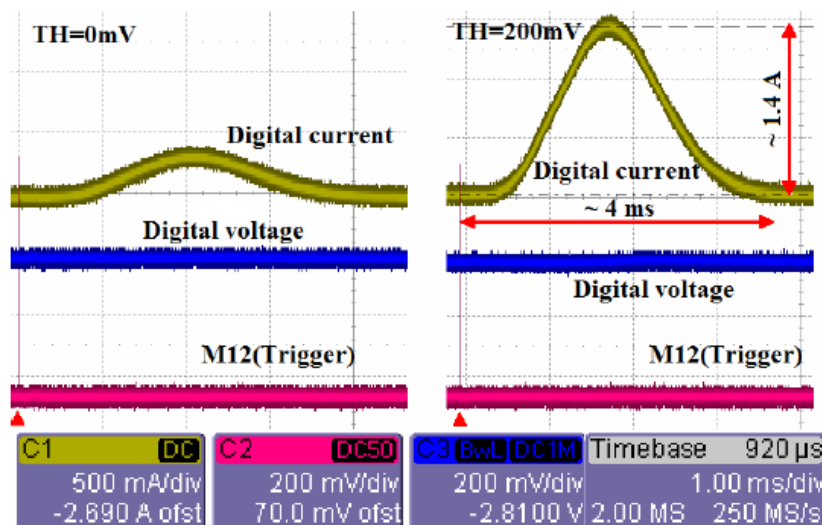
Task 8.2: Serial powering

Shunt regulator architectures

- **Hybrid with Shunt "W"**
  - Use each ABCN's integrated shunt regulator
  - Use each ABCN's integrated shunt transistor(s)
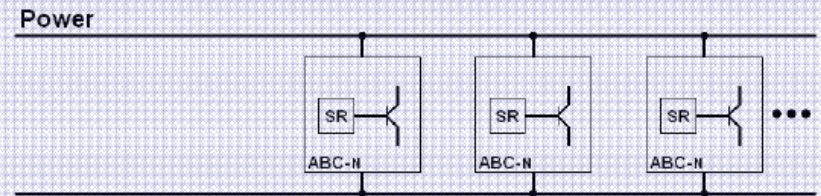
- **Hybrid with Shunt "M"**
  - Use one external shunt regulator
  - Use each ABCN's integrated shunt transistor(s)
    - Two (redundant) shunt transistors, 140mA each
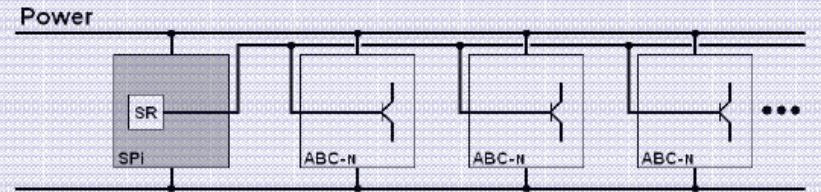
- **Hybrid with SPi (or similar)**
  - Use one external shunt regulator
  - Use one external power transistor

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W scheme - Results

Conceptual diagram of the distributed shunt

Features

• one shunt device per chip

• one shunt regulator per chip

• no external components

• sophisticated **over-current protection**

Stress test. Shunt stands huge currents (~ A) without damage

IR camera pictures during operation

37,26°C
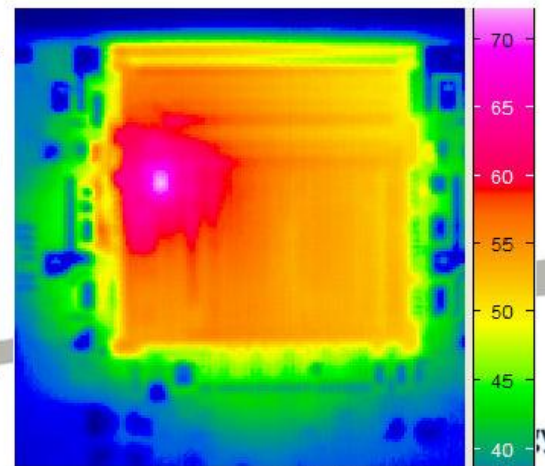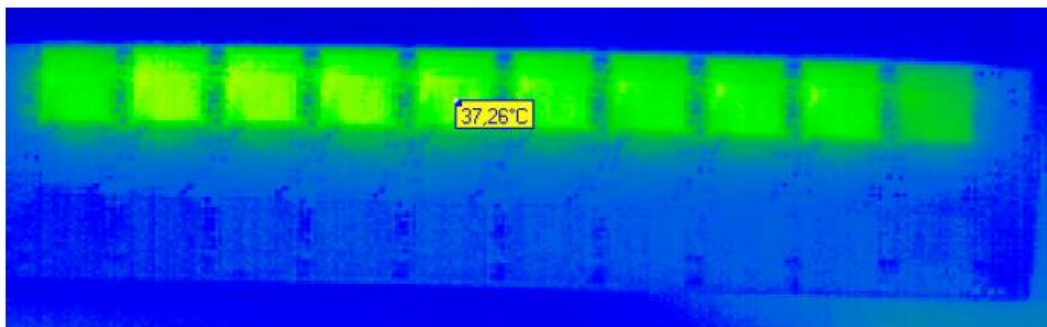
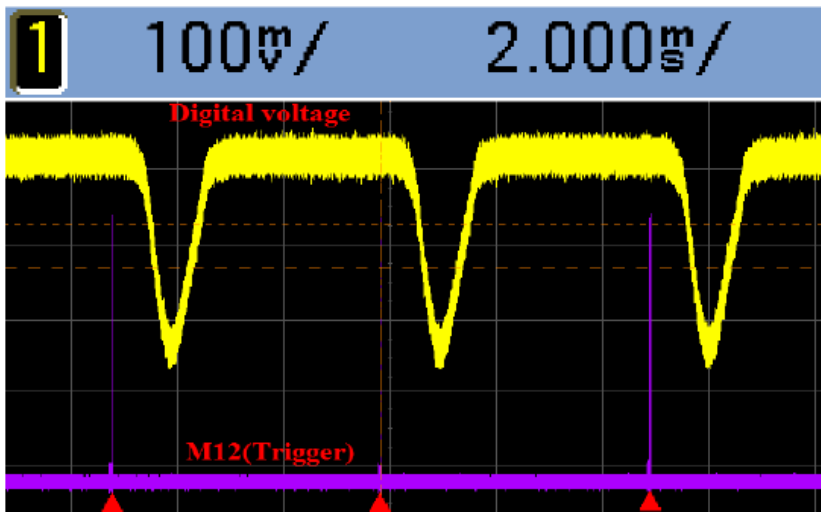**Over-current protection distributes excess current equally after turning off the clock in 10 chip hybrid**
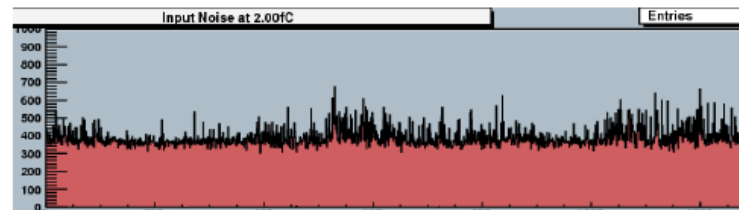
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Task 8.2: Serial powering

W scheme - Results
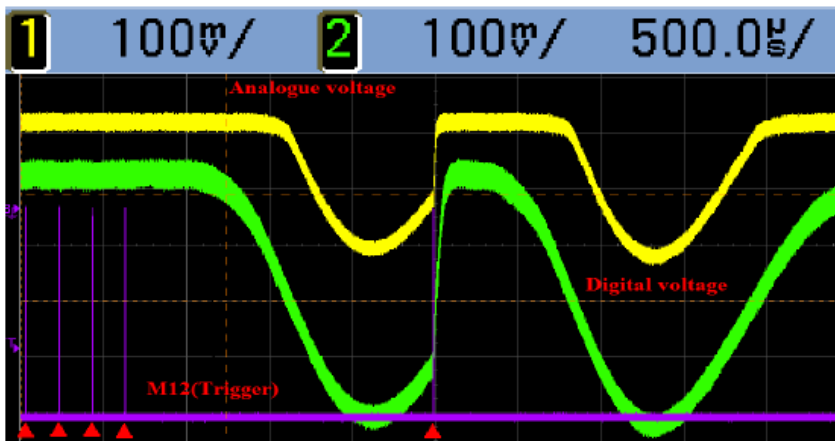
Bumps and the voltages @ 3.8A

Corresponding ENC plot

• W scheme performs well **if** triggers timed **to avoid current bump**

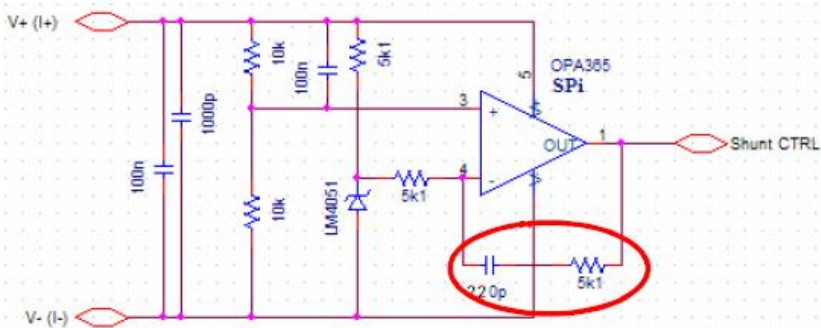• DAQ could be set-up to accommodate bump if required.

Separated bumps and the voltages @ 4.2A
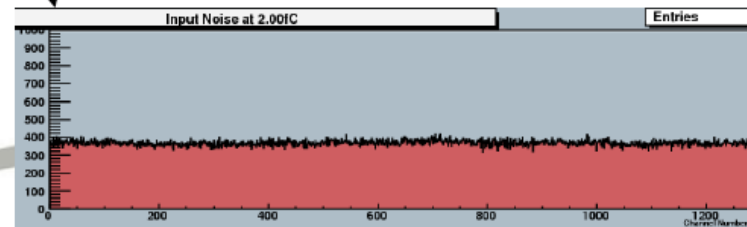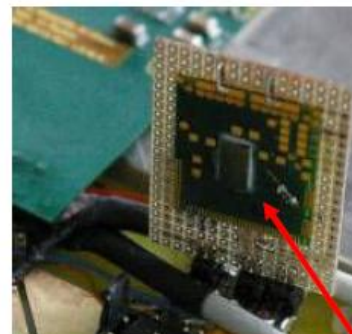
450e⁻ RMS Corresponding ENC plot

Task 8.2: Serial powering

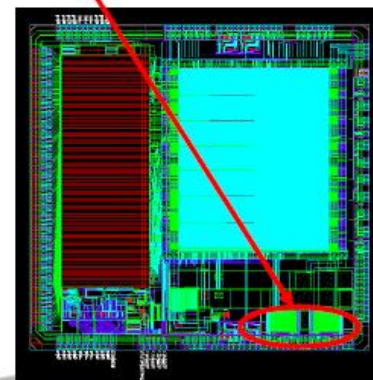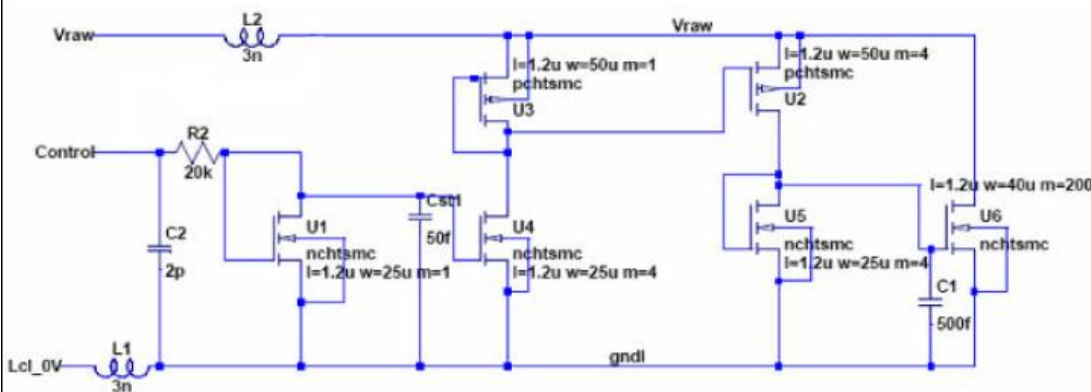**M scheme - Results**

schematic of the external driver

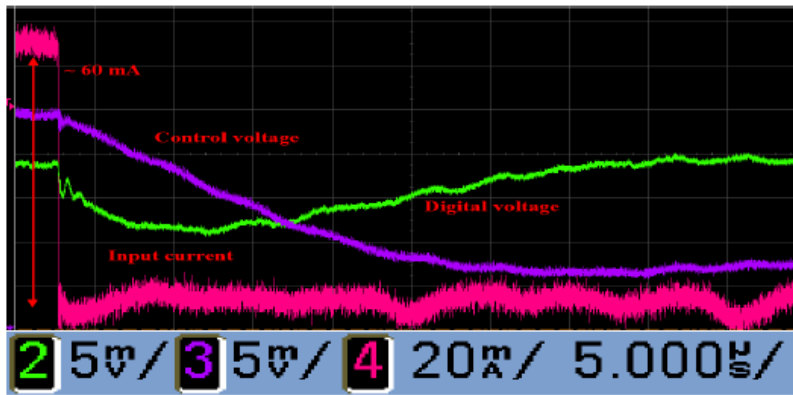implementation with SPi and discretes

Schematic of shunt driver

implementation in ABCN-25

Next version in 130 nm

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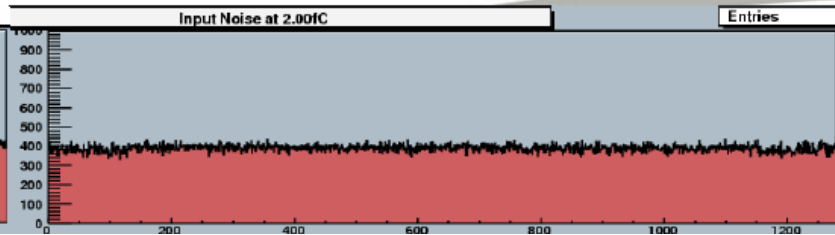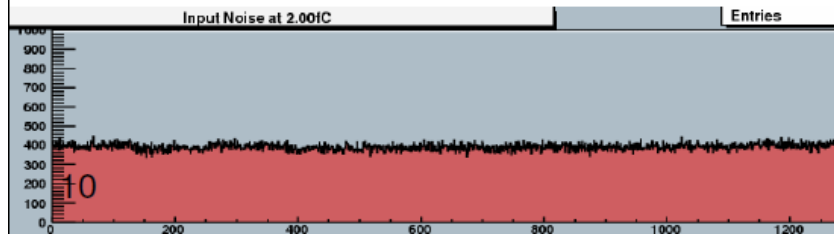
M scheme - Results
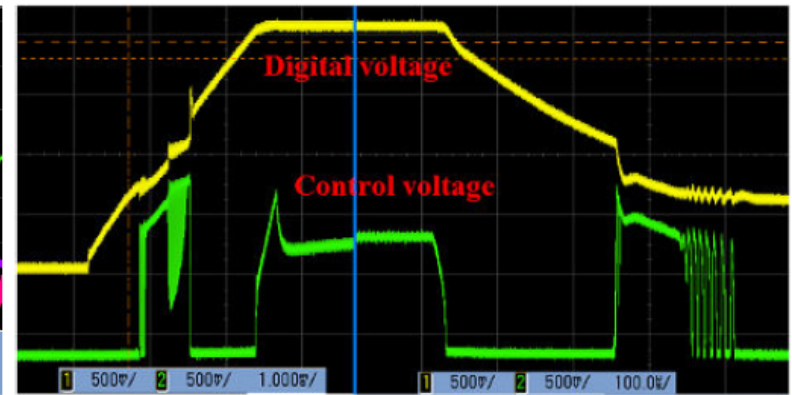
Response to a current step | Start-up | Shut-down

- The **transient response** to a current step is excellent

- The **start-up** works well

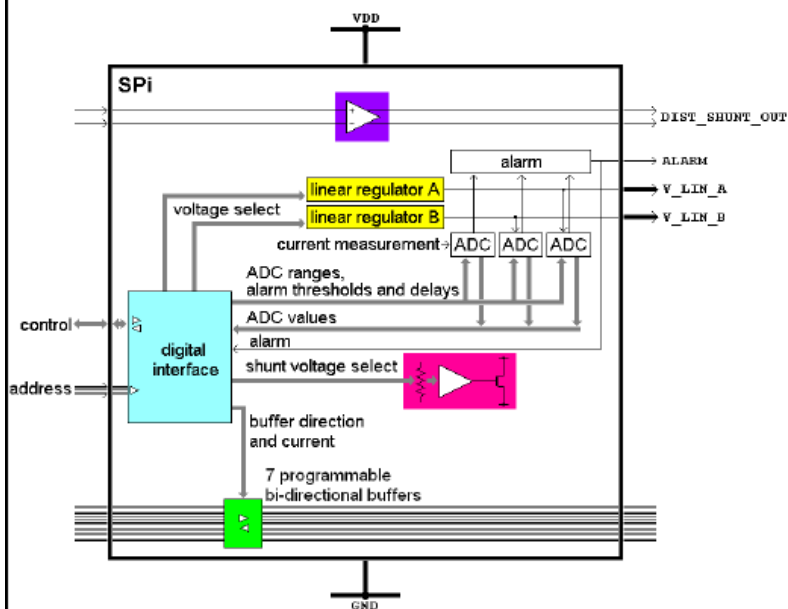- **ENC** is as simulated and **same as for independent powering**

ENC for all channels of the 20 chip hybrid

Task 8.2: Serial powering
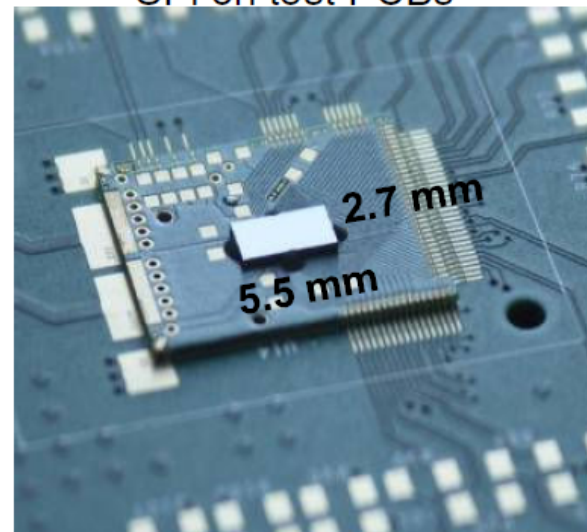
SPi

Serial Power interface. Generic chip in 0.25 μm CMOS. Designed by M. Trimpl (FNAL), M. Newcomer, N.Dressnandt (Penn), specified by RAL.

SPi on test PCBs
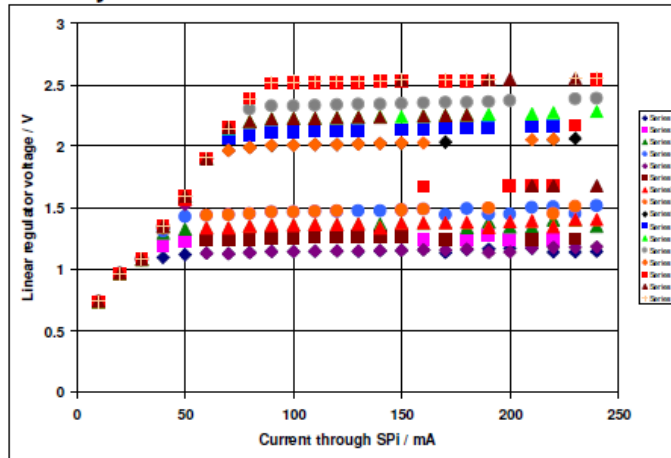
2.7 mm

5.5 mm

- 68 I/O bumps
- 76 power bumps
- Minimum pitch 275 μm

🔴🟣 Two shunt regulator schemes
🟢 Data communication/ AC coupling
🟡🔵 Power management
⚪ Monitoring/alarms

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Example tests on SPi

Programmable linear regulators (mostly) work reliably

Programmable shunt regulator OK

2.5 V

1.5 V

Shunt current

Power line

Communication works well

Clock

Data in

Data out
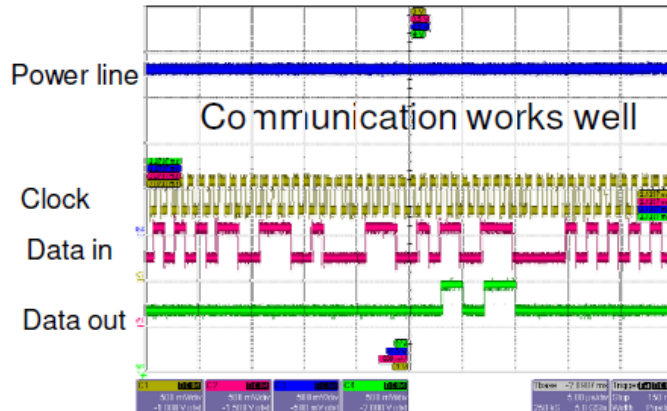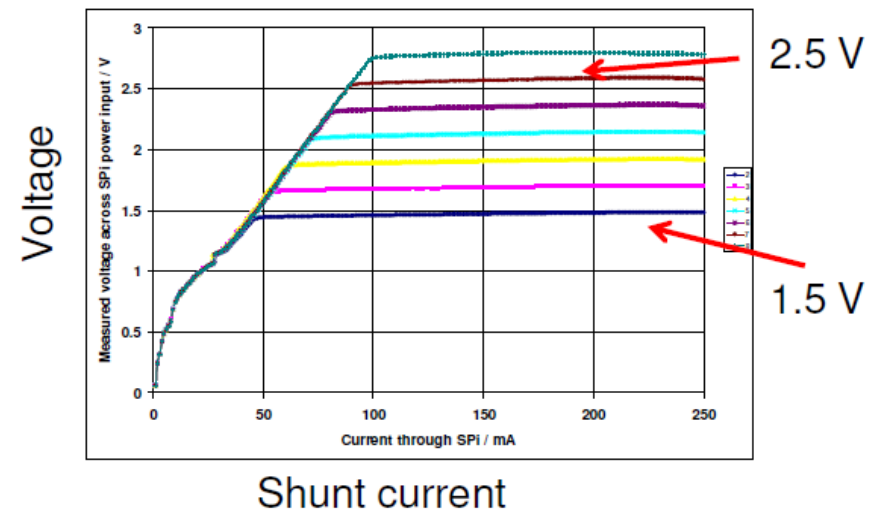
- SPi is being used with the ABCN hybrid for M and SPi scheme with encouraging results.

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SP Protection schemes
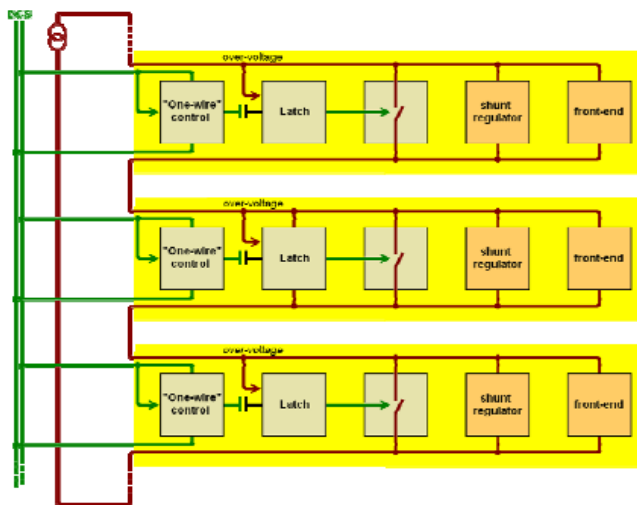
Whilst demonstration staves have generally been reliable:
- What happens if a module fails to an open circuit?
- What happens if a module becomes a noise generator?
- How to turn modules on/off?

We could provide a system to "short out" each module under control of DCS or automatically:
- Voltage across shorted module should be small (<100mV)
- Area of components and number of control lines must be small
- Automatic shorting (over current and over voltage protection)
- Protection circuit must draw no (minimal) power when module active
- Ability to put modules into "stand by" (low power state)

SP Protection schemes
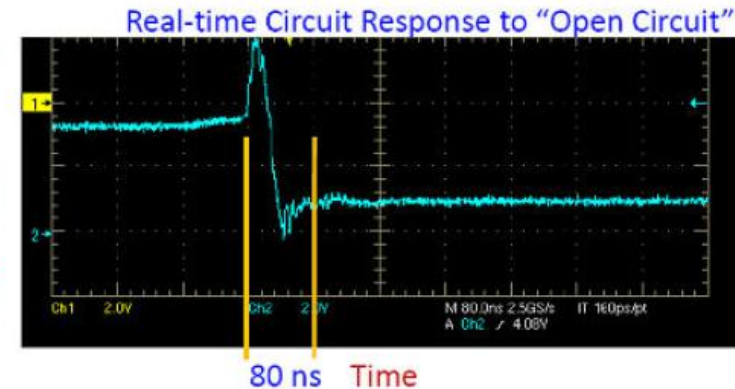
An independent protection and module by-passing function would improve reliability of SP

LBL Discrete schematic – PCB implantation
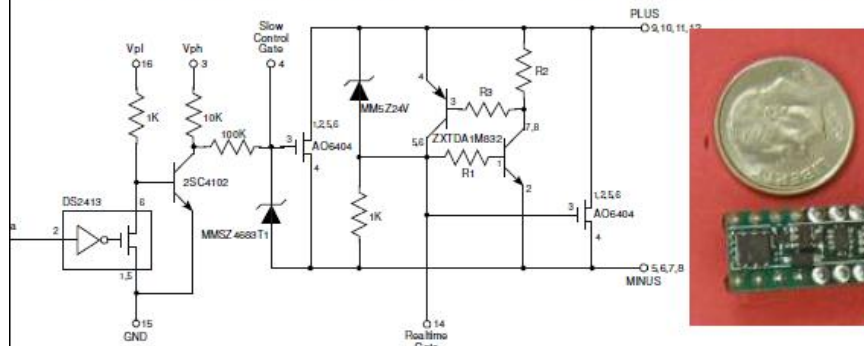
- The discrete version is functional and will be on the stavelets.
- It allows insertion of plug-in board for different powering options
- Plan to get the custom implementation out next spring (2010)?.

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Task 8.2: Serial powering

SP High Voltage schemes
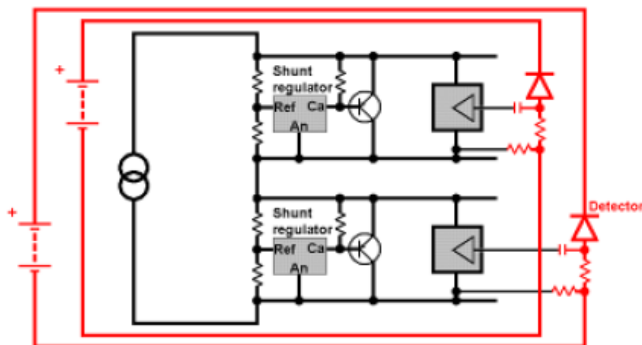
Standard HV powering: **one HV per module**
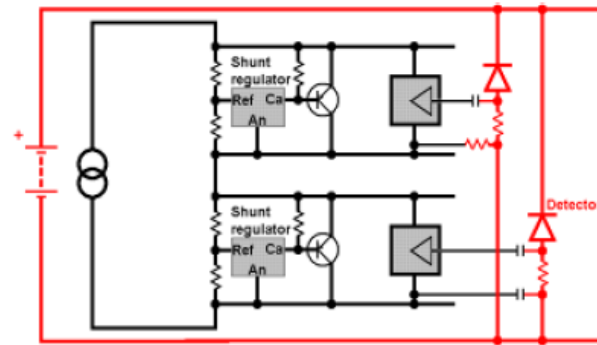
Alternative HV powering: **one HV supply per M modules**

- Serial Powering is compatible with the use of a **single HV supply for several modules**

- Each sensor is dynamically connected to current source ground through output impedances of the chain of shunt regulators

- Low shunt output impedance is crucial to achieve good 'grounding' and reduce noise

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The stavelets

ATLAS community stavelets are planned

Data & hybrid communication

Power & power control communication (SPi)

The power plug-in concept

Distributed   SPi   DC-DC
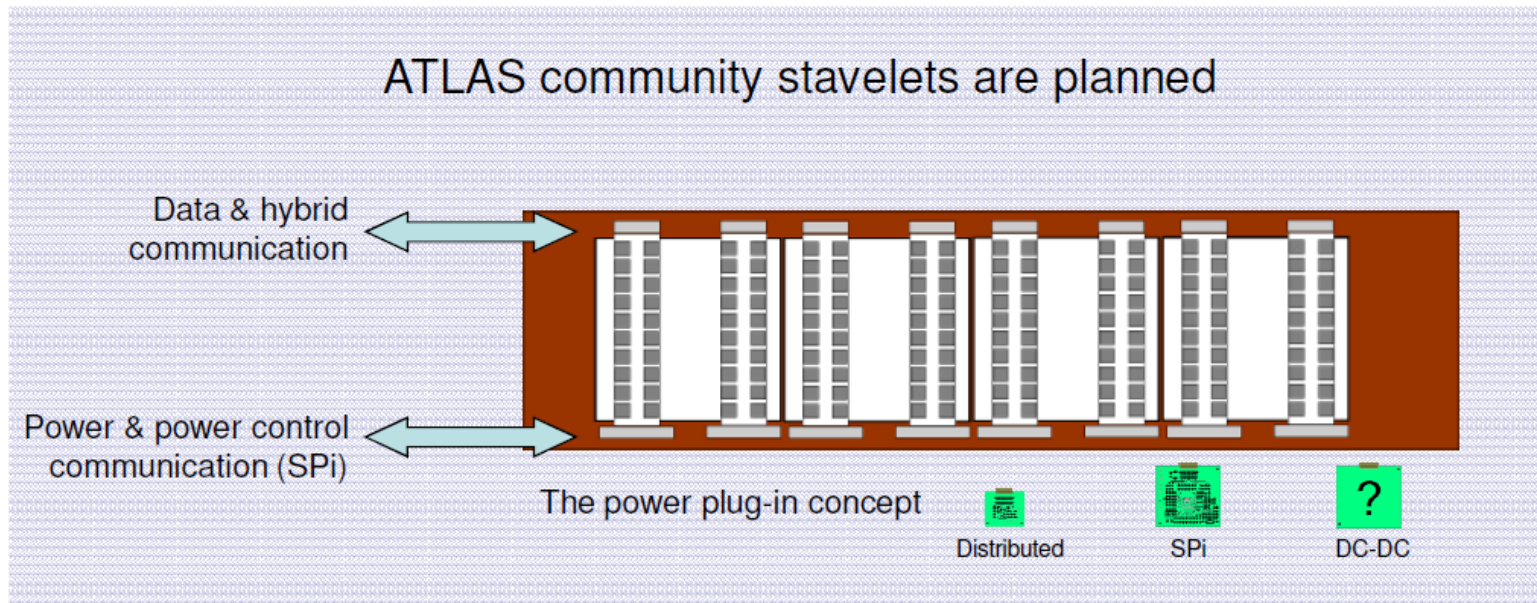
- It allows comparison of different power configurations
- Different bus cable designs
- Different grounding and shielding concepts
- Stavelets early 2010, realistic stave 09 late 2010 ?
- Stavelets allow testing of different powering options

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Task 8.2: Serial powering

Stavelet construction progress at RAL

Module placement area
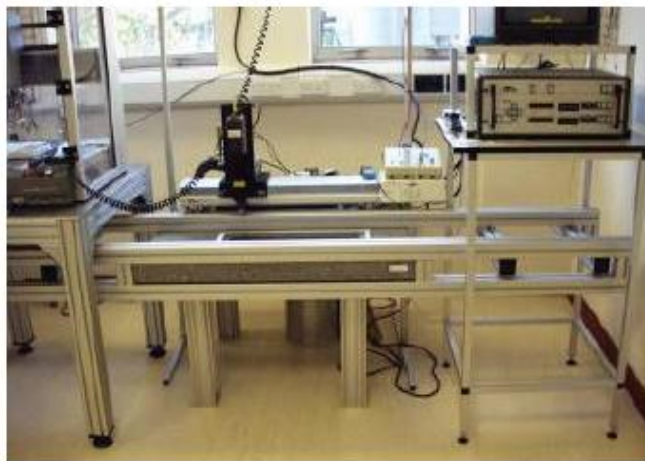
Glue pattern trials
(left - on test board , right – on test bus cable)

Module placement arm

Rotate stage   ZX stages   Y stage

Stavelet test box

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Task 8.2: Serial powering

http://cern.ch/SLHC-PP

SLHC-PP Annual Meeting
4-5 February 2009

Wladek Dabrowski
AGH-UST, Krakow

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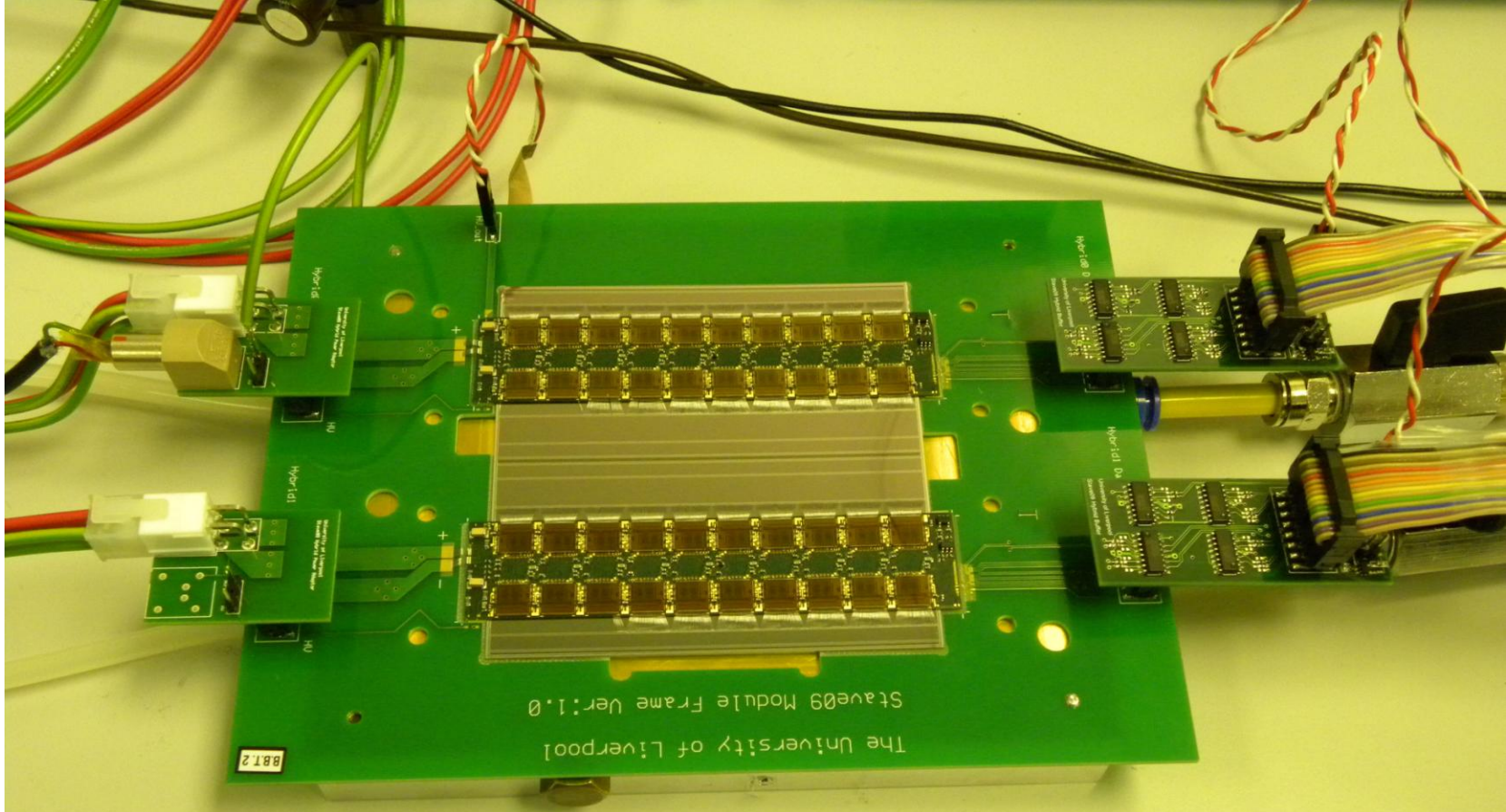
Assembled stavelet

Task 8.2: Serial powering

Protection board assembly and testing

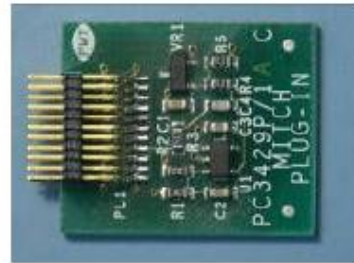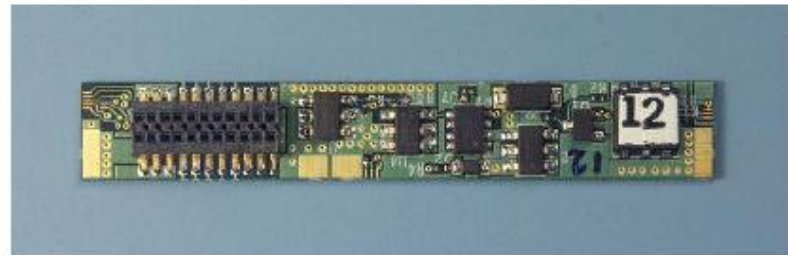Plug in boards for testing different serial powering schemes to be mounted onto PPB provided by BNL (received last week)

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Serial powering R&D - highlights

Radiation resistant ASICs for serial powering schemes have been developed (SHULDO, SPi, two optional regulator integrated in the ABCN-25).

Proof of principle for signal AC coupling has been demonstrated.

Dedicated current source unit has been developed.

Module protection schemes have been worked out, prototypes built of discrete components.

Full size silicon strip modules have been powered successfully using different options of the developed shunt regulators.

Serial powering is the baseline option for the Atlas Stave09 project but testing DC-DC converters is possible.

Work on implementing the serial powering circuits in 130 nm CMOS has been started.

SLHC-PP Annual Meeting 4-5 February 2009

Wladek Dabrowski AGH-UST, Krakow

Documentation/reporting

B. Allongue, G. Blanchot, F. Faccio, C. Fuentes, S. Michelis,c, S. Orlandi
System Integration Issues of DC to DC converters in the sLHC Trackers. TWEPP-09

S.Michelis, C. Azra,B.Allongue, G.Blanchot, F.Faccio, C.Fuentes, S.Orlandi
ASIC buck converter prototypes for LHC upgrades. TWEPP-09

M. Bochenek, W. Dabrowski, F. Faccio, J. Kaplon
An integrated DC-DC step-up charge pump and step-down converter in 130 nm technology. TWEPP-09

F.Faccio, G.Blanchot, S.Michelis, C.Fuentes, B.Allongue, S.Orlandi.
Irradiation results of technologies for a custom DC-DC converter. TWEPP-09

F.Faccio
Roadmap for power distribution using DCDC converters. TWEPP-09

K. Klein, L. Feld, R. Jussen, W. Karpinski, J. Merz, J. Sammet
Experimental Studies Towards a DC-DC Conversion Powering Scheme for the CMS Silicon Strip Tracker at SLHC. TWEPP-09

T. Tica, P. W. Phillips, M. Weber
Performance and Comparison of Custom Serial Powering Regulators and Architectures for SLHC Silicon Trackers. TWEPP-09

Richard Holt
SPi test results. TWEPP-09

Marc Weber, RAL
Roadmap for serial powering. TWEPP-09

F. Anghinolfi, W. Dabrowski, N. Dressnandt, J. Kaplon, D. La Marra, M. Newcomer, S. Pernecker, K. Poltorak, K. Swientek
Performance of the ABCN-25 readout chip for the ATLAS Inner Detector Upgrade. TWEPP-09

Documentation/reporting

F. Huegging, D. Arutinov, M. Barbero, A. Eyring, L. Gonella, M. Karagounis, H. Krueger, N. Wermes
Development of Serial Powering for the Upgrade of the ATLAS Pixel Detector.
2009 Nuclear Science Symposium and Medical Imaging Conference

M. M. Weber
Serial Powering for Silicon Tracking at the Super-LHC.
2009 Nuclear Science Symposium and Medical Imaging Conference

W. Dabrowski, F. Anghinolfi, N. Dressnandt, M. Dwuznik, J. Kaplon, D. La Marra, M. Newcomer, S. Pernecker, K. Poltorak, S. G. Sevilla, K. Swientek
Design and Performance of the ABCN-25 Readout Chip for the ATLAS Inner Detector Upgrade.
2009 Nuclear Science Symposium and Medical Imaging Conference

C. Fuentes, B. Allongue, S. Buso, G. Blanchot, F. Faccio, S. Michelis, S. Orlandi, G. Spiazzi
Power Distribution with Custom DC-DC Converters for SLHC Trackers.
2009 Nuclear Science Symposium and Medical Imaging Conference

- All tasks of WP8 are on schedule or even ahead of schedule in some cases.

- Sufficient material (papers and talks) for reporting exist already.

- Work towards final demonstrators to be delivered by M36 is progressing well.

- Activity of WP8 if fully coherent with the ATLAS and CMS R&D programs on development of new concepts and technologies for inner trackers.