

ALICE Muon IDentifier (MID) Status and Plans



New Resistive Plate Chamber (RPC) detectors

New Front-End Electronics for the RPCs (FEERIC project)

Wireless FEERIC threshold distribution

Readout Electronics



The ALICE Muon Identifier (MID) for LHC run3-4



Motivations

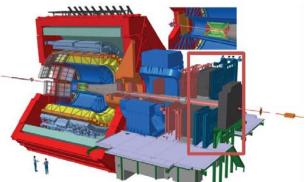
- Precision measurements of the QGP properties during LHC run3-4
- Lol for the ALICE Upgrade, CERN-LHCC-2012-012, <u>http://cds.cern.ch/record/1475243</u>

Conditions

- High interaction rate after run2: 50 kHz in Pb-Pb
- To be compared to ~10 kHz peak during LHC run2

Strategy

- Hardware triggers not very selective in HI
 - \Rightarrow readout all Min-Bias and/or continuous readout
 - \Rightarrow online reduction (O² project)



• Large statistics : Pb-Pb at $\sqrt{s=5.5}$ TeV, $L_{INT} \sim 13$ nb⁻¹ (>10¹¹ Min-Bias events)

□ Muon IDentifier (MID) = upgrade of present Muon TRigger (MTR) system

- Readout and Trigger electronics TDR, http://cds.cern.ch/record/1603472
- MTR: 72 Resistive Plate Chambers (140 m²), 21k FE ch., muon p_T based trigger decision
- MID
 - \Rightarrow **Provides muon identification** (match with MFT/MCH tracks behind thick iron wall)
 - \Rightarrow Continuous readout (new Readout Electronics), very reduced trigger capabilities
 - \Rightarrow 1/3 new RPCs, new Front-End Electronics

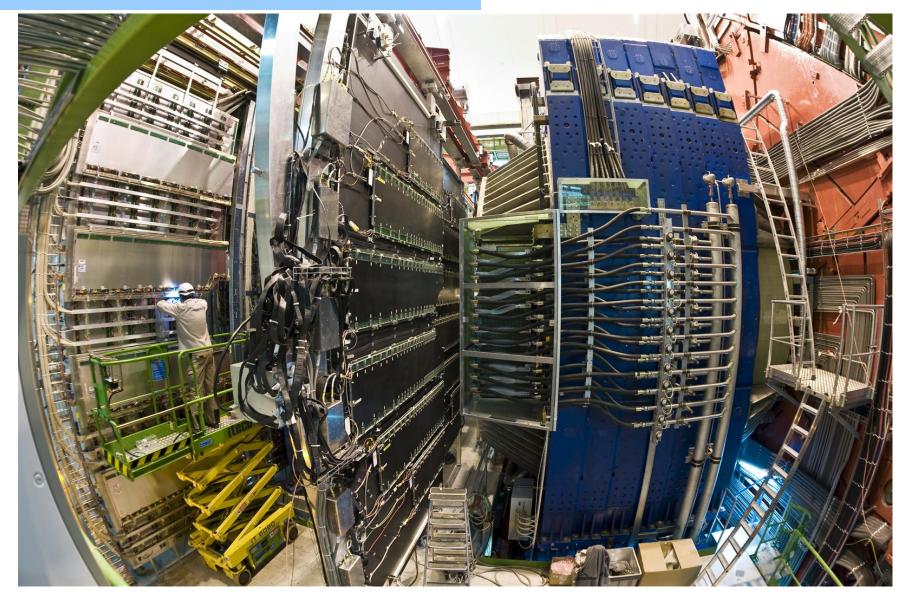
□ Installation during LS2 (2019-2020), data taking during LHC run3 and run4





MTR picture







MID : new RPC production and tests

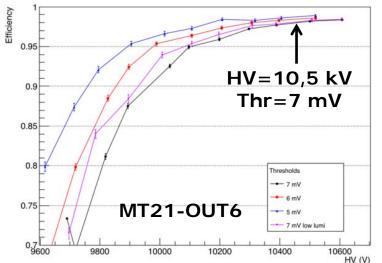


- □ Goal: replace the 24 most irradiated RPCs (out of 72) and other RPCs showing ageing at the end of Run2
- D Production status
 - 30 RPCs produced so far
 - 20 more in production

Test status

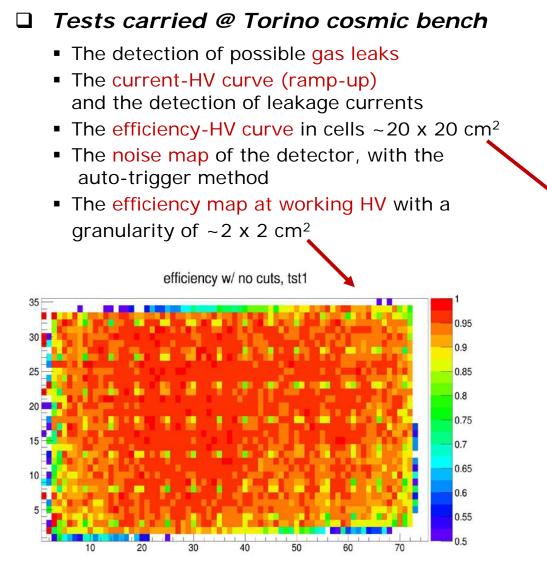
- Ongoing, 16 RPCs already tested
- Present yield ~70%
- Based on the final yield, we will consider building more RPCs → if late for installation, they will be kept as spares
- Two new RPCs installed in ALICE cavern (MT21-OUT6 and MT22-IN3) on 02/18 for long term tests in realistic conditions
 - HV/threshold scan on 04/18
 - High efficiency and stability so far
- Plans
 - Mass production tests (end): 12/18
 - Installation: few weeks during 2019

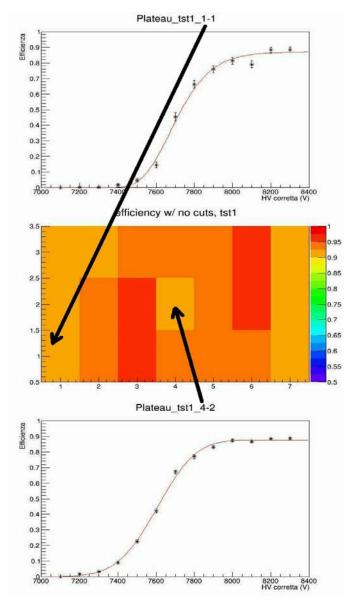
















□ Goal = slow down RPC aging after LS2

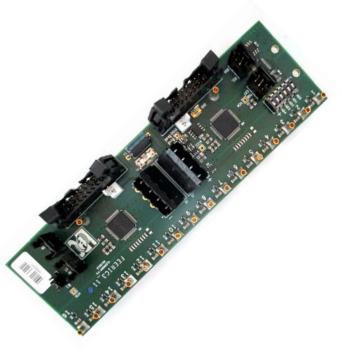
- 20992 ch., 2384 FE cards (+14% spares)
- Present ASIC ADULT: no amplification
- Future ASIC FEERIC with amplification

□ 39 FEERIC cards on 1 (/72) RPC (MT22-IN3) in ALICE cavern since 02/15

- Very satisfactory performance and stability
- Factor 4 less charge released in the RPC gas with FEERIC => reduced aging
- RPC from the new production since 02/18
- □ ASIC production (x5000) validated in two weeks on 06/16 using the prod. test bench
 - Yield > 98%, 60% spare ASIC available
- Card production
 - CERN price enquiry DO-30313/EP/FEERIC
 - Production completed since 01/18

□ Installation of new RPCs and FEERIC cards

- During 2019, ~3 months, not consecutive
- Prepa. of installation (documents, tools) ongoing

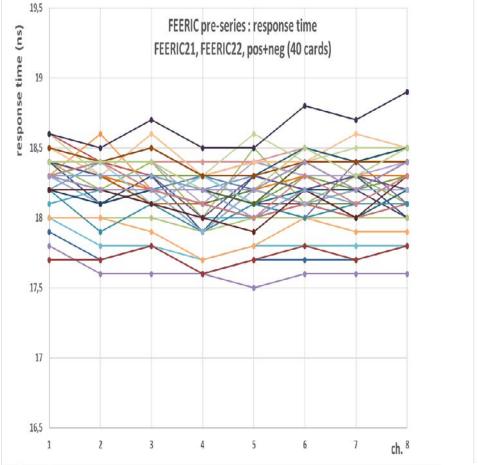




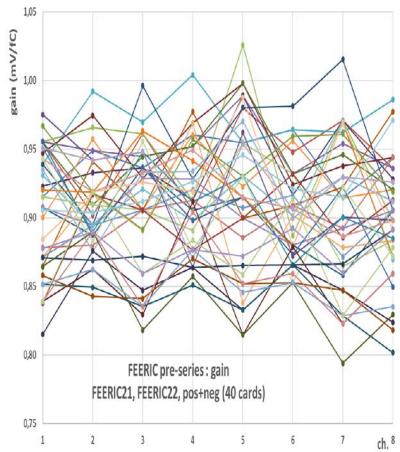


MID : FEERIC *sample* performance ex. of response Time and Gain dispersion





- Response time dispersion < 1,5 ns</p>
- Response time dispersion assumed in PRR is 3 ns (for full prod.)

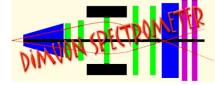


• Gain dispersion ~ $\pm 10\%$

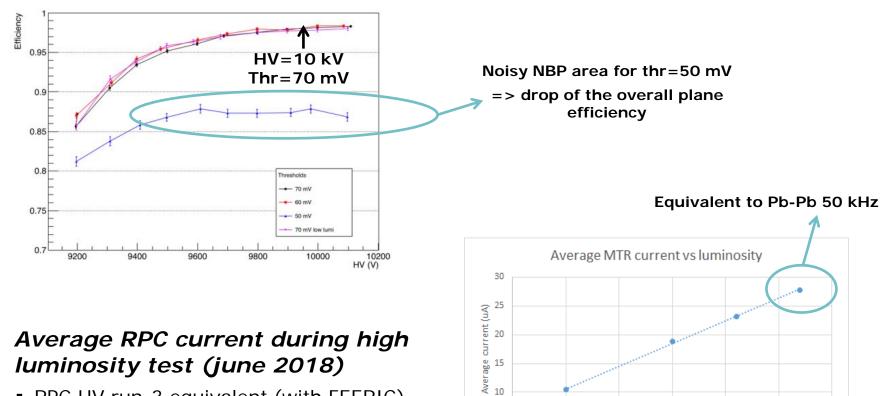
Thesis service task ongoing on analysis of full production dispersion



MID : FEERIC FE Electronics for the RPCs Efficiency and current@high luminosity



- HV/threshold scan (04/18) for the RPC (MT22-IN3) from the new production equipped with FEERIC cards in ALICE cavern
 - High efficiency reached for thr=60 mV and 70 mV (in high and low lumi runs)



5

10

20

30

Average RPC current during high *luminosity test (june 2018)*

- RPC HV run-3 equivalent (with FEERIC)
- No trip, no spike, I_{RPC} linear vs. luminosity up to 50 kHz Pb-Pb equivalent

70

50

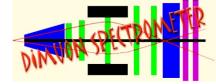
60

40

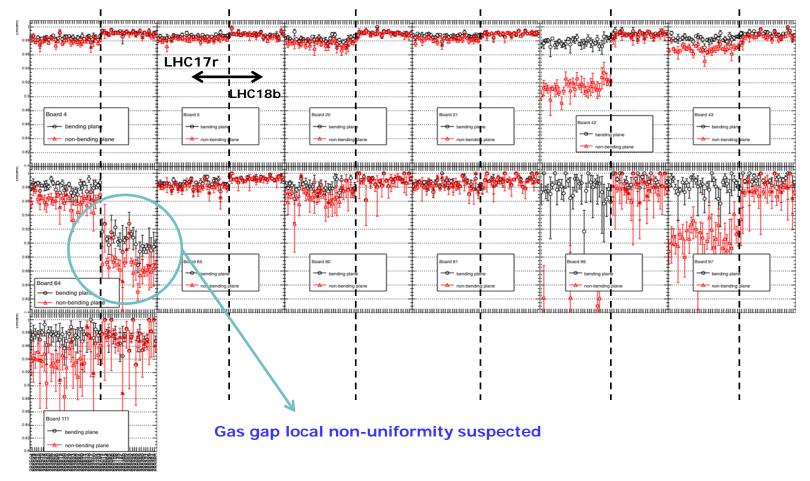
Luminosity (Hz/ub)



MID : FEERIC FE Electronics for the RPCs Efficiency (RPC in ALICE cavern)

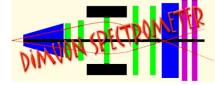


- □ Comparison of MT22-IN3 efficiency between LHC17r and LHC18b periods in standard conditions of operation (all RPC area)
 - High efficiency reached with RPC from new production (LHC18b)





MID : FEERIC wireless threshold distribution



- □ Why going to new -wireless- threshold distribution ?
 - Threshold setting per FEERIC card (vs. per RPC side in the present setup)
 - Possibility of fine tuning locally each RPC working point (common HV, threshold optimization)
- □ Technical choices (discussed at Dec. 2017 ALICE TB)
 - Zigbee high level protocol used (for wireless transmission)
 - SoftWare based on Arduino libs (I2C, SD and Xbee cards)
 - I2C bus between FEERIC cards on each RPC side

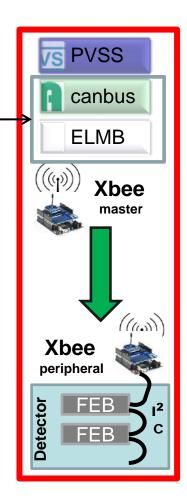
Status

- Wireless threshold Hw/Sw prototype installed in Feb. 2018 on the RPC equipped with FEERIC cards in ALICE cavern
- Long term performance and reliability tests in 2018
- R&D ongoing for ethernet link to Xbee master -



- 24 Xbee peripheral cards
- 2 master cards
- Production, installation
 - end 2018, early 2019







MID : FEERIC wireless threshold distribution

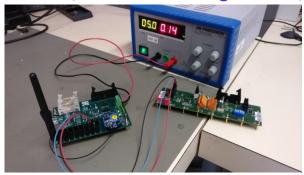


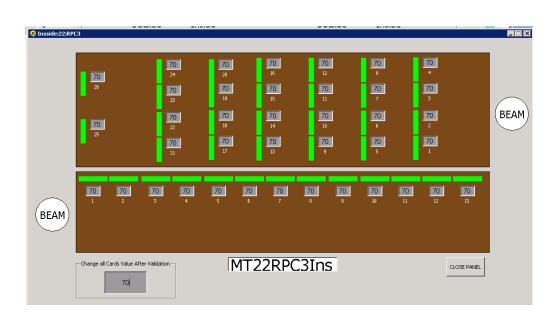
Xbee card description and functionalities

- Same Xbee card for master and peripheral cards (1->12 in ALICE)
- One single FirmWare: master/peripheral role is assigned by SoftWare configuration. By default, a board acts as peripheral
- SD Card for initialisation
- EEPROM for storing/re-loading last used threshold values in case of power cycle
- Whole chain, hw+sw, operational, including PVSS software



Xbee peripheral coupled to FEERIC board (threshold setting via I2C)



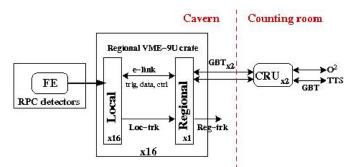


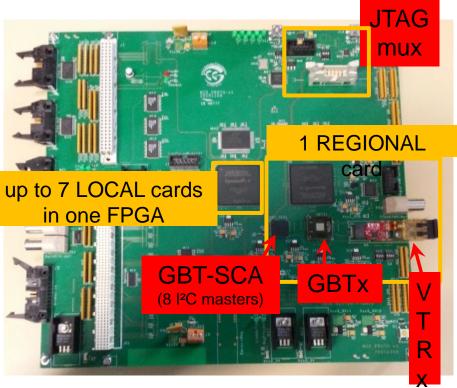


MID : Readout Electronics Prototype



- Readout electronics for continuous mode
- Replacement of the 234 Local and of the 16 Regional cards presently in operation
- Readout card prototype ready since early 2016 (EDR in June 2015) and fully operational
 - Emulate, on the same card, 7 Local cards connected by e-links@320 Mb/s to one Regional card implementing one GBT@3.2 Gb/s (GBTx, GBT-SCA, VTRx)
 - FPGA programming and GBT config. OK
 - Tests of communication with G-RORC (as CRU emulator) validated in Jan. 2017
 - Slow control I2C (via GBT-SCA) OK
 - Advanced FPGA firmware ready
 - Response to HB triggers OK
 - Self-triggered events OK

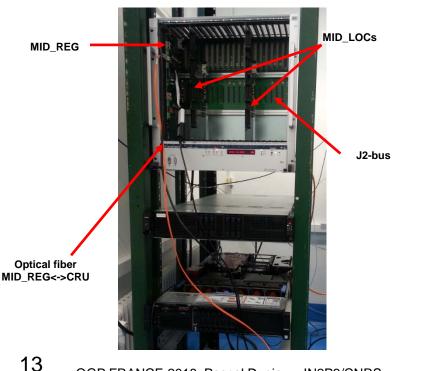


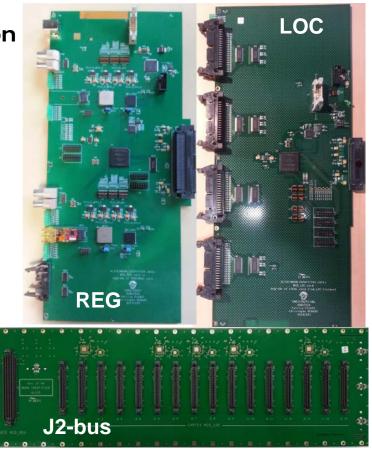


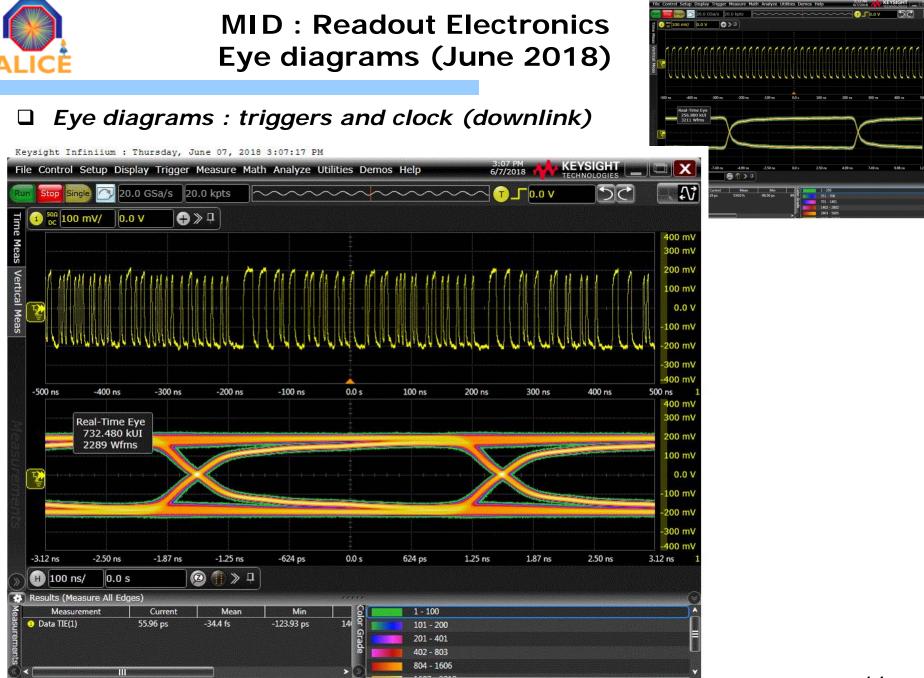




- Pre-series : 3 samples of Local, Regional and J2-bus (between Loc-Reg) produced => full chain tests
- D PRR defended in April 2018 (https://indico.cern.ch/event/719264/)
 - Tests (signal transmission integrity mostly) and Local & Regional card layout to be finalized
 - Full crate (1/16 of total) still to be validated
 - PRR follow-up meeting before production



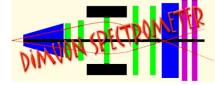




QGP FRANCE 2018, Pascal Dupieux, IN2P3/CNRS

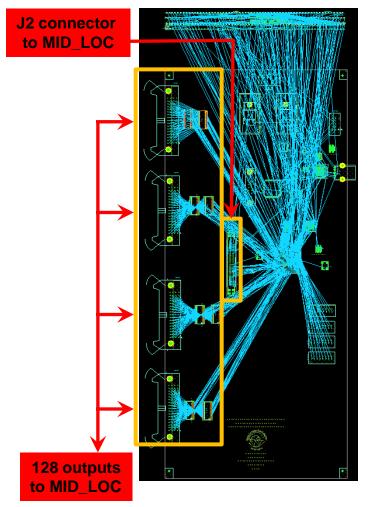


MID : Readout Electronics LOCAL test bench and FEERIC interface



□ MID-TST-LOC

- Layout completed in Subatech
- Routing, production ongoing at LPC



□ *MID-FE-LOC-INTERFACE*

- Support for 8 FEERIC cards
- Delivered by LPC to Subatech







□ ALICE team of South Africa has joined MID project in 2017

- In charge of MID CRU specific code development
- Will be involved in full crate validation
- A test bench has been set up (waiting for LTU, CRU+FLP for completion)
- Output data format is discussed regularly with O2 experts
- Input raw data format and segmentation was provided to SA team by MID readout electronics developer

First release of MID user logics (up-link only) ongoing



MID CRUs

- 2 CRUS of type "24/24" in the counting room
- 1 CRU+FLP from first batch in Subatech for tests of readout electronics (July 2018)
- 1 CRU+FLP req. asap in SA for MID user logics



MID : Overall Schedule



V2.5 (Jan-18)	2015	2016	2017	2018	2019	2020
RPC produced and tested (12/18)						
FEC EDR (3/15)				Ì		
FEC PRR (4/16)		\bigcirc		1		
FEC produced and tested (1/18)						
RPC / FEC installation (01-12/19, 3 months)					\odot	
RO EDR (6/15)	•••					
RO prototype finished (11/15)	\bigcirc					
RO pre-series protos, PRR (18/4/18)						
RO 1(/16) full crate produced and tested (12/18)						
RO produced and tested (06/19)						◆
RO installation (04/20, 15 days)						
Commissioning				,		_