



Contribution ID: 304

Type: Oral

hls4ml: deploying deep learning on FPGAs for trigger and data acquisition

Monday, March 11, 2019 6:00 PM (20 minutes)

Machine learning is becoming ubiquitous across HEP. There is great potential to improve trigger and DAQ performances with it. However, the exploration of such techniques within the field in low latency/power FPGAs has just begun. We present hls4ml, a user-friendly software, based on High-Level Synthesis (HLS), designed to deploy network architectures on FPGAs. As a case study, we use hls4ml for boosted-jet tagging with deep networks at the LHC. We map out resource usage and latency versus network architectures, to identify the typical problem complexity that hls4ml could deal with. We discuss possible applications in current and future HEP experiments.

Primary authors: TRAN, Nhan Viet (Fermi National Accelerator Lab. (US)); PIERINI, Maurizio (CERN); HARRIS, Philip Coleman (Massachusetts Inst. of Technology (US)); JINDARIANI, Sergio (Fermi National Accelerator Lab. (US)); DUARTE, Javier Mauricio (Fermi National Accelerator Lab. (US)); KREIS, Ben (Fermi National Accelerator Lab. (US)); NGADIUBA, Jennifer (CERN); WU, Zhenbin (University of Illinois at Chicago (US)); RANKIN, Dylan Sheldon (Massachusetts Inst. of Technology (US)); SUMMERS, Sioni Paris (Imperial College Sci., Tech. & Med. (GB)); RIVERA, Ryan Allen (Fermi National Accelerator Lab. (US))

Presenter: NGADIUBA, Jennifer (CERN)

Session Classification: Track 2: Data Analysis - Algorithms and Tools

Track Classification: Track 2: Data Analysis - Algorithms and Tools