Contribution ID: **377** Type: **Oral**

Real-time cluster finding for LHCb silicon pixel VELO detector using FPGA

Wednesday 13 March 2019 18:40 (20 minutes)

The hardware trigger L0 will be removed in LHCb upgrade I, and the software High Level Trigger have to process event at full LHC collision rate (30 MHz). This is a huge task, and delegating some low-level time-consuming tasks to FPGA accelerators can be very helpful in saving computing time that can be more usefully devoted to higher level tasks. In particular, the 2-D pixel geometry of the new LHCb VELO detector makes the cluster-finding process a particularly CPU-time demanding task. We present here the first results achieved with a highly parallel clustering algorithm implemented in dedicated FPGA cards, developed in an R&D programme in the context of the LHCb Upgrade I, in view of potential future applications.

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Session Classification: Track 1: Computing Technology for Physics Research

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